M02020

4 Gbps CMOS TIA with AGC

The M02020 is a 4 Gbps TIA achieving a wide input dynamic range to support different transmission distance requirements. Input overload of 2 mA_{PP} is provided to support short-haul fiber optic systems and input sensitivity of approximately -23 dBm is useful for single-mode tests of high power long haul links.

In order to satisfy such high sensitivity and good optical overload requirements, automatic gain control (AGC) is implemented in the M02020. The AGC monitors the output amplitude and automatically reduces the TIA gain when the photodiode current exceeds the AGC threshold, maintaining the output at a constant level.

A replica of the average photodiode current is available at the MON pad for photo-alignment and Receive Power monitoring (SFF-8472 compliant).

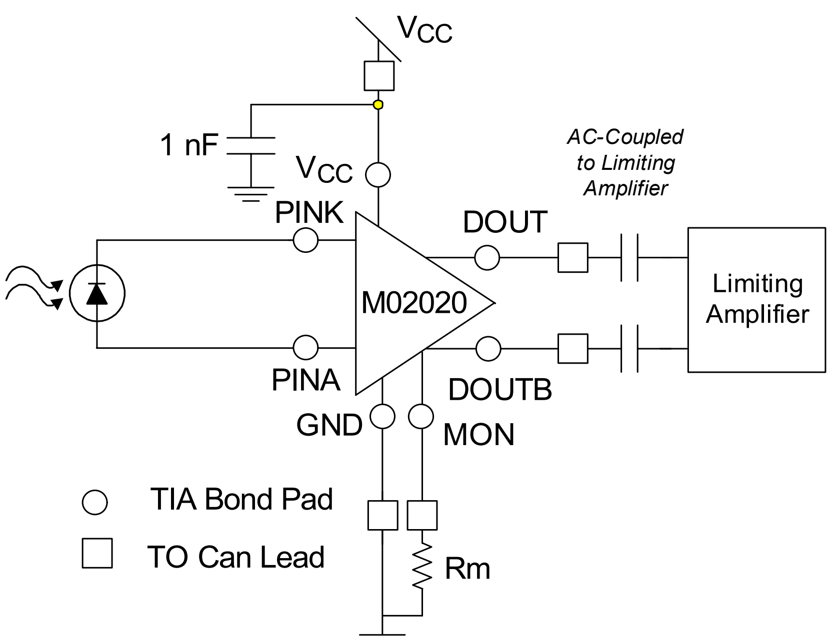
Applications

- Fibre Channel Transceivers (1x, 2x and 4x)
- 4.25 Gbps ROSA
- SFF/SFP Modules
- ATM/SONET
- 4 km and 10 km single-mode links

Features

- Typical -22.8 dBm Sensitivity
- Data rates to 4.25 Gbps
- No filter (PINK) capacitor required
- AGC provides dynamic range of 27 dB
- 3.6 kΩ differential transimpedance
- 4 mA_{PP} overload input current
- Photodiode current monitor
- Internal or external bias for photodiode
- Single +3.3V supply
- Same pad layout and die size as M02011/13/14/15/16/24/26

Typical Applications Diagram



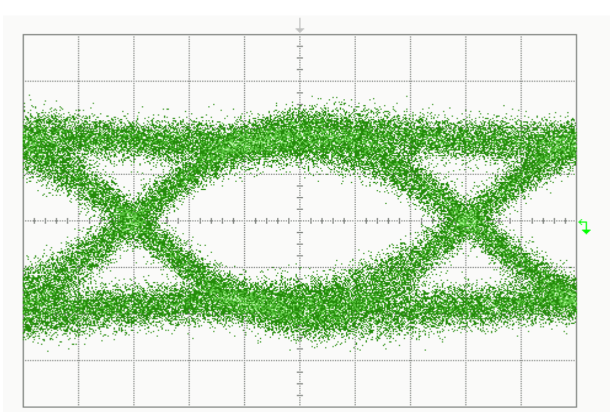
Ordering Information

Part Number	Package	Operating Temperature
M02020-12	Waffle Pack	–40 °C to 95 °C
M02020-22	Sawn Quartered Wafer	–40 °C to 95 °C
M02020-32	Expanded whole wafer on a ring	–40 °C to 95 °C

Revision History

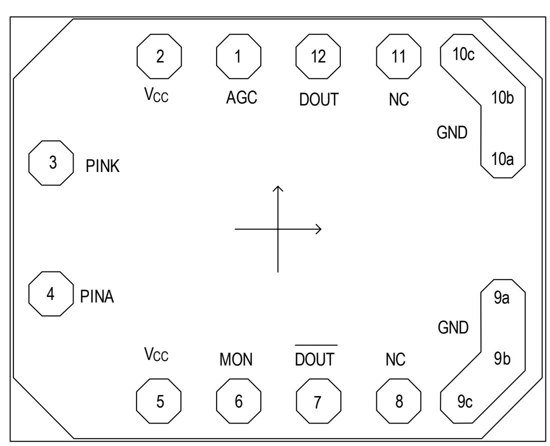
Revision	Level	Date	ASIC Revision	Description
F	Released	October 2007	-12	Update AC specifications (Table 1-4) based on final characterization results. Add description of monitor output in Section 3.2.4. Correct monitor output compliance voltage requirements in Section 4.2.
E	Preliminary	July 2007	-12	Add specific ordering information versus requesting the customer to contact the sales office.
D	Preliminary	June 2007	-12	Add Applications information. Restore Dout and $\overline{\text{Dout}}$ pad information to reflect updated device pad out. Modify specifications based on initial device evaluation.
C	Advance	December 2006	-11	Updated pad location information (pad centers moved 9 μm toward the die edge), update Dout and $\overline{\text{Dout}}$ location. Update Figure 4-1.
B	Advance	November 2006	-11	Update specifications based on final design parameters.
A	Advance	June 2006	-11	Initial release.

Typical Eye Diagram



Eye diagram for 4.25 Gbps at -23 dBm input power

Pad Configuration



Die size ≈ 1090 x 880 μm

1.0 Product Specification

1.1 Description of Key Specifications

1.1.1 Input Referred Noise

In the design of a Transimpedance Amplifier, the primary goal is to minimize the input referred noise of the amplifier. This achieves the best S/N ratio for optimum bit error rate performance of the incoming optical data stream. The noise performance of a TIA is a key specification for meeting the stringent optical sensitivity requirement. In general, the input referred noise calculations for a TIA are identical to those in other conventional amplifiers. The input referred noise can be determined from several methods. Traditionally at Mindspeed, TIA noise is obtained from dividing the output RMS voltage noise of the TIA by the transimpedance. The small signal transimpedance of the TIA can be calculated by applying a known p-p input current and then measuring the p-p differential output voltage. The equations used for I_N (Input Referred Noise) and G_{TIA} (Transimpedance) are shown below. The TIA output RMS noise can be measured conveniently by using a wide band oscilloscope (or by using a power meter and converting the noise power to noise voltage).

$I_N = (Vout_{RMS} / G_{TIA})$

$G_{TIA} = (Vout_{PP} / I\_input_{PP})$, where:

I_N = Input referred noise in RMS

G_{TIA} = TIA small signal transimpedance

I_input_{PP}= p-p input current

1.1.2 Optical Input Sensitivity

TIA input sensitivity can be calculated from the optical sensitivity equation directly based on the input referred noise, photodiode responsivity and transmitter extinction ratio information. Note that the Signal to Noise (S/N) must exceed 14.1 to achieve a system bit error rate (BER) of 1×10^{-12}.

Sensitivity = 10log {((S/N x I_N x (ER + 1)) / (2 x ρ x ER – 1)) x 1000} dBm

Where:

Sensitivity = Input sensitivity expressed in average power

S/N = 14.1(for 10^{-12} BER)

I_N = Input Referred Noise in RMS

ER = Extinction Ratio = 10 (typically)

ρ = Photodiode Responsivity = 0.9 (typically)

1.2 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{CC}	Power supply (V_{CC}-GND)	-0.4 to +4	V
T_A	Operating ambient	-40 to +95	°C
T_{STG}	Storage temperature	-65 to +150	°C
I_{IN}	PINA Input current	8 (1)	mA_{PP}
V_{PINA}, V_{PINK}, V_{Dout}, V_{DoutB}, V_{AGC}, V_{MON}	Maximum input voltage at PINA, PINK, Dout, DoutB, AGC and MON	-0.4V to Vcc +0.4V	V
I_{PINK}	Maximum average current sourced out of PINK	10	mA
I_{Dout}, I_{DoutB}	Maximum average current sourced out of Dout and DoutB	10	mA

NOTES:
1. Equivalent to 4.9 mA average current.

1.3 Recommended Operating Conditions

Table 1-2. Recommended Operating Conditions

	Parameter	Rating	Units
V_{CC}	Power supply (V_{CC} - GND)	3.3 ± 10%	V
C_{PD}	Max. Photodiode capacitance (V_r = 1.7V when using PINK), for 4.3 Gbps data rate	0.5	pF
T_A	Operating ambient temperature	-40 to +95	°C
R_{LOAD}	Recommended differential output loading	100 (1)	Ω

NOTES:
1. 100Ω is the load presented by the post amp.

1.4 DC Characteristics

Table 1-3. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_B	Photodiode bias voltage (PINK - PINA)	1.7	2.0	–	V
V_{CM}	Common mode output voltage	–	1.45	–	V
I_{CC}	Supply current (no loads)	–	44	50	mA

1.5 AC Characteristics

V_{CC} = +3.0V to +3.6V, T_A = -40 °C to +95 °C. Typical values are at T_A = 25 °C, V_{CC} = 3.3V, C_{PD} = 0.5 pF, L_{IN} = 1.0 nH unless otherwise noted (1)

Table 1-4. AC Characteristics

Parameter	Conditions	Minimum	Typical	Maximum	Units
Small Signal Bandwidth	-3dB electrical (Below AGC turn-on, linear gain region)	2.25	3.4	–	GHz
Small Signal Transimpedance	Differential Output (Below AGC turn-on, linear gain region)	2250	3600	4500	Ω
Overload Input Current (2)		2.0	4.0	–	mA_{PP}
Maximum Differential Output Swing	Iin range: 80 μA_{PP} – 4.0 mA_{PP}	150	280	–	mV_{PP}
Input Referred Noise (3)	1.0625 Gbps (800 MHz, Bessel filter)	–	270	380	nA_{RMS}
	2.125 Gbps (1.6 GHz, Bessel filter)	–	375	530	
	4.25 Gbps (3.2 GHz, Bessel filter)	–	550	700	
Duty Cycle Distortion (DCD)	Iin range: from sensitivity to overload	–	5	15	ps_{PP}
Deterministic Jitter (DJ)	Iin range: from sensitivity to overload (Includes DCD)	–	13	30	ps_{PP}
Output Resistance	Differential Output	80	100	120	Ω
AGC Settling Time	To reach 1% of AGC final value within six time constants	–	2.4	–	μs
Low Frequency Cut-off	-3dB electrical, below AGC kick-in	–	17	25	kHz
Photodiode current monitor Offset	No input current	–	0.2	1.0	μA
Photodiode current monitor Accuracy (4)	Iin range: 3 μA_{AVG} – 3.0 mA_{AVG} after offset removed, V_{MON} = 0 – 2.0V	–	0	±1	dB
Photodiode current monitor Gain Ratio	V_{MON} = 0 to 2.0V	–	1:1	–	–
Power Supply Rejection Ratio	DC to 1 MHz	–	30	–	dB
Optical Input Sensitivity (5)	1.0625 Gbps (800 MHz, Bessel filter)	–	-25.9	–	dBm
	2.125 Gbps (1.6 GHz, Bessel filter)	–	-24.5	–	
	4.25 Gbps (3.2 GHz, Bessel filter)	-21.7	-22.8	–	

NOTES:

1. Die parameters are production tested at room temperature only, but are guaranteed by design and characterization to operate over an ambient temperature range (T_A) of -40 °C to +95 °C and V_{CC} range of 3.0 to 3.6V.
2. Overload is the largest p-p input current that the M02020 accepts while meeting specifications.
3. Input Referred Noise is derived by calculation as (RMS output noise) / (Gain at 100 MHz).
4. Includes variation over supply and temperature.
5. Measured by using 10^{-12} BER. Assume transmitter extinction ratio is 10 dB and responsivity of photo diode is 0.9 A/W.

2.0 Pad Definitions

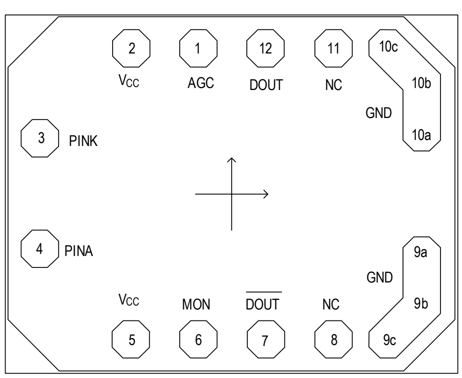
Table 2-1. Pad Descriptions

Die Pad #	Name	Function
1	AGC	Monitor or force AGC voltage.
2	V_{CC}	Power pin. Connect to most positive supply.
3	PINK	Common PIN input. Connect to photo diode cathode.[1]
4	PINA	Active PIN input. Connect to photo diode anode.
5	V_{CC}	Power pin. Connect to most positive supply (only one V_{CC} pad needs to be connected).
6	MON	Analog current source output. Current matched to average photodiode current.
7	$\overline{DOUT}$	Differential data output (goes low as light increases).
8	NC	No Connect. Leave floating.
9	GND	Ground pin. Connect to the most negative supply. [2]
10	GND	Ground pin. Connect to the most negative supply. [2]
11	NC	No Connect. Leave floating.
12	DOUT	Differential data output (goes high as light increases).
NA	Backside	Backside. Connect to the lowest potential, usually ground.

NOTES:

1. Alternatively the photodiode cathode may be connected to a decoupled positive supply, e.g. V_{CC}.
2. All ground pads are common on the die. Only one ground pad needs to be connected to the TO-Can ground. However, connecting more than one ground pad to the TO-Can ground, particularly those across the die from each other can improve performance in noisy environments.

Figure 2-1. Bare Die Layout



3.0 Functional Description

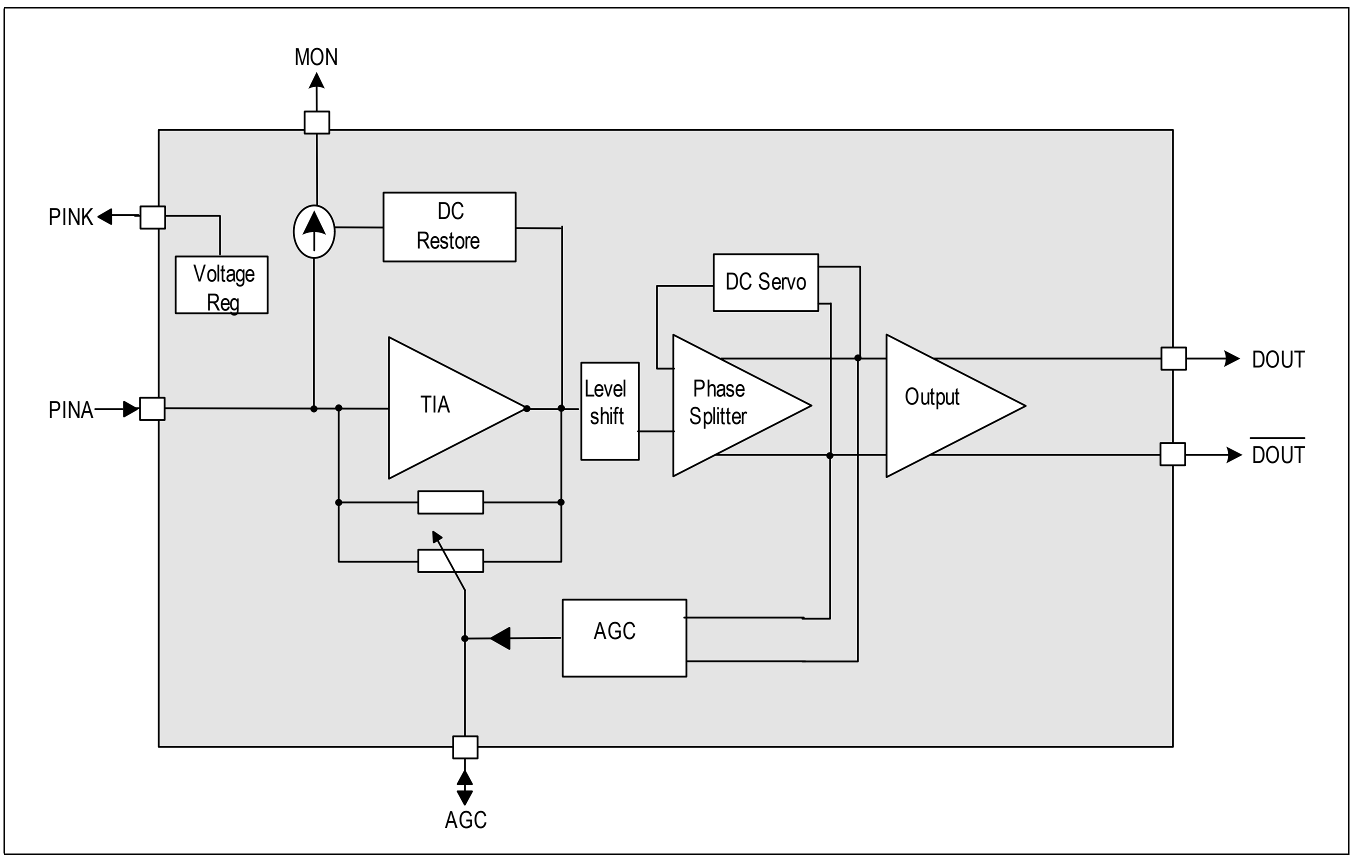
3.1 Overview

The M02020 is a 4G TIA with a wide input dynamic range to support different transmission distance requirements. Input overload of $4mA_{PP}$ is provided to support short-haul Fiber-Optic systems. In addition, input sensitivity of approximately -23 dBm is provided for longer-reach ATM/SONET systems.

In order to satisfy such high sensitivity and good optical overload requirements, automatic gain control circuit (AGC) is implemented in the M02020. The AGC monitors the output amplitude and automatically reduces the TIA gain when the photodiode current exceeds the AGC threshold, maintaining the output at a constant level.

A replica of the average photodiode current is available at the MON pad for photo-alignment and 'Loss of Signal' detecting.

Figure 3-1. M02020 Block Diagram



3.2 General Description

3.2.1 TIA (Transimpedance Amplifier)

The transimpedance amplifier consists of a high gain single-ended CMOS amplifier (TIA) with a feedback resistor. The feedback creates a virtual ground low impedance at the input and virtually all of the input current passes through the feedback resistor defining the voltage at the output. Advanced CMOS design techniques are employed to maintain the stability of this stage across all input conditions.

An on-chip low dropout linear regulator has been incorporated into the design to give excellent noise rejection up to several MHz.

The circuit is designed for PIN photodiodes in the “grounded cathode” configuration, with the anode connected to the input of the TIA and the cathode connected to AC ground, such as the provided PINK terminal. Reverse DC bias is applied to reduce the photodiode capacitance. Avalanche photodiodes can be connected externally to a higher voltage.

3.2.2 AGC

The M02020 has been designed to operate over the input range of +6 dBm to -23 dBm. This represents a ratio of 1:500 whereas the acceptable dynamic range of the output is only 1:30 which implies a compression of 16:1 in the transimpedance. The design uses a MOS transistor operating in the triode region as a “voltage controlled resistor” to achieve the transimpedance variation.

Another feature of the AGC is that it only operates on signals greater than –12.5 dBm (@ 0.9 A/W). This knee in the gain response is important when setting “signal detect” functions in the following post amplifier. It also aids in active photodiode alignment.

The AGC pad allows the AGC to be disabled during photodiode alignment by grounding the pad through a low impedance. The AGC control voltage can be monitored during normal operation at this pad by a high impedance (>10 MΩ) circuit.

3.2.3 Output Stage

The signal from the TIA enters a phase splitter followed by a DC-shift stage and a pair of voltage follower outputs. These are designed to drive a differential (100Ω) load. They are stable for driving capacitive loads such as interstage filters. Since the M02020 exhibits rapid roll-off (3 pole), simple external filtering is sufficient.

3.2.4 Monitor O/P

High impedance output sources a replica average photodiode current for photo-alignment and monitoring purposes. This output is compatible with the DDMI Receive Power Specification (SFF-8472) and Mindspeed’s DDMI controller products. Ensure that the voltage on V_{MON} is in the range of 0 to 2V. Refer to Figure 4-1.

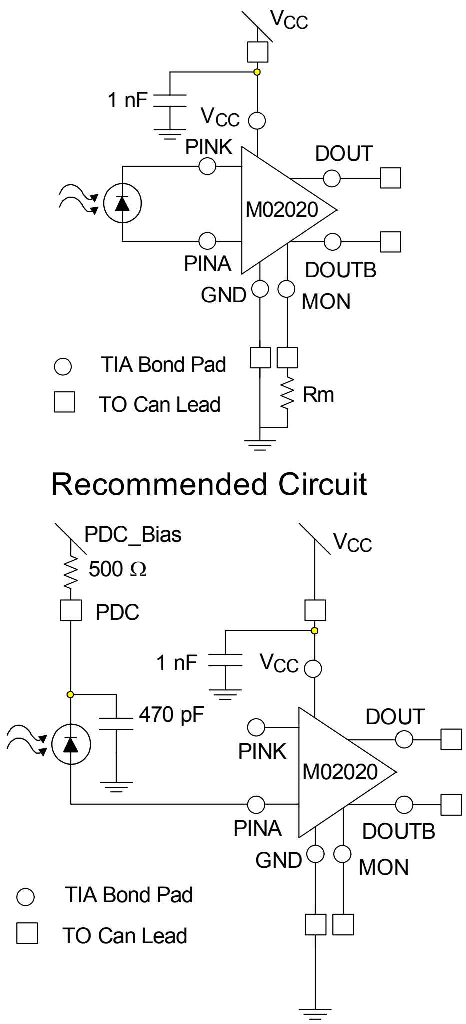
4.0 Applications Information

4.1 Recommended Pin Diode Connections

Figure 4-1. Suggested PIN Diode Connection Methods

Note:

Selection of Rm depends on the maximum input current as detailed in Table 4-1.



Alternative Circuit: External PD/APD Bias

NOTE:

The monitor output is not usable if PINK does not bias the PD.

4.2 Monitor O/P

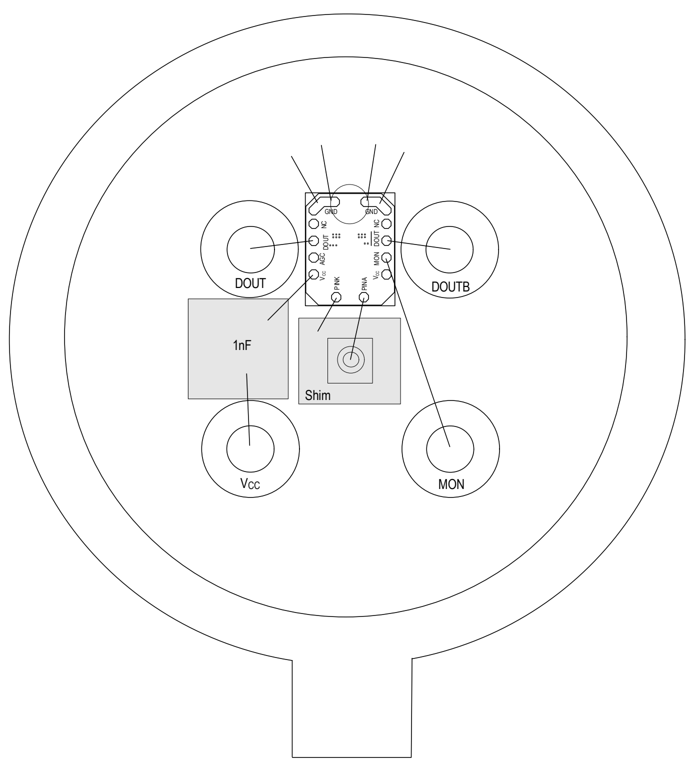
High impedance output sources a replica average photodiode current for photo-alignment use. This output is compatible with the DDMI Receive Power Specification (SFP-8472) and Mindspeed's DDMI controllers. Ensure that the voltage on V_{MON} is in the range of 0 to 2.0V. Refer to Figure 4-1.

Table 4-1. Selection of Rm for Maximum Input Current

I_{IN} Max (mA)	Optical Power (dBm)	Rm (Ω)
4	+6	500
2	+3	1000
1	0	2000
0.5	-3	4000

4.3 TO-Can Layout

Figure 4-2. Typical Layout Diagram with Photodiode Mounted on Submount (5 pin TO-Can)

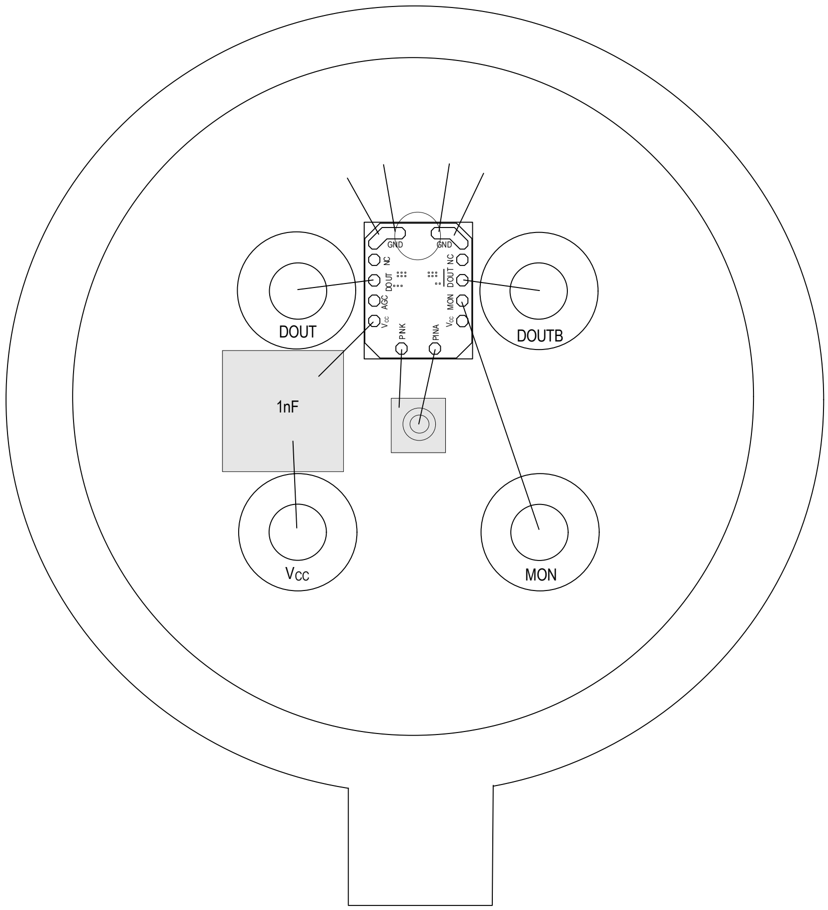


NOTES:

Typical application inside of a 5 lead TO-Can.
It is only necessary to bond one V_{CC} pad and one GND pad. However, bonding both of each ground pads is encouraged for improved performance in noisy environments.

The backside must be connected to the lowest potential, usually ground, with conductive epoxy or a similar die attach material. If a monitor output is not required then a 4 lead TO-Can may be used.

Figure 4-3. Typical Layout Diagram with Photodiode Mounted on TO-Can base (5 pin TO-Can)



NOTES:

Typical application inside of a 5 lead TO-Can.
It is only necessary to bond one V_{CC} pad and one GND pad. However, bonding both of each ground pads is encouraged for improved performance in noisy environments.

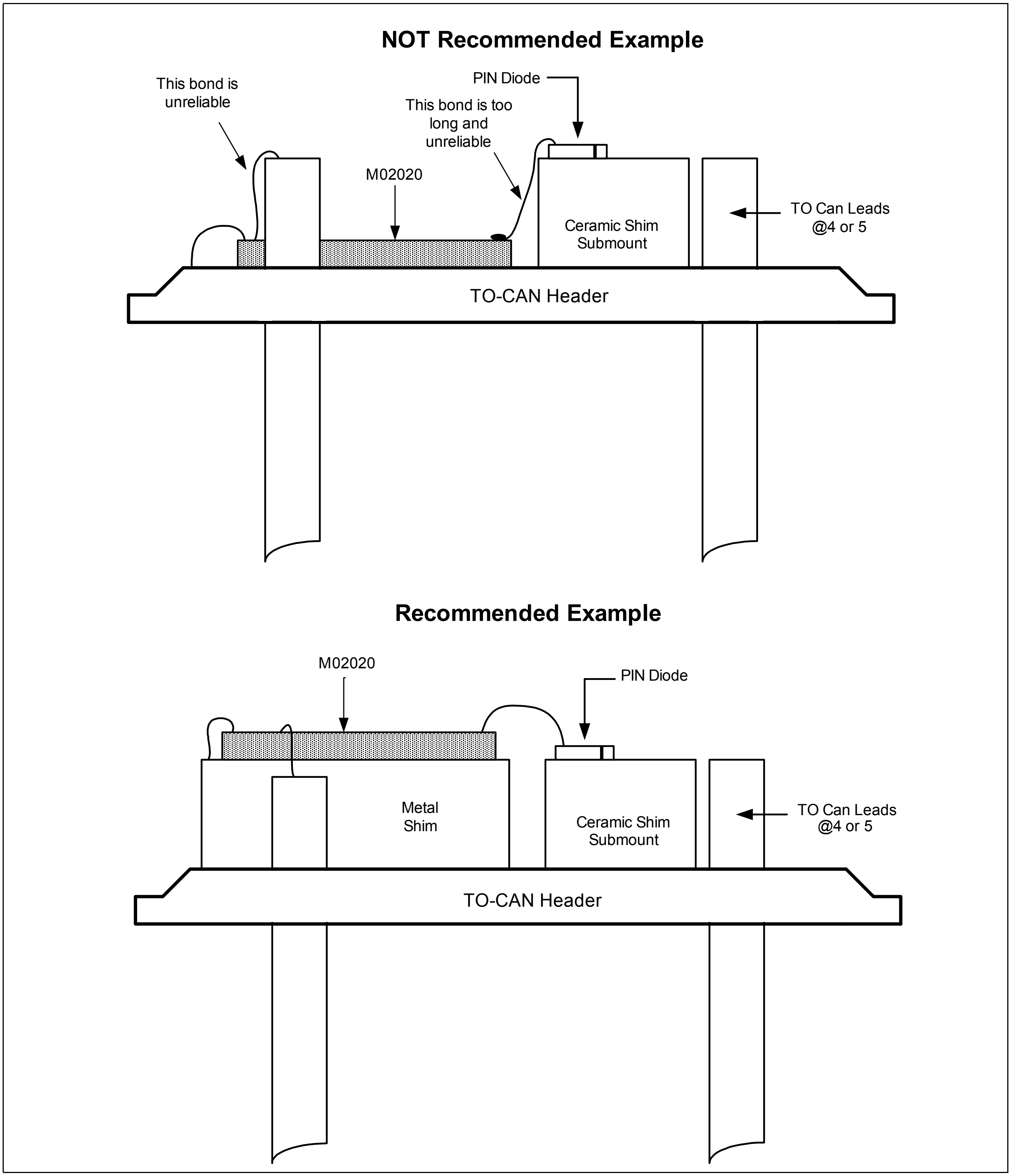
The backside must be connected to the lowest potential, usually ground, with conductive epoxy or a similar die attach material. If a monitor output is not required then a 4 lead TO-Can may be used.

4.4 Treatment of PINK

PINK does not require capacitor bypassing when powering a photo diode or if PINK is not used to bias the photo diode.

4.5 TO-Can Assembly Recommendations

Figure 4-4. TO-Can Assembly Diagram



4.5.1 Assembly

The M02020 is designed to work with a wirebond inductance of 1 nH ± 0.25 nH. Many existing TO-Can configurations will not allow wirebond lengths that short, since the PIN diode submount and the TIA die are more than 1 mm away in the vertical direction, due to the need to have the PIN diode in the correct focal plane. This can be remedied by raising up the TIA die with a conductive metal shim. This will effectively reduce the bond wire length. Refer to Figure 4-4 above for details.

Mindspeed recommends ball bonding with a 1 mil (25.4 µm) gold wire. For performance reasons the PINA pad has less via material connected to it. It therefore requires more care in setting of the bonding parameters. **For the same reason PINA has reduced ESD protection.**

In addition, please refer to the Mindspeed Product Bulletin (document number 0201X-PBD-002). Care must be taken when selecting chip capacitors, since they must have good low ESR characteristics up to 1.0 GHz. It is also important that the termination materials of the capacitor be compatible with the attach method used.

For example, Tin/Lead (Pb/Sn) solder finish capacitors are incompatible with silver-filled epoxies. Palladium/Silver (Pd/Ag) terminations are compatible with silver filled epoxies. Solder can be used only if the substrate thick-film inks are compatible with Pb/Sn solders.

4.5.2 Recommended Assembly Procedures

For ESD protection the following steps are recommended for TO-Can assembly:

a. Ensure good humidity control in the environment (to help minimize ESD).

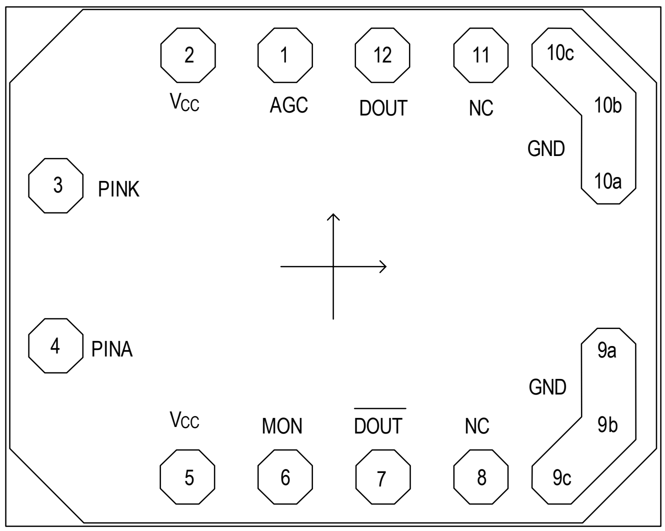
b. Consider using additional ionization of the air (also helps minimize ESD).

c. As a minimum, it is best to ensure that the body of the TO-can header or the ground lead of the header is grounded through the wire-bonding fixture for the following steps. The wire bonder itself should also be grounded.

1. Wire bond the ground pad(s) of the die first.
2. Then wire bond the V_{CC} pad to the TO-Can lead.
3. Then wire bond any other pads going to the TO-Can leads (such as DOUT, $\overline{\text{DOUT}}$ and possibly MON)
4. Next wire bond any capacitors inside the TO-Can.
5. Inside the TO-can, wire bond PINK.
6. The final step is to wire bond PINA.

5.0 Die Specification

Figure 5-1. Bare Die Layout



Pad Number	Pad	X	Y
1	AGC	-76	338
2 (1)	V_{CC}	-228	338
3	PINK	-443	124
4	PINA	-443	-124
5 (1)	V_{CC}	-228	-338
6	MON	-76	-338
7	$\overline{DOUT}$	76	-338
8 (3)	NC	228	-338

Pad Number	Pad	X	Y
9c (1, 2)	GND	375	-338
9b (1, 2)	GND	443	-270
9a (1, 2)	GND	443	-124
10a (1, 2)	GND	443	124
10b (1, 2)	GND	443	270
10c (1, 2)	GND	375	338
11 (3)	NC	228	338
12	DOUT	76	338

NOTES:

1. It is only necessary to bond one V_{CC} pad and one GND pad. However, bonding both GND pads is encouraged for improved performance in noisy environments.
2. Each location is an acceptable bonding location.
3. Leave floating.

Process technology: CMOS, Silicon Nitride passivation
Die thickness: 300 µm
Pad metallization: Aluminum
Die size: 1090 µm x 880 µm
Pad openings: 72 µm sq.
Pad Centers in µm referenced to center of device
Connect backside bias to ground

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