GENERAL DESCRIPTION

The XRK39351 is a low voltage PLL based clock driver designed for high speed clock distribution applications.

The XRK39351 has two reference clock inputs, one LVPECL and the other LVCMOS. The REF_SEL input selects clock input to be used as the PLL's reference source.

The XRK39351 uses PLL technology to frequency lock its outputs to the clock reference input. The divider in the feedback path will determine the frequency of the VCO. The XRK39351 provides 9 LVCMOS outputs that are separated into 4 banks. Each of the separate output banks can individually divide down the VCO output frequency. This allows the XRK39351 to generate a variety of output-to-input frequency ratios (1:1, 1:2, 1:4, 2:1 and 4:1). All outputs provide LVCMOS compatible levels while driving 50Ω terminated transmission lines.

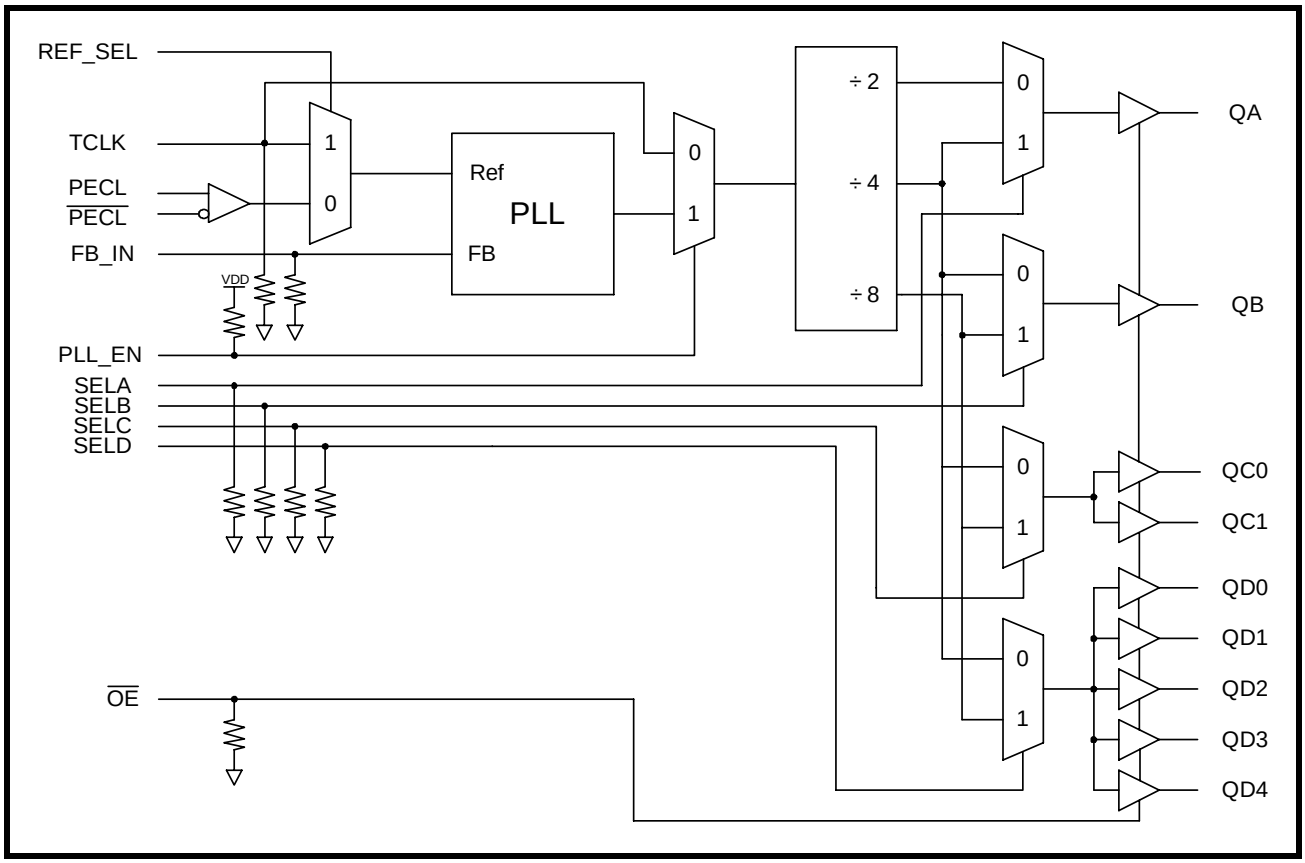
The input reference clock can be directly applied to the output dividers bypassing the PLL when PLL_EN input is pulled low. This is a test mode intended for system debug purposes.

The XRK39351 has an output/input frequency range of 25MHz to 200MHz with the PLL enabled and an input frequency range of 2MHz to 300MHz when the PLL is disabled (test mode).

FEATURES

- 9 LVCMOS Outputs (4 banks)
- 25 - 200 MHz output frequency range
- Fully Integrated PLL
- 2.5V or 3.3V Operation
- Selectable reference clock input, LVCMOS or LVPECL
- 150ps max output to output skew
- Pin compatible with MPC9351
- Industrial temp range: -40°C to +85°C
- 32-Lead TQFP Packaging

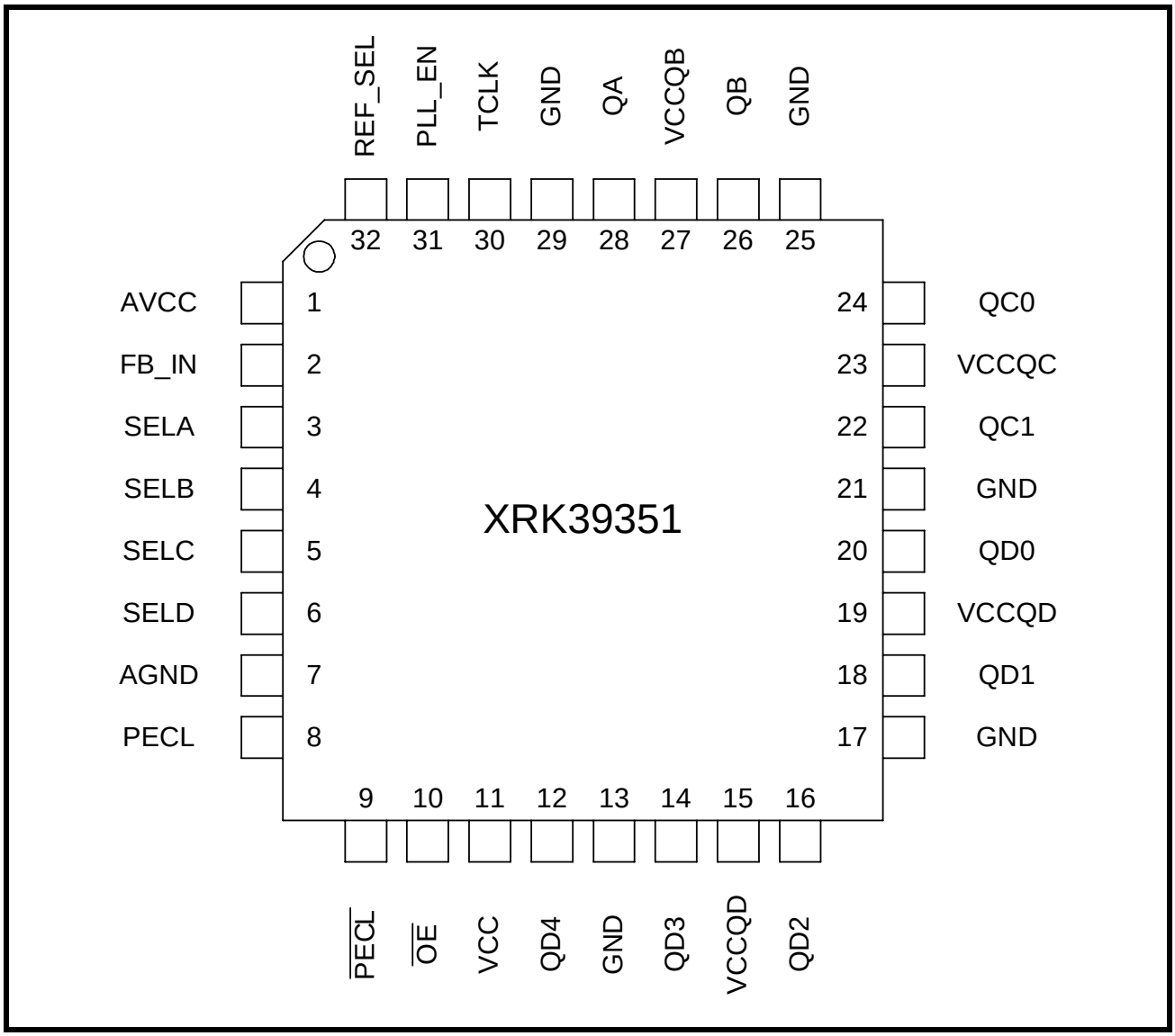
FIGURE 1. BLOCK DIAGRAM OF THE XRK39351



PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRK39351CQ	32-Lead TQFP	0°C to +70°C
XRK39351IQ	32-Lead TQFP	-40°C to +85°C

FIGURE 2. PIN OUT OF THE XRK39351



PIN DESCRIPTIONS

NUMBER	NAME	TYPE		DESCRIPTION
1	AVCC	Power		Power supply for PLL
2	FB_IN	Input	pull-down	External PLL feedback clock input
3	SELA	Input	pull-down	Selects divider value for Bank A output
4	SELB	Input	pull-down	Selects divider value for Bank B output
5	SELC	Input	pull-down	Selects divider value for Bank C outputs
6	SELD	Input	pull-down	Selects divider value for Bank D outputs
7	AGND	Power		PLL ground
8	PECL	Input		LVPECL - pos differential reference clock
9	$\overline{\text{PECL}}$	Input		LVPECL - neg differential reference clock
10	$\overline{\text{OE}}$	Input	pull-down	Output enable/disable and device reset
11	VCC	Power		Power supply for core, inputs and bank A output clock
12, 14, 16, 18, 20	QD[4:0]	Output		Bank D clock outputs
13, 17, 21, 25, 29	GND	Power		Ground
15, 19	VCCQD	Power		Power supply for bank D output clocks
20, 22	QC[1:0]	Output		Bank C clock outputs
23	VCCQC	Power		Power supply for bank C output clocks
26	QB	Output		Bank B clock output
27	VCCQB	Power		Power supply for bank B output clock
28	QA	Output		Bank A clock output
30	TCLK	Input	pull-down	LVCMOS reference clock input
31	PLL_EN	Input	pull-up	Selects PLL or PLL-bypass (test mode) operation
32	REF_SEL	Input	pull-down	Selects primary reference clock source

TABLE 1: CONTROL INPUT FUNCTION TABLE

PIN NAME	0	1	DEFAULT
REF_SEL	PECL clock inputs selected as reference	TCLK input selected as reference	0
PLL_EN	PLL is bypassed. Test Mode. TCLK reference source drives the divider select blocks	PLL enabled. Normal operation. VCO output drives the divider select blocks	1
SELA	Bank A divider = 2	Bank A divider = 4	0
SELB	Bank B divider = 4	Bank B divider = 8	0
SELC	Bank C divider = 4	Bank C divider = 8	0
SELD	Bank D divider = 4	Bank D divider = 8	0
OE	Outputs enabled	Outputs tri-stated, VCO running at minimum frequency	0

DC CHARACTERISTICS (V_{CC}= 3.3 ± 5%, T_A= -40°C TO +85°C)

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNIT	CONDITION
V_{CMR}[a]	PECL Clock inputs common mode range	1.2		V_{CC}-0.9	V	
V_{PP}	PECL Clock peak-to-peak input voltage	500		1000	mV	
V_{IH}	Input voltage high	2.0		VCC+0.3	V	
V_{IL}	Input voltage low			0.8	V	
V_{OH}	Output High Voltage[a]	2.4			V	I_{OH}=-24mA
V_{OL}	Output Low Voltage[a]			0.55 0.30	V V	I_{OL}=24mA I_{OL}=12mA
Z_{OUT}	Output Impedance		14-17		Ω	
I_{IN}	Input leakage current			±150	µA	V_{IN} =V_{CC} or V_{IN} =GND
I_{CC_PLL}	Maximum PLL supply current		3.0	5.0	mA	AV_{CC} pin
I_{CC}	Maximum Quiescent supply current			4	mA	All V_{CCQX} pins
V_{TT}	Output Termination Voltage		V_{CC}÷2		V	

a. VCMR is the cross point of the differential input signal.

AC CHARACTERISTICS (V_{CC}= 3.3 ± 5%, T_A= -40°C TO +85°C) [a]

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT	CONDITION
f_{VCO}	VCO Frequency		200		400	MHz	
f_{ref}	Input Reference Frequency	÷2 feedback	100		200	MHz	PLL_EN = 1
		÷4 feedback	50		100		PLL_EN = 1
		÷8 feedback	25		50		PLL_EN = 1
		PLL Bypass	2		300		PLL_EN = 0
f_{MAX}	Max Output Frequency	÷2 feedback	100		200	MHz	
		÷4 feedback	50		100		
		÷8 feedback	25		50		
t_{ir}/t_{if}	Input Rise/Fall time				1.0	ns	0.8 to 2.0V
f_{refDC}	Input Clock duty cycle		25		75	%	
t_{pd}	Propagation Delay - (SPO, Input clock to FB)						
		TCLK to FB_IN	-50		150	ps	PLL Locked
		PECL to FB_IN	-25		325	ps	PLL Locked
t_{skew}	Output-to-Output Skew				150	ps	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter (RMS)	÷4 feedback		10	22	ps	All outputs set to ÷4
$t_{JIT(PER)}$	Period Jitter (RMS)	÷4 feedback		8	15	ps	All outputs set to ÷4
$t_{JIT(I/O)}$	I/O Phase Jitter (RMS)			4 - 17		ps	
BW	PLL bandwidth	÷2 feedback		9.0-20.0		MHz	
		÷4 feedback		3.0-9.5		MHz	
		÷8 feedback		1.2-2.1		MHz	
DC	Output duty cycle	÷2 feedback	45	50	55	%	100 - 200MHz
		÷4 feedback	47.5	50	52.5	%	50 - 100MHz
		÷8 feedback	48.75	50	51.75	%	25 - 50MHz
t_{LOCK}	Maximum PLL Lock Time				1.0	ms	
t_{or}/t_{of}	Output Rise/Fall time		100		1000	ps	0.55 to 2.4V
$t_{PLZ,HZ}$	Output Disable Time				10	ns	
$t_{PHZ,LZ}$	Output Enable Time				10	ns	

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.

DC CHARACTERISTICS (V_{CC}= 2.5 ± 5%, T_A= -40°C TO +85°C)

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNIT	CONDITION
V_{CMR}[a]	PECL Clock inputs common mode range	1.2		V_{CC}-0.6	V	
V_{PP}	PECL Clock peak-to-peak input voltage	500		1000	mV	
V_{IH}	Input voltage high	1.7		VCC+0.3	V	
V_{IL}	Input voltage low			0.7	V	
V_{OH}	Output High Voltage	1.8			V	I_{OH}=-15mA
V_{OL}	Output Low Voltage			0.6	V	I_{OL}=15mA
Z_{OUT}	Output Impedance		17-20		Ω	
I_{IN}	Input leakage current			±150	µA	V_{IN} =V_{CC} or V_{IN}=GND
I_{CC_PLL}	Maximum PLL supply current		3.0	5.0	mA	AV_{CC} pin
I_{CC}	Maximum Quiescent supply current			1	mA	All V_{CCQX} pins
V_{TT}	Output Termination Voltage		V_{CC}÷2		V	

a. VCMR is the cross point of the differential input signal.

AC CHARACTERISTICS (V_{CC}= 2.5 ± 5%, T_A= -40°C TO +85°C) [a]

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT	CONDITION
f_{VCO}	VCO Frequency		200		400	MHz	
f_{ref}	Input Reference Frequency	÷2 feedback	100		200	MHz	PLL_EN = 1
		÷4 feedback	50		100		PLL_EN = 1
		÷8 feedback	25		50		PLL_EN = 1
		PLL Bypass					PLL_EN = 0
f_{MAX}	Max Output Frequency	÷2 feedback	100		200	MHz	
		÷4 feedback	50		100		
		÷8 feedback	25		50		
t_{ir}/t_{if}	Input Rise/Fall time				1.0	ns	0.7 to 1.7V
f_{refDC}	Input Clock duty cycle		25		75	%	
t_{pd}	Propagation Delay - (SPO, Input clock to FB)						
		TCLK to FB_IN	-100		100	ps	PLL Locked
		PECL to FB_IN	0		300	ps	PLL Locked
t_{skew}	Output-to-Output Skew				150	ps	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter (RMS)	÷4 feedback		10	22	ps	All outputs set to ÷4
$t_{JIT(PER)}$	Period Jitter (RMS)	÷4 feedback		8	15	ps	All outputs set to ÷4
$t_{JIT(I/O)}$	I/O Phase Jitter (RMS)			6 - 25		ps	
BW	PLL bandwidth	÷2 feedback		4.0-15.0		MHz	
		÷4 feedback		2.0-7.0		MHz	
		÷8 feedback		0.7-2.0		MHz	
DC	Output duty cycle	÷2 feedback	45	50	55	%	100 - 200MHz
		÷4 feedback	47.5	50	52.5	%	50 - 100MHz
		÷8 feedback	48.75	50	51.75	%	25 - 50MHz
t_{LOCK}	Maximum PLL Lock Time				1.0	ms	
t_{or}/t_{of}	Output Rise/Fall time		100		1000	ps	0.6 to 1.8V
$t_{PLZ,HZ}$	Output Disable Time				12	ns	
$t_{PHZ,LZ}$	Output Enable Time				12	ns	

a. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.

ABSOLUTE MAXIMUM RATINGS[a]

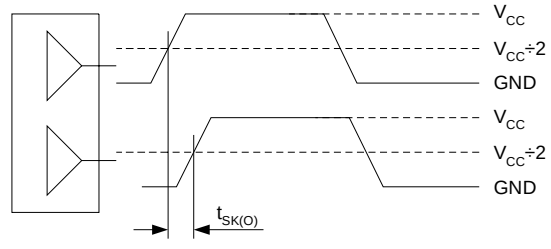
SYMBOL	CHARACTERISTICS	MIN	MAX	UNIT	CONDITION
V_{CC}	Supply Voltage	-0.3	4.6	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	-55	150	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability.

GENERAL SPECIFICATIONS

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNIT	CONDITION
V_{TT}	Output termination voltage		V_{CC}÷2		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
LU	Latch-up immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	Thermal resistance junction to ambient JESD 51-3, single layer test board JESD 51-6, multi layer test board			 62.0 47	 °C/W °C/W	Natural convection
θ_{JC}	Thermal resistance junction to case			14	°C/W	
	Operating junction temperature			115	°C	

FIGURE 3. OUTPUT-TO-OUTPUT SKEW $t_{SK(O)}$



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device.

FIGURE 4. PROPOGATION DELAY ($t_{(Ø)}$, STATIC PHASE OFFSET) TEST REFERENCE

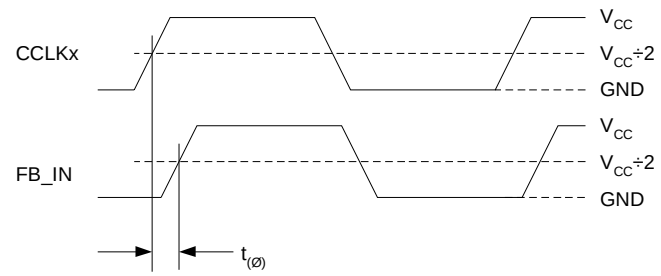
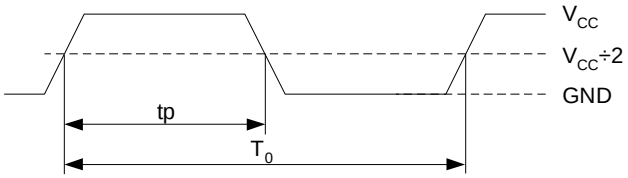


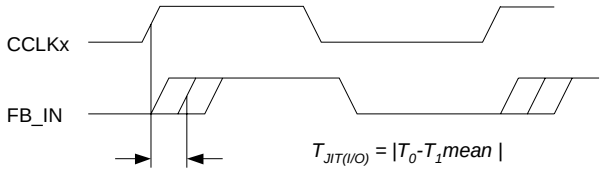
FIGURE 5. OUTPUT DUTY CYCLE (DC)



$DC=t_P/T_0 \times 100\%$

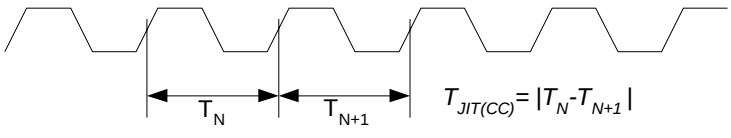
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

FIGURE 6. I/O JITTER



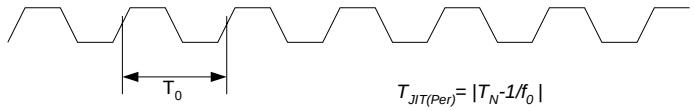
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

FIGURE 7. CYCLE-TO-CYCLE JITTER



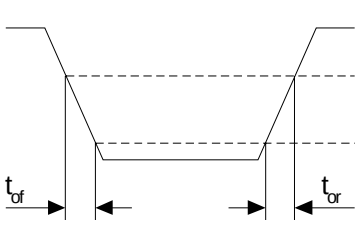
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

FIGURE 8. PERIOD JITTER



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

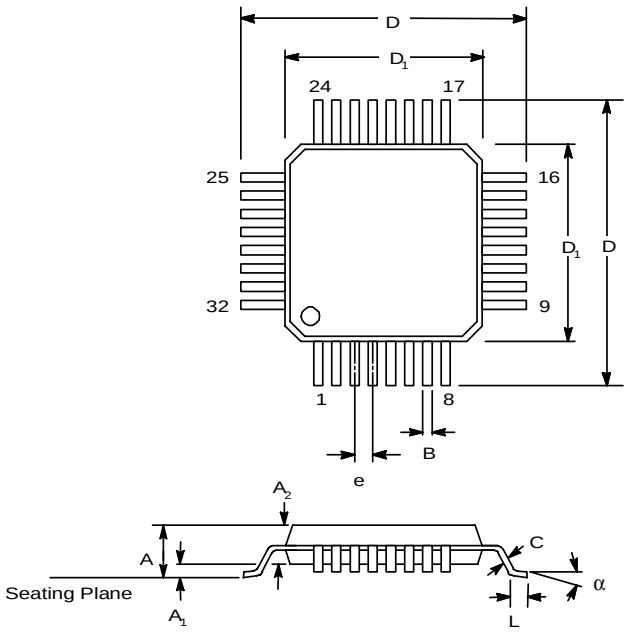
FIGURE 9. OUTPUT TRANSITION TIME TEST REFERENCE



V_{CC}=3.3V	V_{CC}=2.5V
2.4V	1.8V
0.55V	0.6V

PACKAGE DIMENSIONS

32 LEAD THIN QUAD FLAT PACK
(7 x 7 x 1.4 mm TQFP)
rev. 2.00



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.012	0.018	0.30	0.45
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.0315 BSC		0.80 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
1.0.0	November 2006	Initial *FINAL* release.

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