

## **IRS21858SPBF** High(Dual Mode) Side Driver

### Features

- High side programmable ramp gate drive
- High side generic gate driver integrated using the same high side output pin
- Additional high side generic gate driver
- Under voltage lockout for VCC & VBS
- 5V input logic compatible
- Tolerant to negative transient voltage on VS
- RoHS compliant

### Product Summary

Topology	PDP
$V_{\text{OFFSET}}$	$\leq 600 \text{ V}$
$I_{\text{o+}}$ & $I_{\text{o-}}$ (typical)	290mA & 600mA
$t_{\text{ON}}$ & $t_{\text{OFF}}$ (typical)	160ns & 160ns

### Package Options

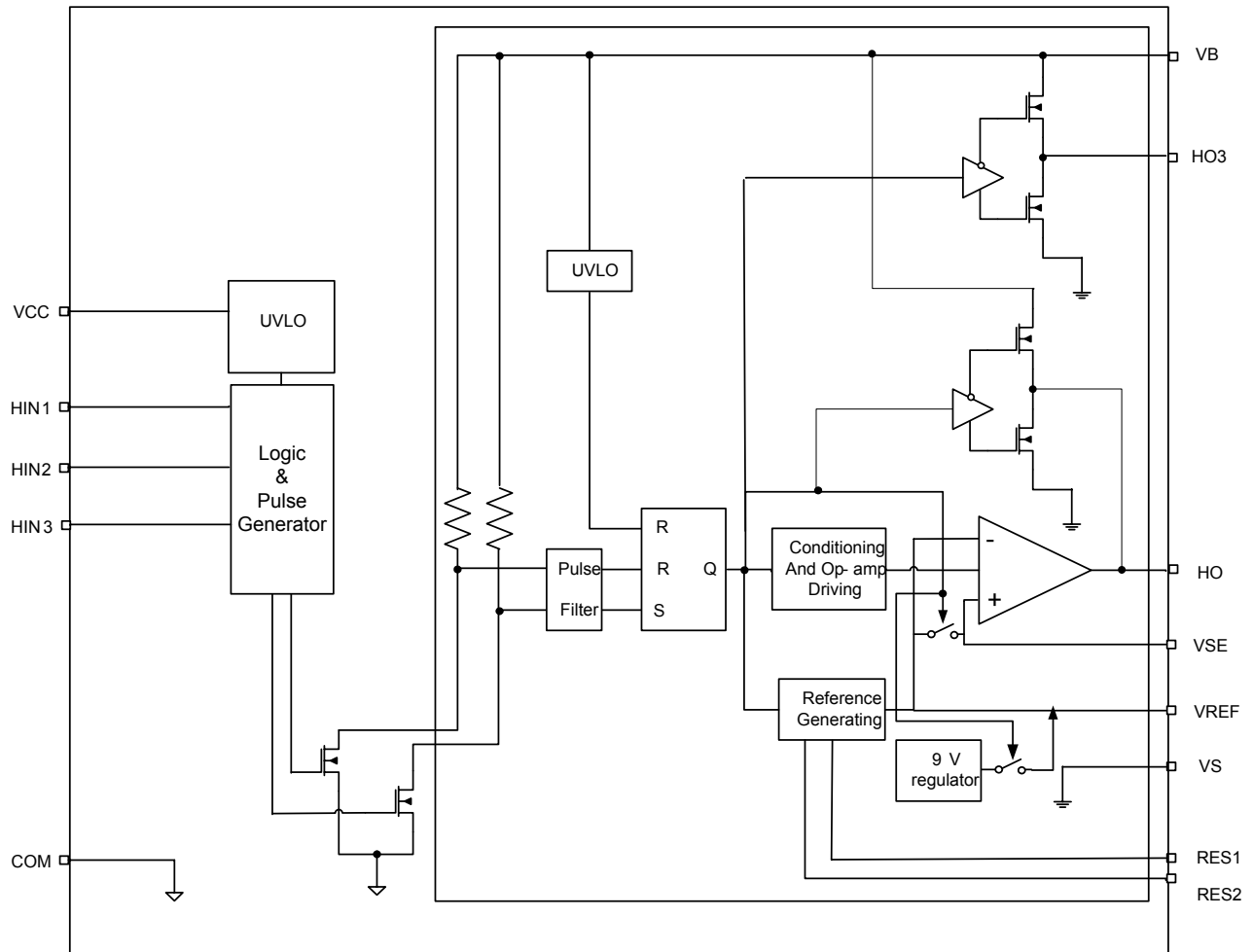


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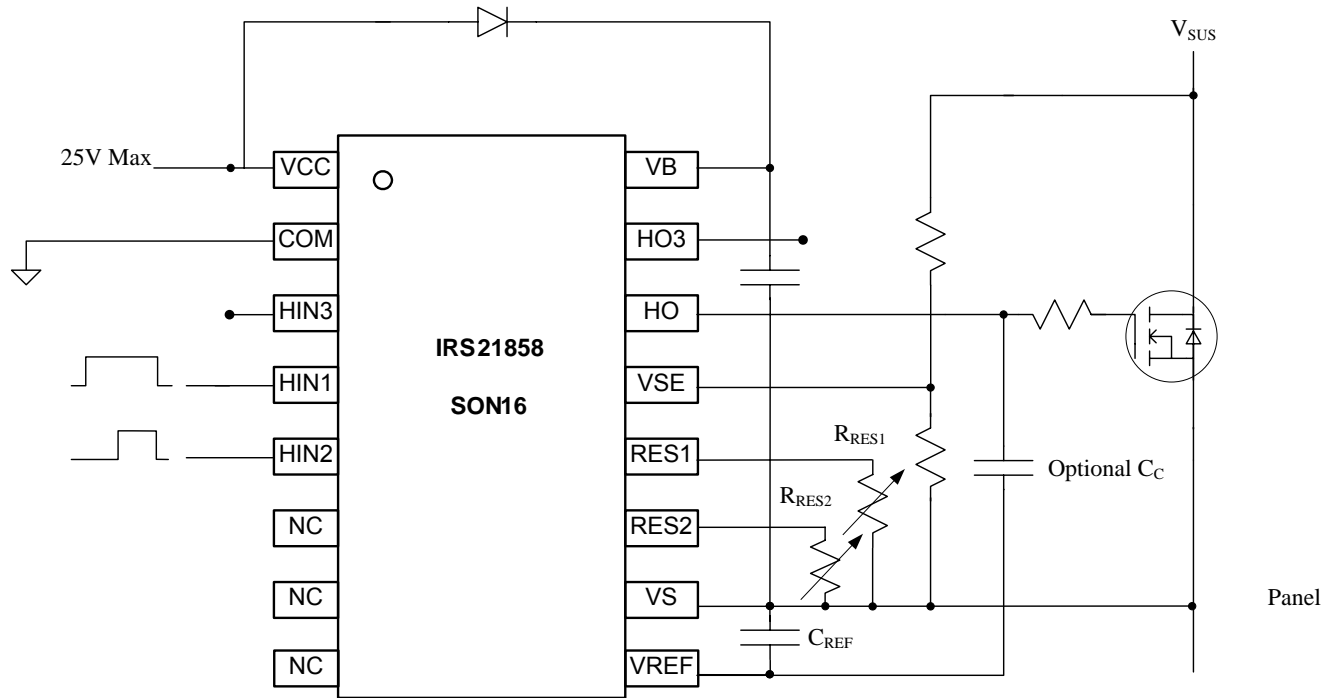
## **Description**

The IRS21858 is high voltage and programmable ramp slope control gate driver for MOSFET and IGBT with single high side dual mode driver and additional generic gate driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with 5V standard CMOS or LSTTL output. The output driver features a programmable slope control by external R and input signal. The floating channels can be used to drive an N-channel power MOSFET or IGBT in the high side configuration, which operates up to 600 volts above the COM ground.

**Simplified Block Diagram**



**Typical Connection Diagrams**



**Linear Ramp driver's connection diagram (Dual slope)**

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>		Industrial <sup>††</sup>
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.
<b>Moisture Sensitivity Level</b>		MSL2 <sup>†††</sup> 260°C (per IPC/JEDEC J-STD-020)
<b>ESD</b>	Machine Model	Class B (per JEDEC standard JESD22-A115)
	Human Body Model	Class 2 (per EIA/JEDEC standard EIA/JESD22-A114)
<b>IC Latch-Up Test</b>		Class I , Level A (per JESD78)
<b>RoHS Compliant</b>		Yes

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

### Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM.

Symbol	Definition	Min	Max	Units
$V_{CC}$	Low side supply voltage	-0.3	25	V
$V_{IN}$	Logic input voltage (HIN1, HIN2, HIN3)	COM-0.3	VCC +0.3	V
$V_{VSE},$ $V_{VREF}$	High side inputs voltage	VS-0.3	VB+0.3	V
$V_{RES1},$ $V_{RES2}$	High side inputs voltage	VS-0.3	VB+0.3	V
$V_B$	High side floating well supply voltage	-0.3	625	V
$V_S$	High side floating well supply return voltage	VB-25	VB+0.3	V
$V_{HO}$	Floating gate drive output voltage	VS-0.3	VB+0.3	V
$V_{HO3}$	Floating gate drive output voltage	VS-0.3	VB+0.3	V
$dV_S/dt$	Allowable VS offset supply transient relative to COM	-	50	V/ns
$P_D$	Package Power Dissipation @ $T_A \leq +25^\circ\text{C}$	-	1.0	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	-	120	$^\circ\text{C}/\text{W}$
$T_J$	Junction Temperature	-55	150	$^\circ\text{C}$
$T_S$	Storage Temperature	-55	150	$^\circ\text{C}$
$T_L$	Lead temperature (Soldering, 10 seconds)	-	300	$^\circ\text{C}$

### Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The offset rating are tested with supplies of  $(V_{CC}-COM) = (V_B - V_S) = 15\text{V}$ .

Symbol	Definition	Min	Max	Units
$V_{CC}$	Low side supply voltage	10	20	V
$V_{IN}$	HIN1, HIN2, LIN3 input voltage	COM	$V_{CC}$	V
$V_{HO3}$	High side gate drive output voltage	$V_S$	$V_B$	V
$V_B$	High side floating well supply voltage	$V_S+10$	$V_S+20$	V
$V_{RES1,RES2}$	RES input voltage	$V_S$	$V_B$	V
$V_{VREF, VSE}$	VREF and VSE input voltage	$V_S$	$V_B - 3$	V
$V_S$	High side floating well supply offset voltage	Note2	600	V
$V_{HO}$	Floating gate drive output voltage	$V_S$	$V_B$	V
$R_{RES1}$	RES1 resistor	50	300	$\text{k}\Omega$
$R_{RES2}$	RES2 resistor	2.5	300	$\text{k}\Omega$
$T_A$	Ambient Temperature	-40	125	$^\circ\text{C}$

†  $V_S$  and  $V_B$  voltages will be tolerant to short negative transient spikes. These will be defined and specified in the future.

†† Logic operation for  $V_S$  of -5 to 600V. Logic state held for  $V_S$  of -5V to  $-V_{BS}$ . (Please refer to Design Tip DT97-3 for more details).

**Static Electrical Characteristics (All values are target data)**

(VCC-COM) = (VB-VS)=15V. TA = 25°C. The VIN, VIN TH and IIN parameters are referenced to COM. The Vo and Io parameters are referenced to VS and are applicable to the respective output leads HO, HO3. The VCCUV parameters are referenced to COM. The VBSUV parameters are referenced to VS.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
VCCUV+	VCC supply undervoltage positive going threshold	8.0	8.9	9.8	V	
VCCUV-	VCC supply undervoltage negative going threshold	7.4	8.2	9.0		
VBSUV+	VBS supply undervoltage positive going threshold	8.0	8.9	9.8		
VBSUV-	VBS supply undervoltage negative going threshold	7.4	8.2	9.0		
ILK	High side floating well offset supply leakage current	---	---	50	μA	VB = VS = 600V
IQBS	Quiescent VBS supply current	---	2.5	3.75	mA	IN1, 2 = 5V
		---	1.45	2.2		IN1, 2 = 0V
IQCC	Quiescent VCC supply current	---	120	250	μA	IN1,2,3 = 0V or 5V
VIH	Logic "1" input voltage	3.5	---	---	V	
VIL	Logic "0" input voltage	---	---	0.8		
IIN+	Logic "1" input bias current	---	10	---	μA	VIN =5V
IIN -	Logic "0" input bias current	---	0	---		VIN =0V
Io+ <sub>HO,HO3</sub>	Output high short circuit pulsed current	---	290	---	mA	Vo=15V, VIN=5V, PW<=10us
Io- <sub>HO,HO3</sub>	Output low short circuit pulsed current	---	600	---		Vo=0V, VIN=0V, PW<=10us
VOL <sub>HO, HO3</sub>	Low level output voltage	---	30	110	mV	Io=2mA
VOH <sub>HO, HO3</sub>	High level output voltage, Vbias-Vo	---	50	130	mV	Io=2mA

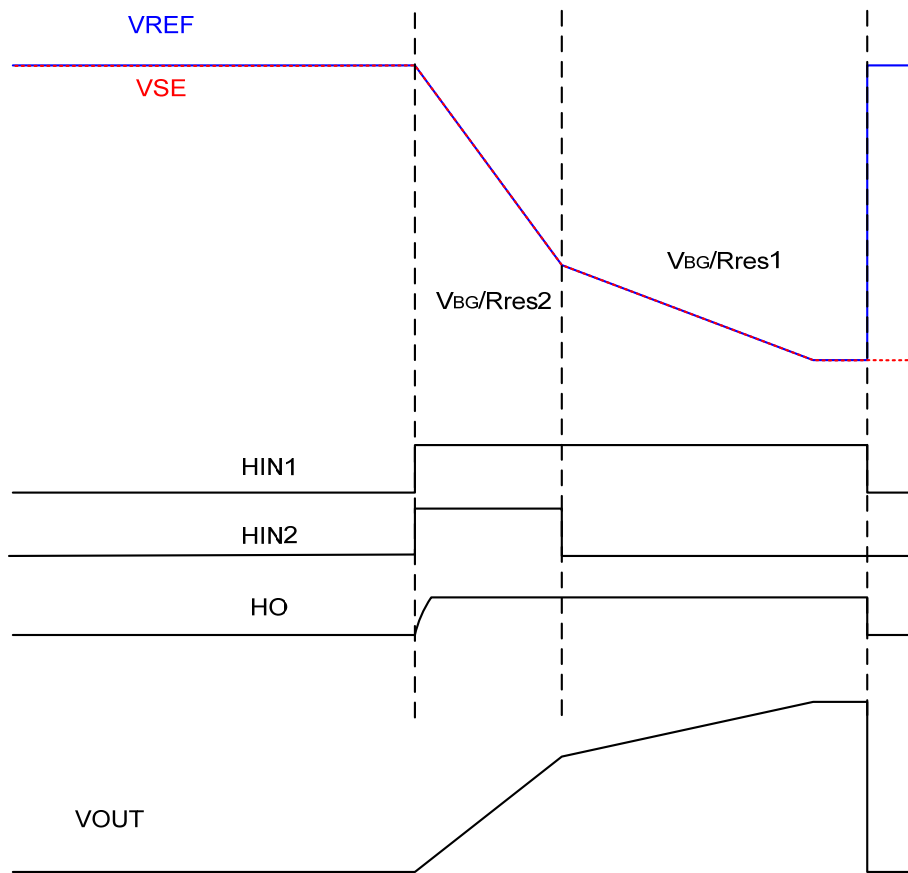


**Dynamic Electrical Characteristics (All values are target data)**

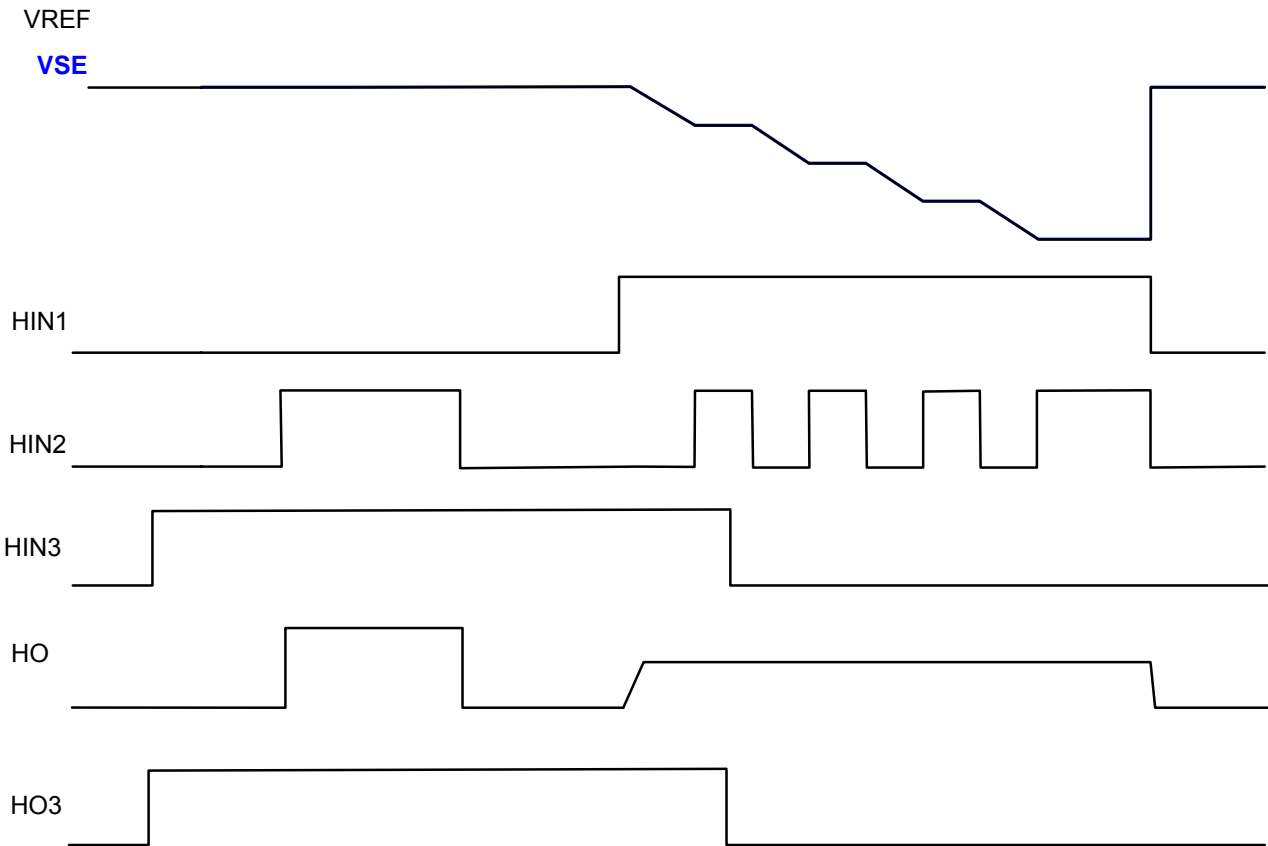
(VCC-COM)=(VB-VS)=15V. TA = 25°C. CL = 1000pF unless otherwise specified. All parameters are reference to COM.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
<b>Internal Operational Amplifier Characteristics</b>						
t <sub>ref_in_ramp1</sub>	Vref Falling time of Linear ramp reference 9V to 2V	---	277.8	---	μs	GBD* C <sub>REF</sub> =1nF, V <sub>SE</sub> open, R <sub>RES1</sub> =100K, HIN1=5V, HIN2=com
t <sub>ref_in_ramp2</sub>	Vref Falling time of Linear ramp reference 9V to 2V	---	14	---	μs	GBD* C <sub>REF</sub> =1nF, V <sub>SE</sub> open, R <sub>RES2</sub> =4.99K, HIN1=5V, HIN2=5V
I <sub>ref_in_ramp1</sub>	Vref DC current of Linear ramp reference at 5V	22.68	25.2	27.72	uA	C <sub>REF</sub> =1nF, V <sub>SE</sub> open, R <sub>RES1</sub> =100K, HIN1=5V, HIN2=com
I <sub>ref_in_ramp2</sub>	Vref DC current of Linear ramp reference at 5V	450	500	550	uA	C <sub>REF</sub> =1nF, V <sub>SE</sub> open, R <sub>RES2</sub> =4.99K, HIN1=5V, HIN2=5V
Gm	OTA transconductance	---	12	---	mS	CL_HO=1nF, R <sub>RES1,2</sub> open
G <sub>open loop</sub>	Open loop gain	45	60	---	dB	Cc =1nF, R <sub>RES1,2</sub> open
BW <sub>SS</sub>	Small signal bandwidth	---	3.5	---	MHz	Cc =1nF, R <sub>RES1,2</sub> open
V <sub>OS</sub>	Input offset voltage	---	20	---	mV	R <sub>RES1,2</sub> open
HO <sub>SR+</sub>	Output positive slew rate	---	4.5	---	V/μs	CL_HO=1nF, R <sub>RES1,2</sub> open
CMRR	Common mode rejection ratio	50	65	---	dB	R <sub>RES1,2</sub> open
PSRR	Power supply rejection ratio	50	65	---	dB	R <sub>RES1,2</sub> open
<b>Propagation Delay Characteristics</b>						
t <sub>on</sub>	Turn-on delay (HO, HO3)	---	160	260	ns	Gate Drive Mode CL =1nF
t <sub>off</sub>	Turn-off delay (HO, HO3)	---	160	260		
t <sub>r</sub>	Turn-on rise from 10% to 90%	---	60	110		
t <sub>f</sub>	Turn-off fall from 90% to 10%	---	20	50		
MT	Delay matching, HO & HO3 turn-on/off			50		

GBD\*: Guaranteed by design



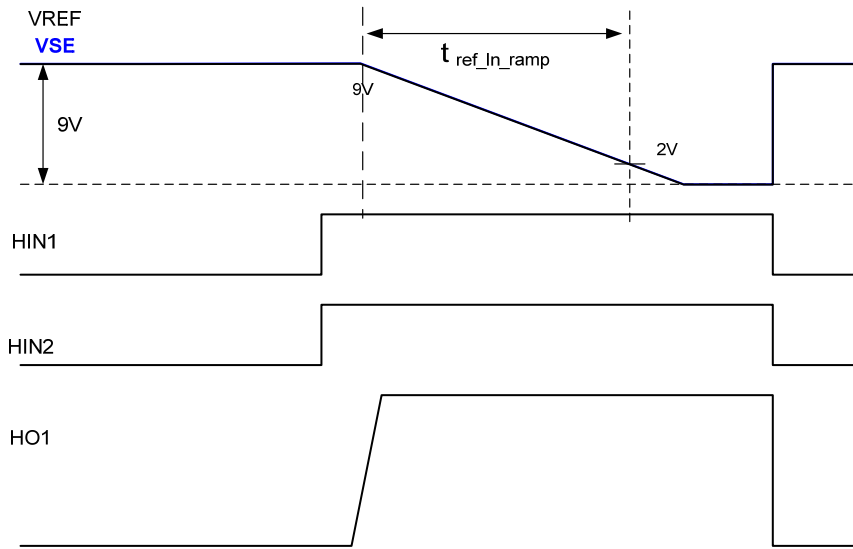
**Figure 1A Input/Output Timing Diagram: Linear Ramp (Dual slope)**



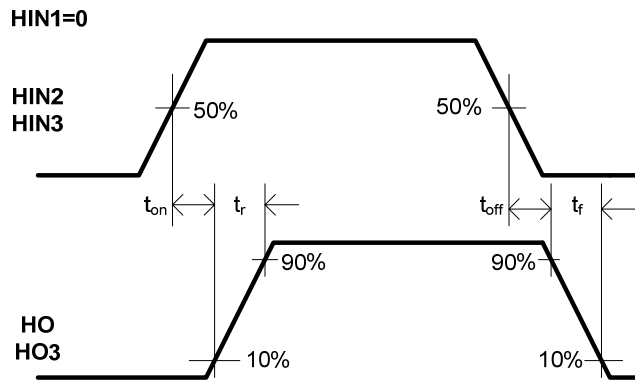
**Figure 1B Input/Output Timing Diagram : HO/HO3 outputs**

**Logic Truth Table**

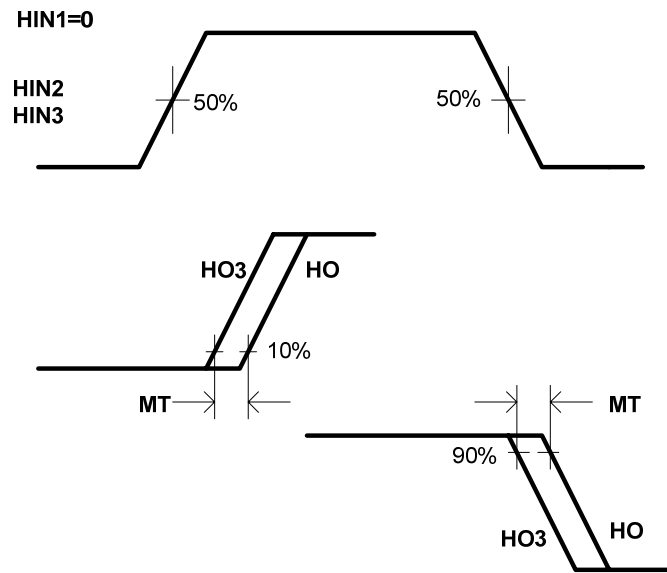
HIN1	HIN2	HIN3	OTA of HO	Gate driver of HO	Gate driver of HO3
0	0	0	High impedance (HIZ)	0	0
0	0	1	High impedance (HIZ)	0	1
0	1	0	High impedance (HIZ)	1	0
0	1	1	High impedance (HIZ)	1	1
1	0	0	Linear ramp rate controlled by RES1	High impedance (HIZ)	0
1	0	1	Linear ramp rate controlled by RES1	High impedance (HIZ)	1
1	1	0	Linear ramp rate controlled by RES2	High impedance (HIZ)	0
1	1	1	Linear ramp rate controlled by RES2	High impedance (HIZ)	1
1	Step(0/1)	1 or 0	Stepwise linear (Dual slope)	High impedance (HIZ)	1 or 0



**Figure 2 Timing Definitions of  $V_{REF}$**

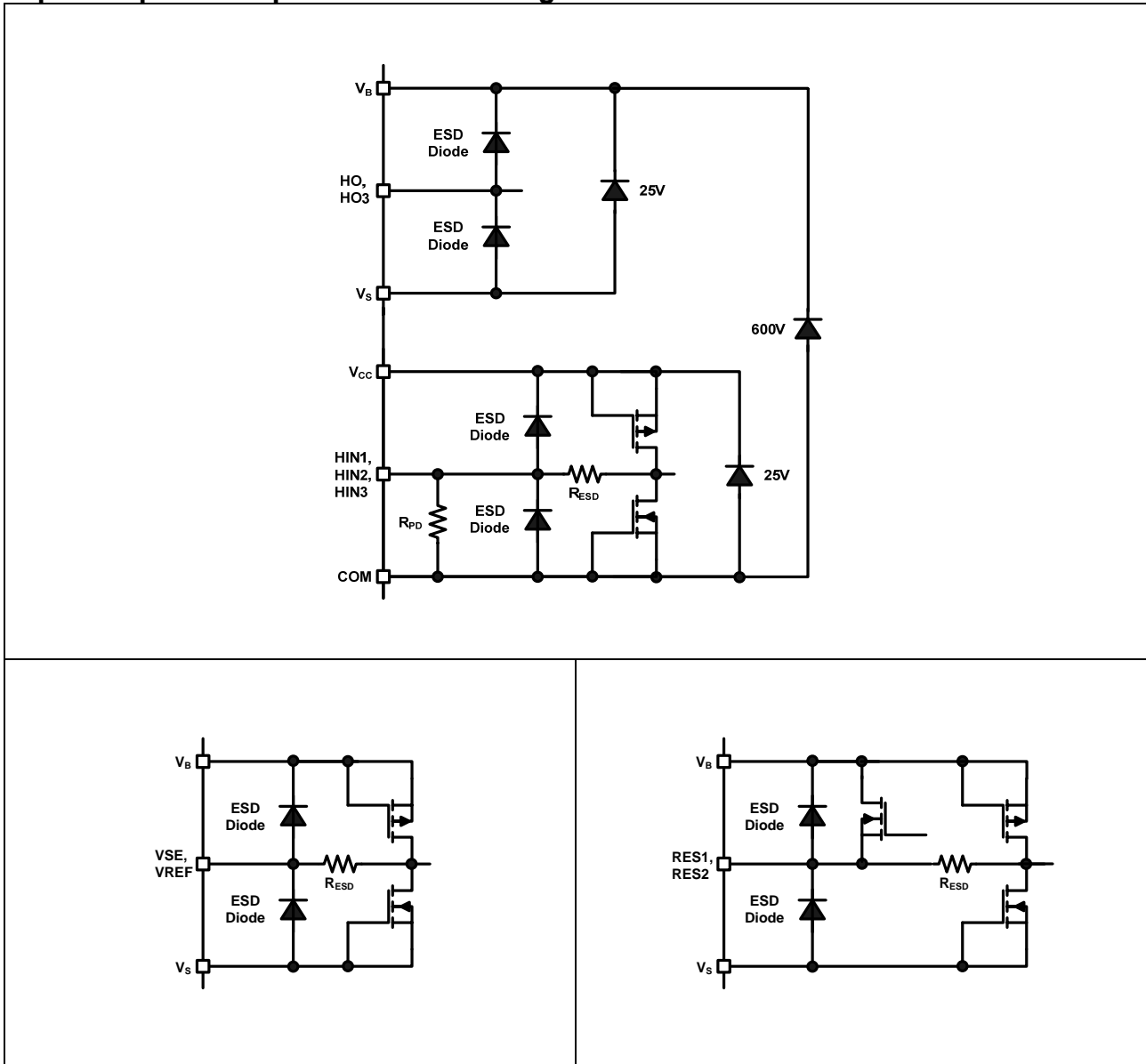


**Figure 3 Switching Time Waveform Definitions of  $HO$  and  $HO3$**



**Figure 4 Delay Matching Waveform Definitions**

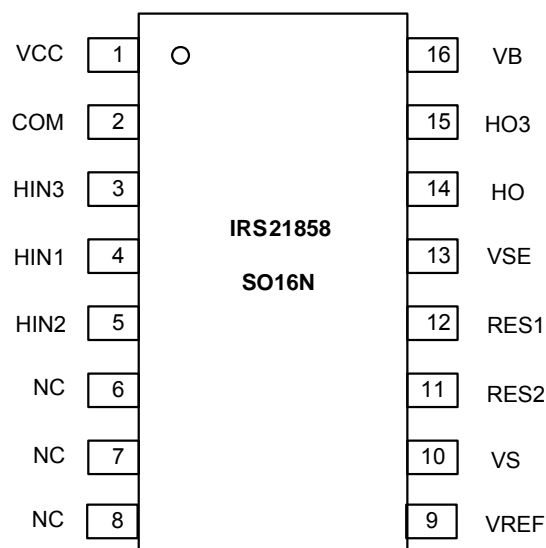
**Input/Output Pin Equivalent Circuit Diagrams**



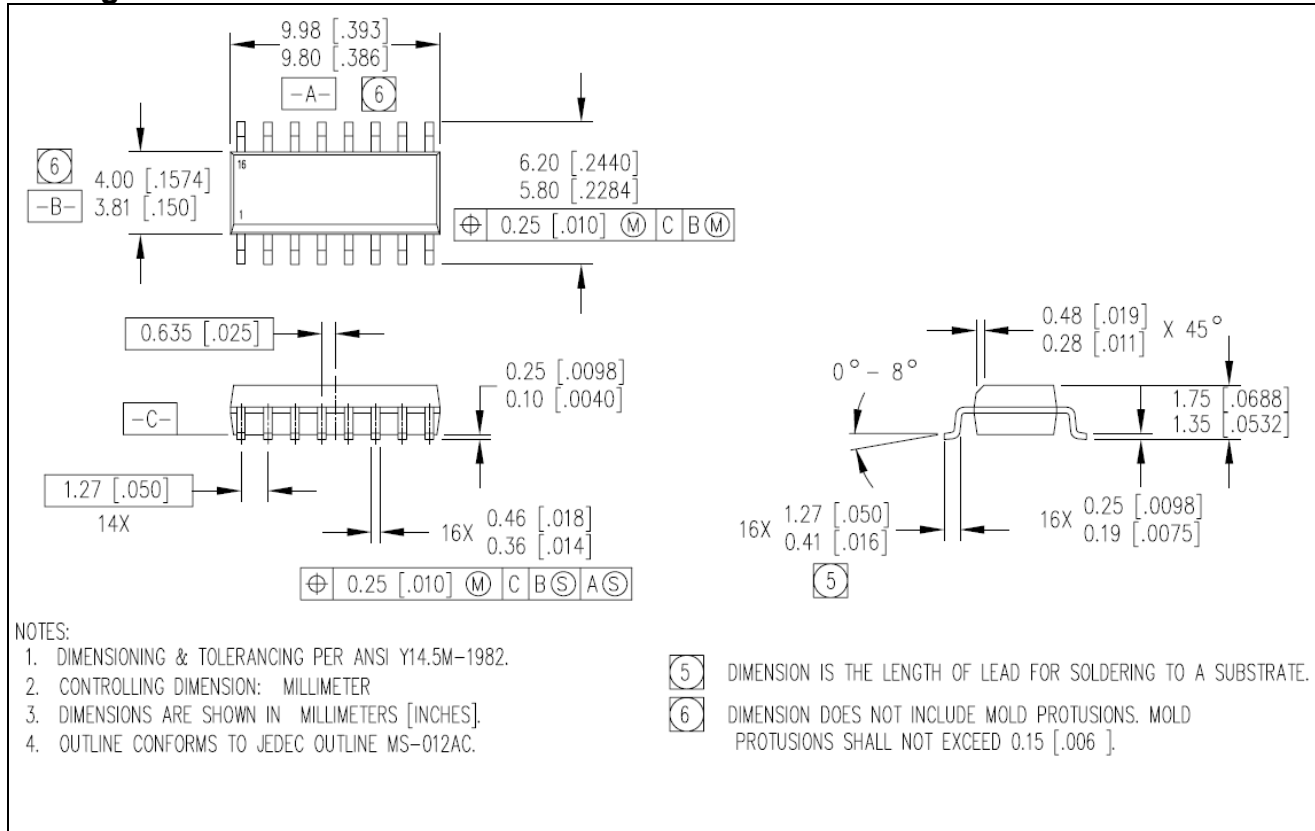
**Lead Definitions**

<b>PIN#</b>	<b>Symbol</b>	<b>Description</b>
1	VCC	Low side supply voltage
2	COM	Low side supply return
3	HIN3	Logic input for high side gate driver output
4	HIN1	Logic input for HO ramp reference control
5	HIN2	Logic input for high side gate driver outputs, in phase
6	NC	No Connection
7	NC	No Connection
8	NC	No Connection
9	VREF	External programmable R/C input for ramp generation
10	VS	High side gate drive floating supply return
11	RES1	Adjustable current source resistor input
12	RES2	Adjustable current source resistor input
13	VSE	Voltage sense input
14	HO	High side gate driver output
15	HO3	High side gate driver output
16	VB	High side gate drive floating supply

**Lead Assignments**



**Package Details: SOIC16N**



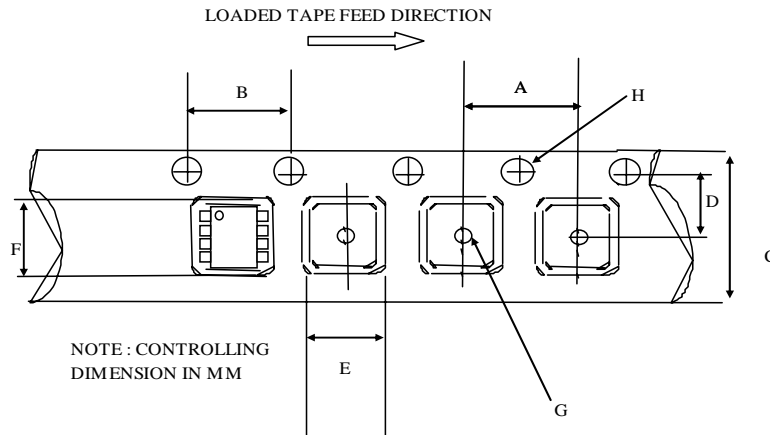
**NOTES:**

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AC.

- 5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
- 6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

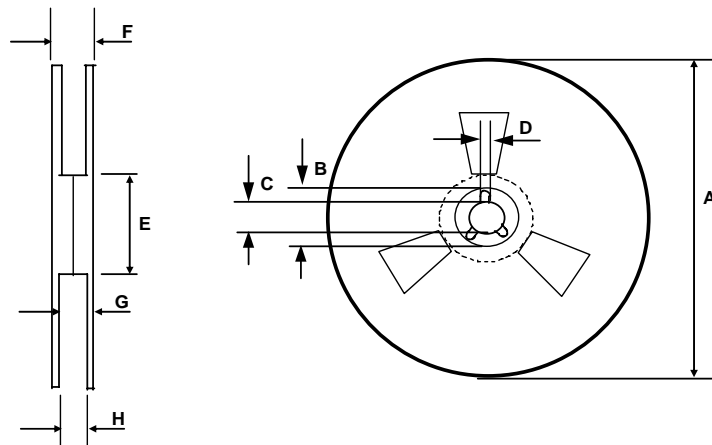


**Tape and Reel Details: SOIC16N**



**CARRIER TAPE DIMENSION FOR 16SOICN**

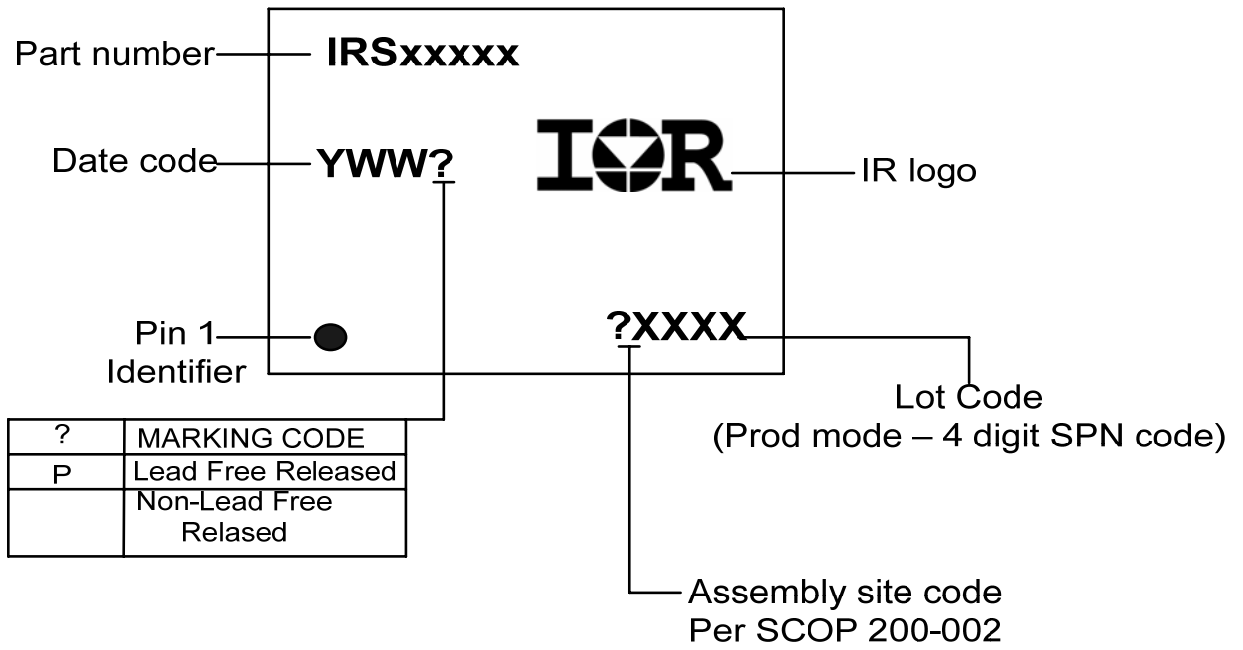
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	10.20	10.40	0.402	0.409
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



**REEL DIMENSIONS FOR 16SOICN**

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

**Part Marking Information**



**Ordering Information**

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS21858S	SOIC16N	Tube/Bulk	45	IRS21858SPBF
		Tape and Reel	2500	IRS21858STRPBF

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