

IRF644, IRF645, IRF646, IRF647, RF1S644, RF1S644SM

13A and 14A, 250V and 275V, 0.28 and 0.34 Ohm,
N-Channel Power MOSFETs

January 1998

Features

- 13A and 14A, 250V and 275V
- $r_{DS(ON)} = 0.28\Omega$ and 0.34Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 275/250VDC Rating-120VAC Line System Operation
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRF644	TO-220AB	IRF644
IRF645	TO-220ABs	IRF645
IRF646	TO-220AB	IRF646 </td
IRF647	TO-220AB	IRF647
RF1S644	TO-262AA	RF1S644
RF1S644SM	TO-263AB	RF1S644

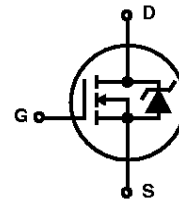
NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in the tape and reel, i.e., RF1S644SM9A.

Description

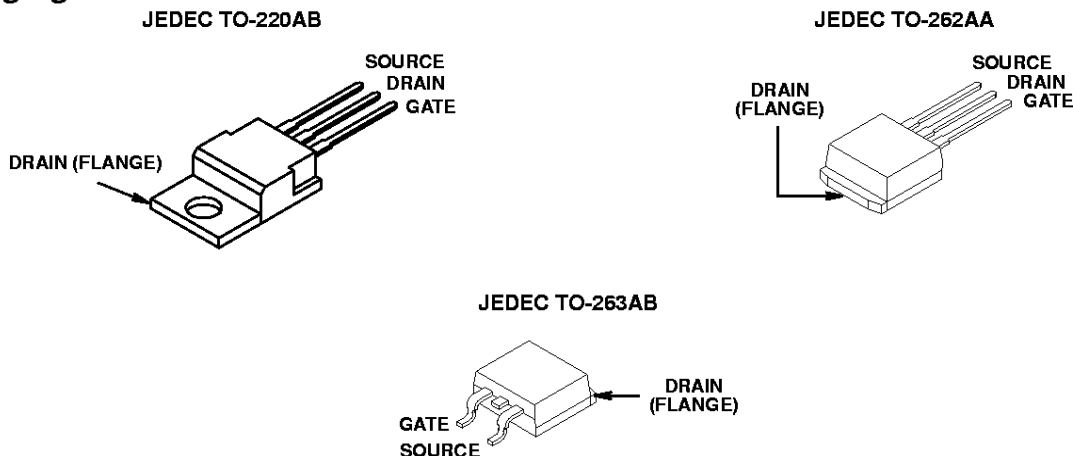
These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17423.

Symbol



Packaging



IRF644, IRF645, IRF646, IRF647, RF1S644, RF1S644SM

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	IRF644, RF1S644, RF1S644SM	IRF645	IRF646	IRF647	UNITS	
Drain to Source Voltage (Note 1)	V_{DS}	250	250	275	275	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR}	250	250	275	275	V
Continuous Drain Current	I_D	14	13	14	13	A
$T_C = 100^\circ\text{C}$	I_D	8.8	8.0	8.8	8.0	A
Pulsed Drain Current (Note 3)	I_{DM}	56	52	56	52	A
Gate to Source Voltage	V_{GS}	± 20	± 20	± 20	± 20	V
Maximum Power Dissipation	P_D	125	125	125	125	W
Linear Derating Factor		1.0	1.0	1.0	1.0	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS}	550	550	550	550	mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering						
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	300	300	300	$^\circ\text{C}$
Package Body for 10s, See TB334	T_{pkg}	260	260	260	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

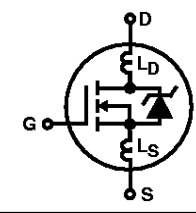
- $T_J = 25^\circ\text{C}$ to 125°C

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

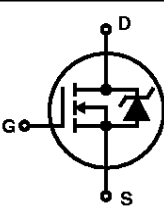
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage IRF644, IRF645, RF1S644, RF1S644SM	BV_{DSS}	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$, (Figure 10)	250	-	-	V
			IRF646, IRF647	275	-	-
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	25	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$	-	-	250	μA
On-State Drain Current (Note 2) IRF644, IRF646, RF1S644, RF1S644SM	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}, V_{GS} = 10\text{V}$, (Figure 7)	14	-	-	A
			IRF645, IRF647	13	-	-
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
Drain to Source On Resistance (Note 2) IRF644, IRF646, RF1S644, RF1S644SM	$r_{DS(ON)}$	$I_D = 8\text{A}, V_{GS} = 10\text{V}$, (Figures 8, 9)	-	0.20	0.28	Ω
			IRF645, IRF647	-	0.28	0.34
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50\text{V}, I_D = 8\text{A}$, (Figure 12)	6.7	10	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 125\text{V}, I_D \approx 14\text{A}, R_{GS} = 9.1\Omega, R_L = 8.6\Omega$, (Figures 17, 18) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	16	24	ns
Rise Time	t_r		-	67	100	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	53	80	ns
Fall Time	t_f		-	49	74	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_g(\text{TOT})$	$V_{GS} = 10\text{V}, I_D = 14\text{A}, V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$, $I_{G(\text{REF})} = 1.5\text{mA}$, (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature	-	39	59	nC
Gate to Source Charge	Q_{gs}		-	6.6	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	20	-	nC

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Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$, (Figure 11)		-	1300	-	pF
Output Capacitance	C_{OSS}			-	320	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	69	-	pF
Internal Drain Inductance	L_D	Measured from the Contact Screw on Tab to Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	4.5	-	nH
		Measured from the Drain Lead, 6mm (0.25in) from Package to Center of Die		-	7.5	-	nH
Internal Source Inductance	L_S	Measured from the Source Lead, 6mm (0.25in) from Header to Source Bonding Pad			-	7.5	-
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	80	$^\circ\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode 		-	-	14	A
Pulse Source to Drain Current (Note 3)	I_{SDM}			-	-	56	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^\circ\text{C}$, $I_{SD} = 14\text{A}$, $V_{GS} = 0\text{V}$, (Figure 13)		-	-	1.8	V
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}$, $I_{SD} = 14\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		150	300	640	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 25^\circ\text{C}$, $I_{SD} = 14\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		1.6	3.4	7.2	μC

NOTES:

2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. $V_{DD} = 50\text{V}$, starting $T_J = 25^\circ\text{C}$, $L = 4.5\text{mH}$, $R_G = 25\Omega$, peak $I_{AS} = 14\text{A}$ (Figures 15, 16).

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Typical Performance Curves Unless Otherwise Specified

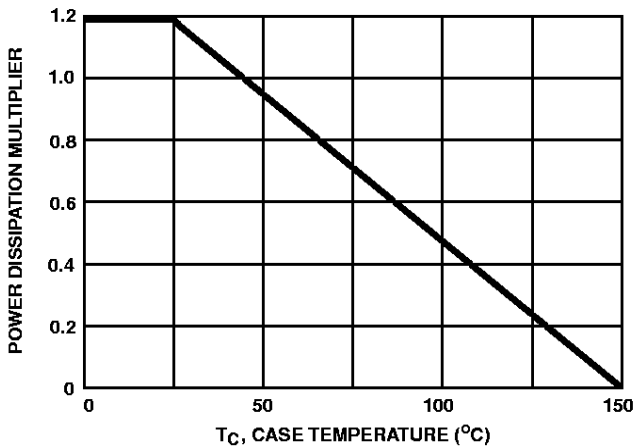


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

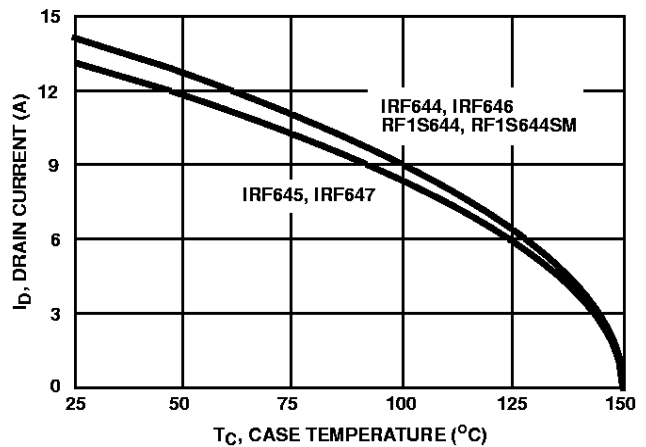


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

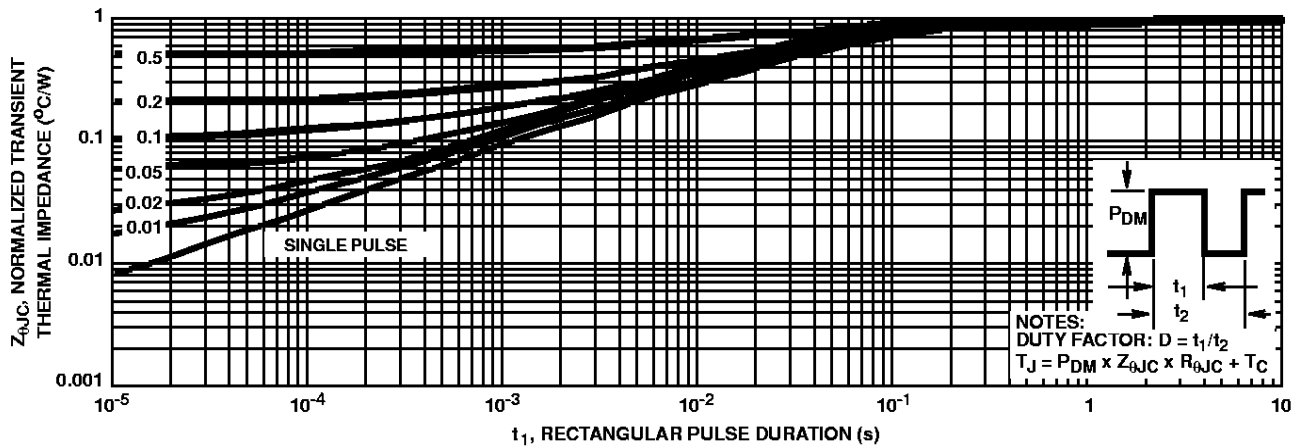


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

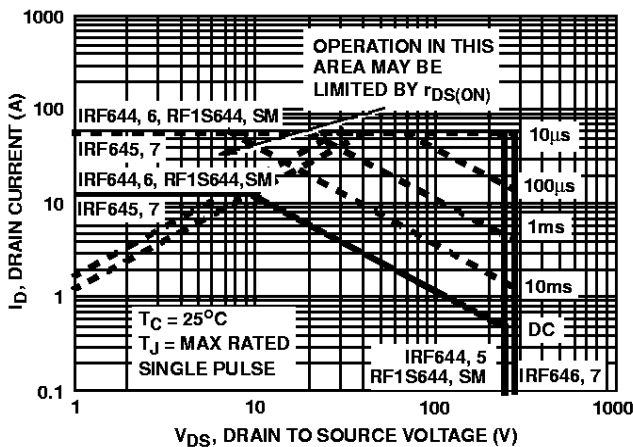


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

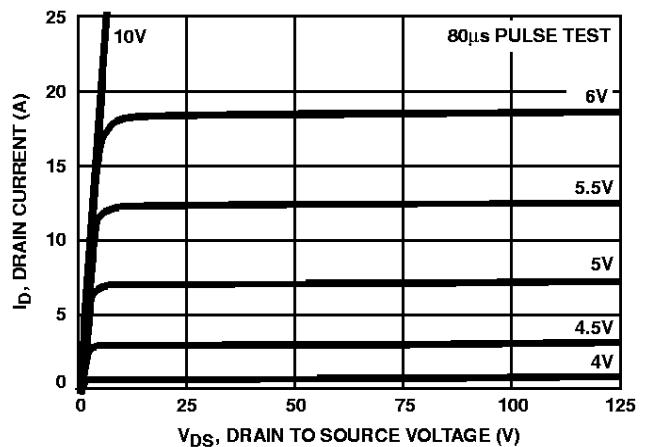


FIGURE 5. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

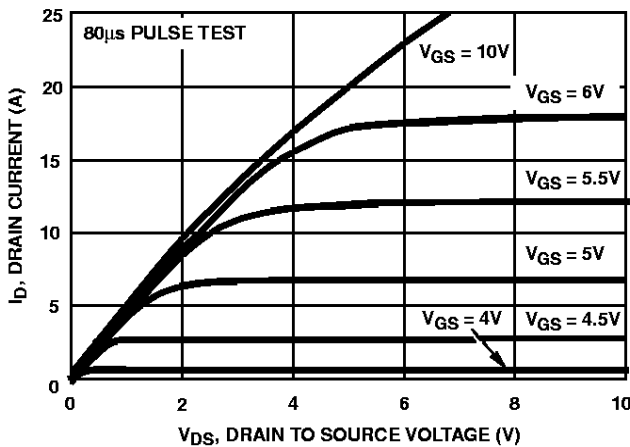


FIGURE 6. SATURATION CHARACTERISTICS

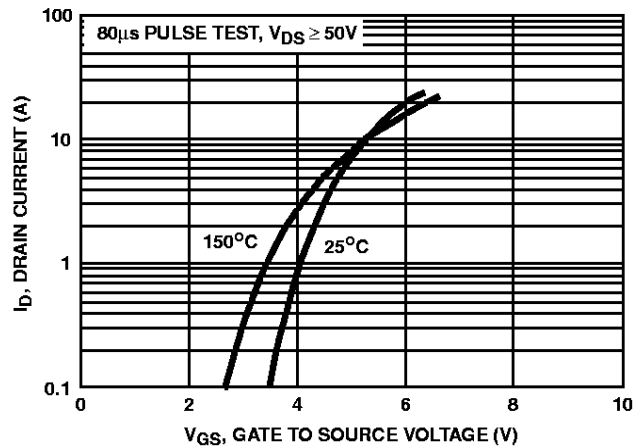


FIGURE 7. TRANSFER CHARACTERISTICS

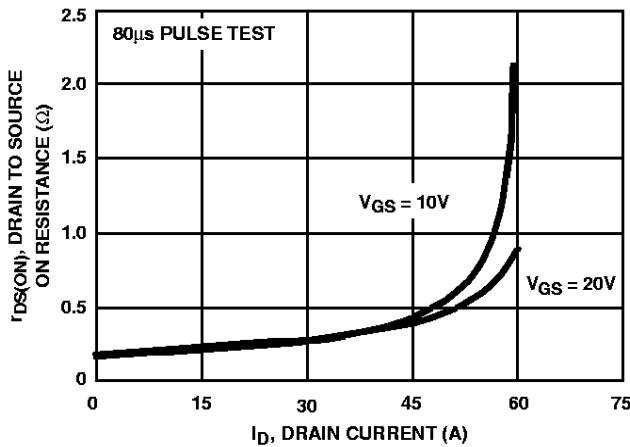


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

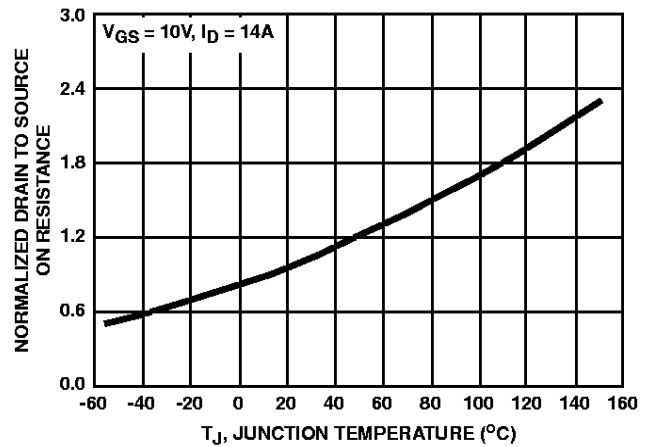


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

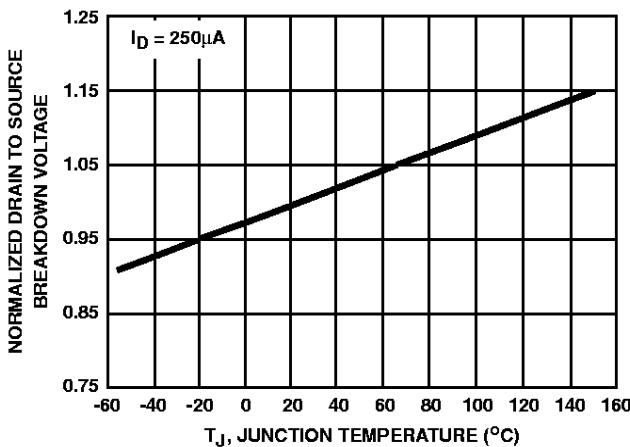


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

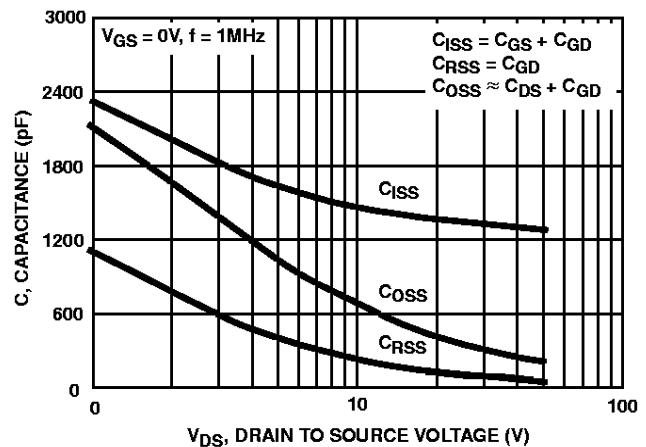


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves Unless Otherwise Specified (Continued)

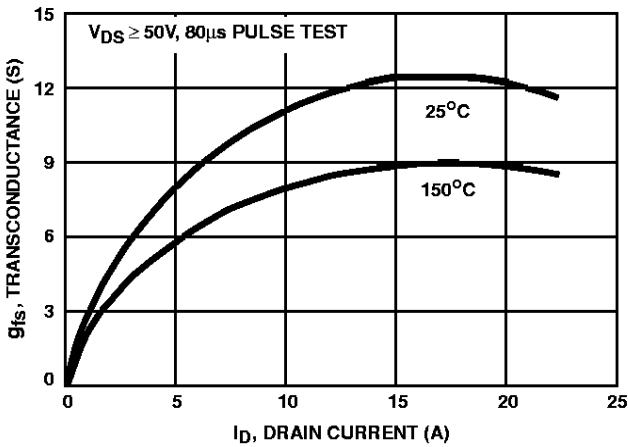


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

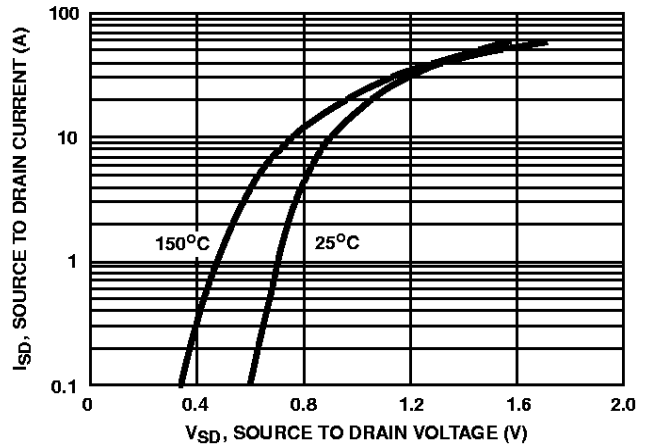


FIGURE 13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

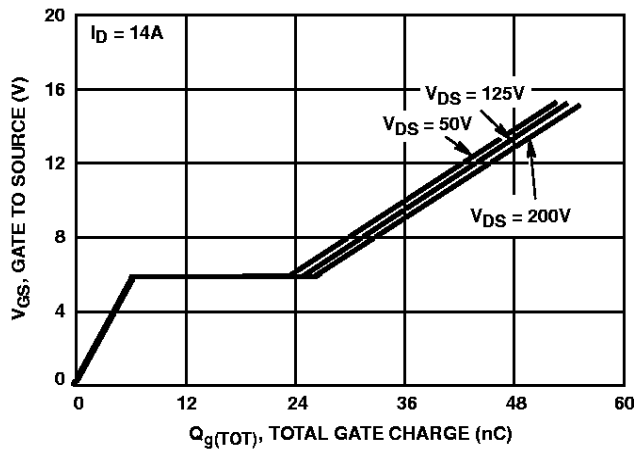


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

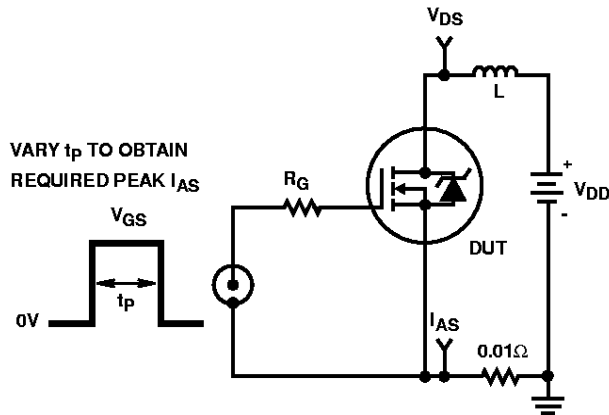


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

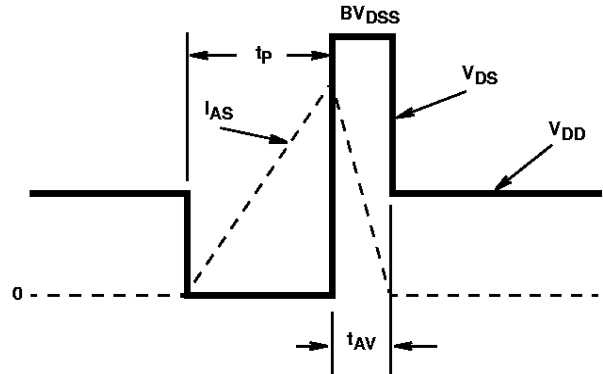


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

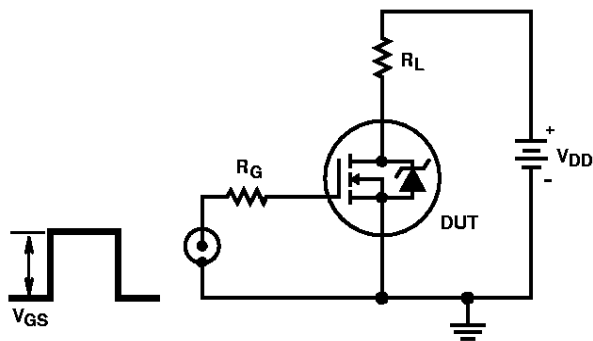


FIGURE 17. SWITCHING TIME TEST CIRCUIT

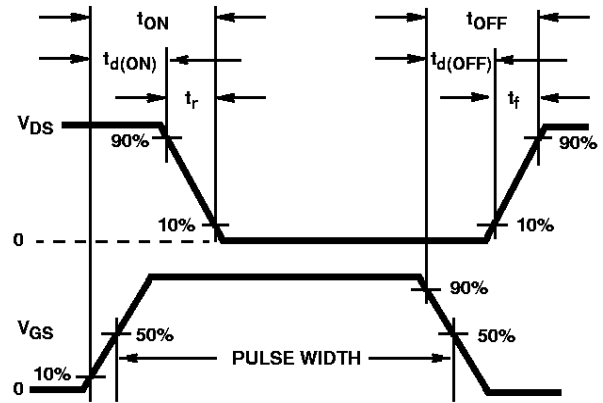


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

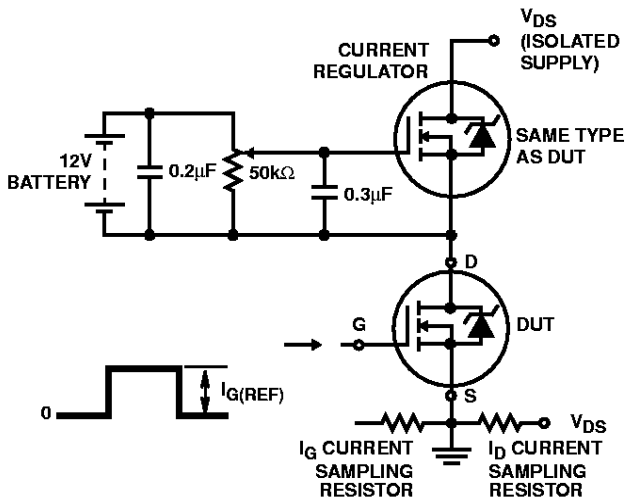


FIGURE 19. GATE CHARGE TEST CIRCUIT

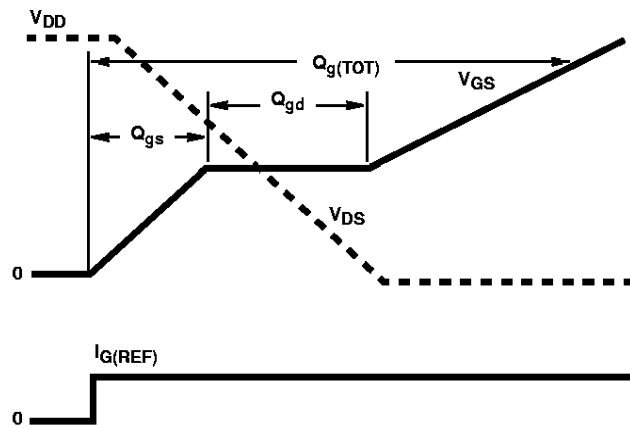


FIGURE 20. GATE CHARGE WAVEFORMS