



12 BIT, 2-TO-1, 3.3V, 2.5V LVPECL CLOCK MULTIPLEXER

ICS85352I

GENERAL DESCRIPTION



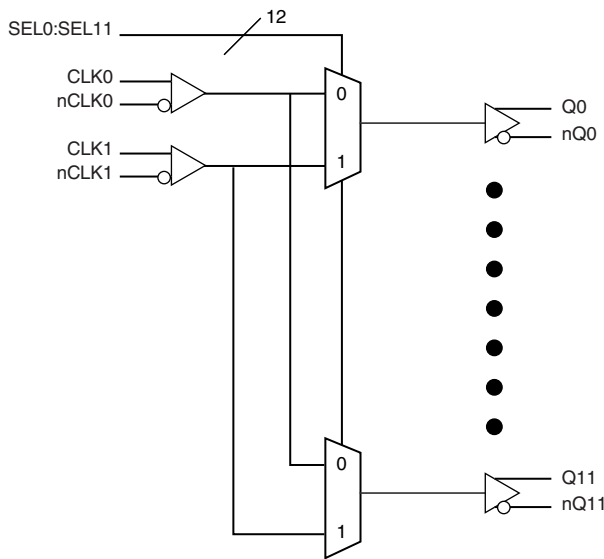
The ICS85352I is a 12 bit, 2-to-1 LVPECL Multiplexer and is a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. Individual input select controls support independent multiplexer operation from a common clock input source. Clock inputs accept most standard differential levels.

The ICS85352I is characterized at full 3.3V or mixed 3.3V core/2.5V output operating supply modes.

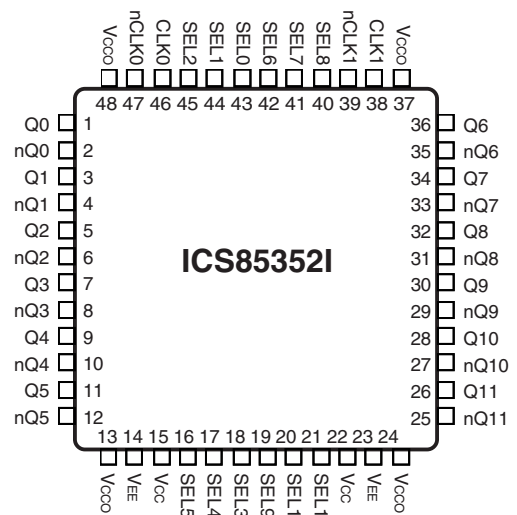
FEATURES

- Twelve, 2-to-1 multiplexers with LVPECL outputs
- Selectable differential CLKx, nCLKx input pairs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 700MHz
- Individual select control for each multiplexer
- Select inputs accept LVCMOS / LVTTTL levels
- Propagation delay: 1.8ns (maximum)
- Full 3.3V or mixed 3.3V core/2.5V output supply
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Lead TQFP, E-PAD
7mm x 7mm x 1.0mm package body
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2 3, 4 5, 6 7, 8 9, 10 11, 12 25, 26 27, 28 29, 30 31, 32 33, 34 35, 36	Q0, nQ0 Q1, nQ1 Q2, nQ2 Q3, nQ3 Q4, nQ4 Q5, nQ5 nQ11, Q11 nQ10, Q10 nQ9, Q9 nQ8, Q8 nQ7, Q7 nQ6, Q6	Output		Differential output pairs. LVPECL interface levels.
13, 24, 37, 48	V _{CCO}	Power		Output supply pins.
14, 23	V _{EE}	Power		Negative supply pins.
15, 22	V _{CC}	Power		Positive supply pins.
16, 17, 18, 19, 20, 21, 40, 41, 42, 43, 44, 45	SEL5, SEL4, SEL3, SEL9, SEL10, SEL11, SEL8, SEL7, SEL6, SEL0, SEL1, SEL2	Input	Pulldown	Clock select inputs. LVCMOS / LVTTTL interface levels.
38	CLK1	Input	Pulldown	Non-inverting differential clock input.
39	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. V _{CC} /2 default when left floating.
46	CLK0	Input	Pulldown	Non-inverting differential clock input.
47	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. V _{CC} /2 default when left floating.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ

TABLE 3. CONTROL INPUT FUNCTION TABLE

SELx	Selected Clock Inputs
0	CLK0, nCLK0
1	CLK1, nCLK1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to $V_{CC} + 0.5V$
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	27.6°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $V_{CCO} = 2.5V$ TO $3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		2.375	3.3	3.465	V
I_{EE}	Power Supply Current				170	mA

TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $V_{CCO} = 2.5V$ TO $3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	SEL0:SEL11	2		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	SEL0:SEL11	-0.3		0.8	V
I_{IH}	Input High Current	SEL0, SEL11 $V_{CC} = V_{IN} = 3.465V$			150	μA
I_{IL}	Input Low Current	SEL0, SEL11 $V_{CC} = 3.465V, V_{IN} = 0V$	-5			μA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $V_{CCO} = 2.5V$ TO $3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, CLK1 $V_{CC} = V_{IN} = 3.465V$			150	μA
		nCLK0, nCLK1 $V_{CC} = V_{IN} = 3.465V$			150	μA
I_{IL}	Input Low Current	CLK0, CLK1 $V_{CC} = 3.465V, V_{IN} = 0V$	-5			μA
		nCLK0, nCLK1 $V_{CC} = 3.465V, V_{IN} = 0V$	-150			μA
V_{PP}	Peak-to-Peak Voltage		0.15		1.0	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1: Common mode input voltage is defined as V_{IH} .

NOTE 2: For single ended applications, the maximum input voltage for CLKx, nCLKx is $V_{CC} + 0.3V$.

TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $V_{CC0} = 2.5V$ TO $3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CC0} - 1.4$		$V_{CC0} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CC0} - 2.0$		$V_{CC0} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to $V_{CC0} - 2V$.

TABLE 5A. AC CHARACTERISTICS, $V_{CC} = V_{CC0} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1		1.0	1.5	2.0	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4				180	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				750	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	150		700	ps
odc	Output Duty Cycle	$f \leq 622MHz$	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{CC} = 3.3V \pm 5\%$, $V_{CC0} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1		1.0	1.5	2.0	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4				180	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				750	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	150		700	ps
odc	Output Duty Cycle	$f \leq 622MHz$	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

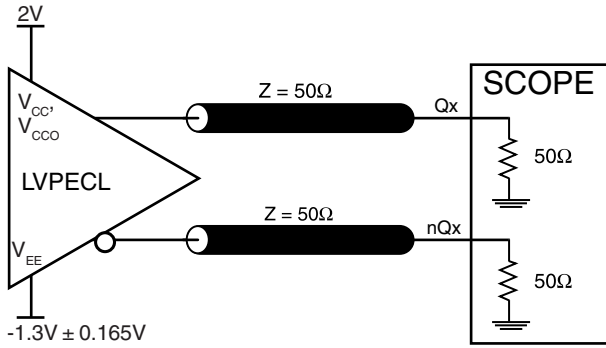
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential cross points.

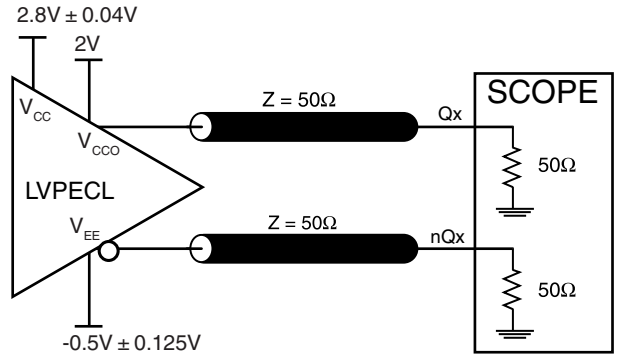
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

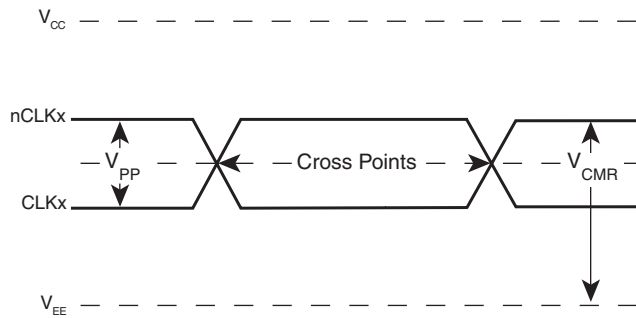
PARAMETER MEASUREMENT INFORMATION



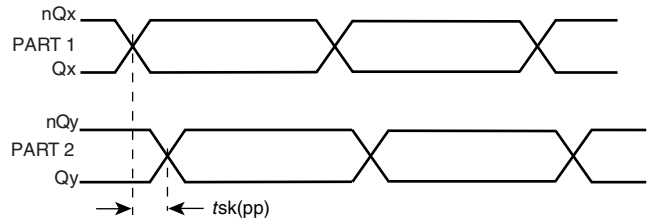
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



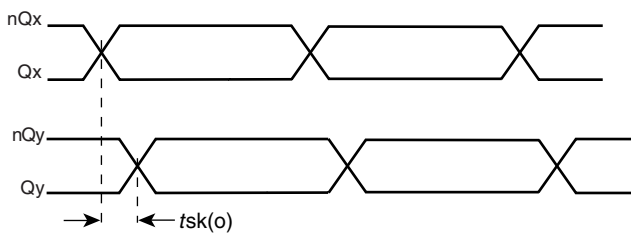
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



DIFFERENTIAL INPUT LEVEL



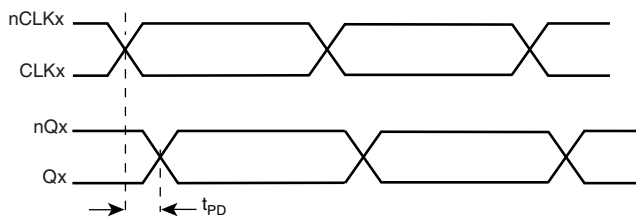
PART-TO-PART SKEW



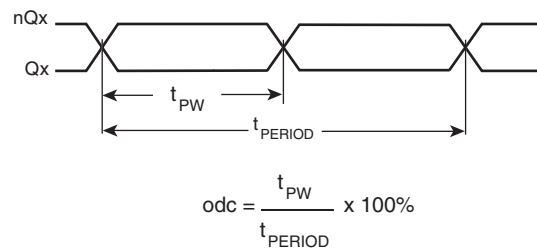
OUTPUT SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

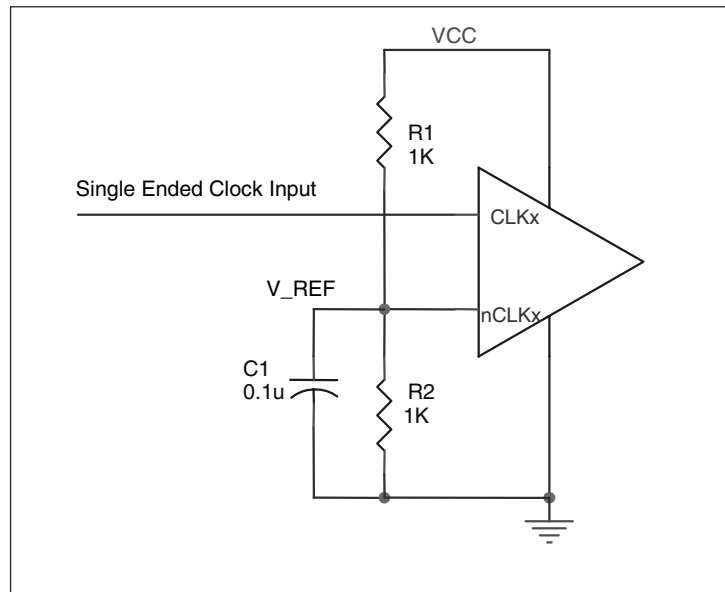


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK/nCLK INPUT:

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from CLK to ground.

LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

OUTPUTS:

LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 2A to 2E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are

examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A*, the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

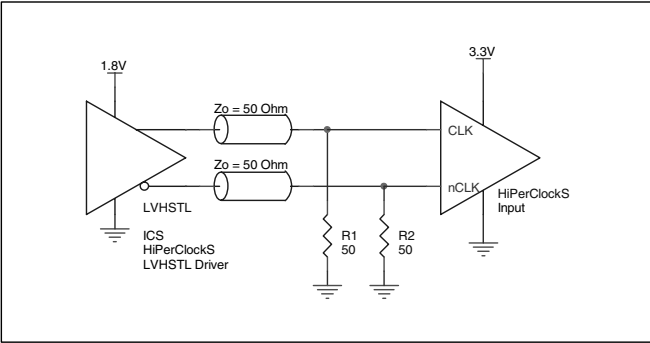


FIGURE 2A. HiPerClockS CLK/nCLK INPUT DRIVEN BY IDT HiPerClockS LVHSTL DRIVER

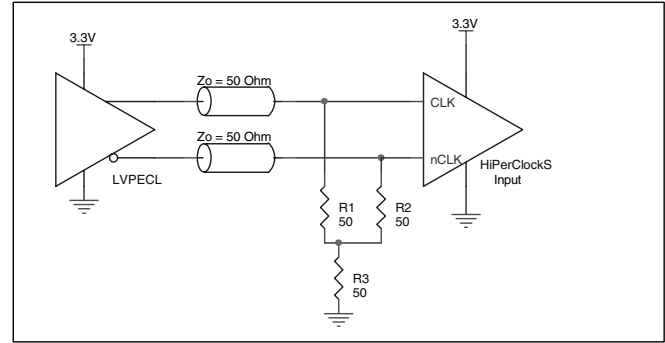


FIGURE 2B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

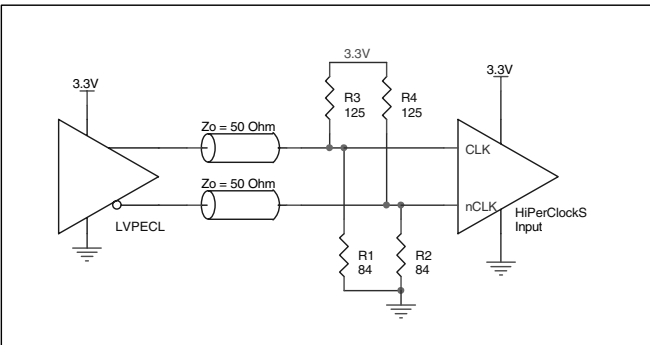


FIGURE 2C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

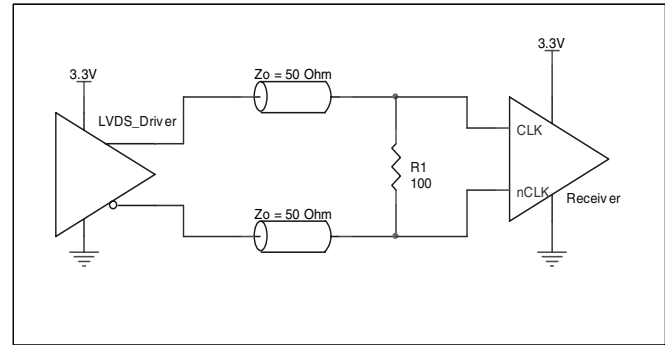


FIGURE 2D. HiPerClockS CLK/nCLK INPUT DRIVEN BY LVDS DRIVER

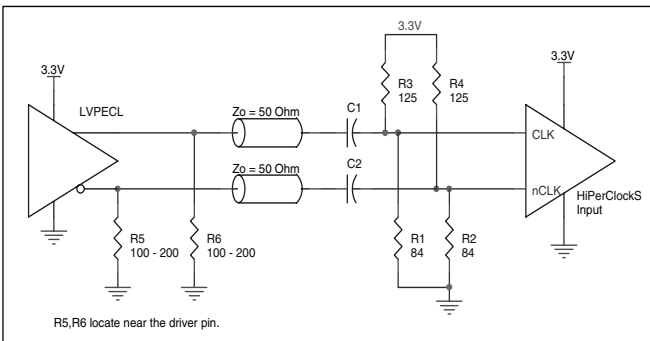


FIGURE 2E. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

THERMAL RELEASE PATH

The expose metal pad provides heat transfer from the device to the P.C. board. The expose metal pad is ground pad connected to ground plane through thermal via. The exposed pad on the device to the exposed metal pad on the PCB is contacted through

solder as shown in *Figure 6*. For further information, please refer to the Application Note on Surface Mount Assembly of Amkor's Thermally /Electrically Enhance Leadframe Base Package, Amkor Technology.

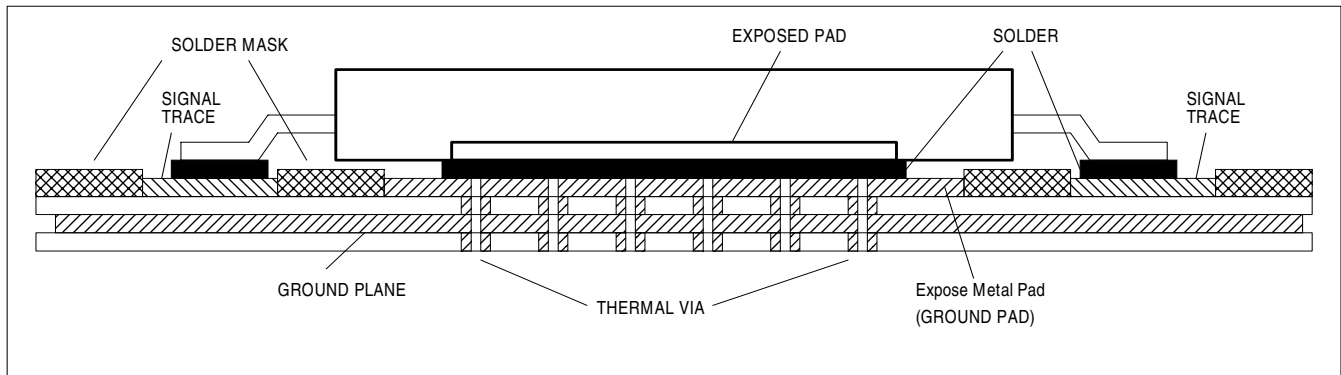


FIGURE 3. P.C. BOARD FOR EXPOSED PAD THERMAL RELEASE PATH EXAMPLE

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

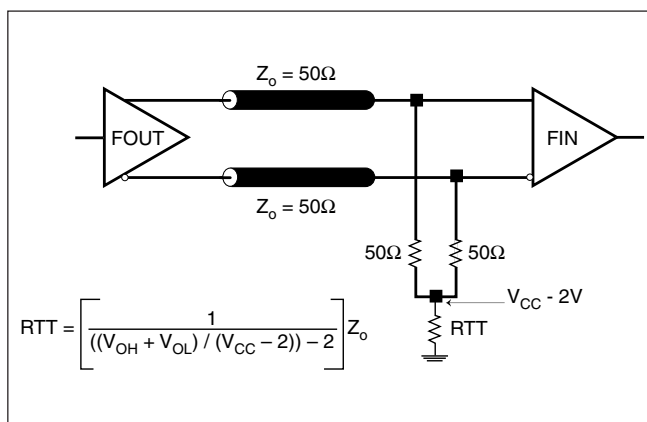


FIGURE 4A. LVPECL OUTPUT TERMINATION

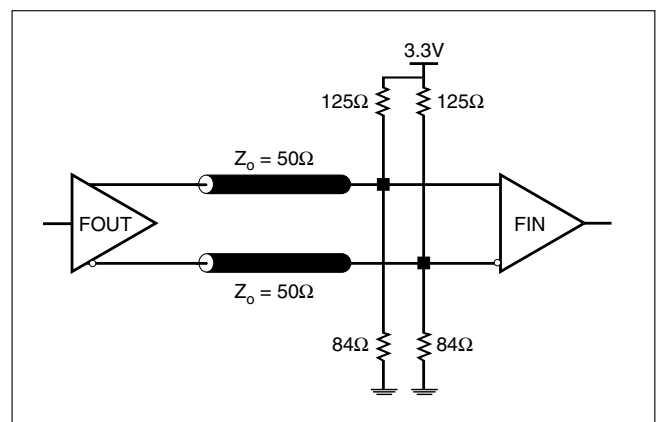


FIGURE 4B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{cc} - 2V$. For $V_{cc} = 2.5V$, the $V_{cc} - 2V$ is very close to ground

level. The R3 in Figure 5B can be eliminated and the termination is shown in Figure 5C.

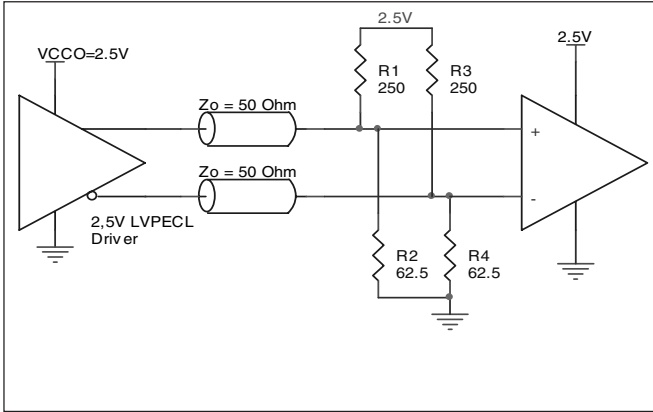


FIGURE 5A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

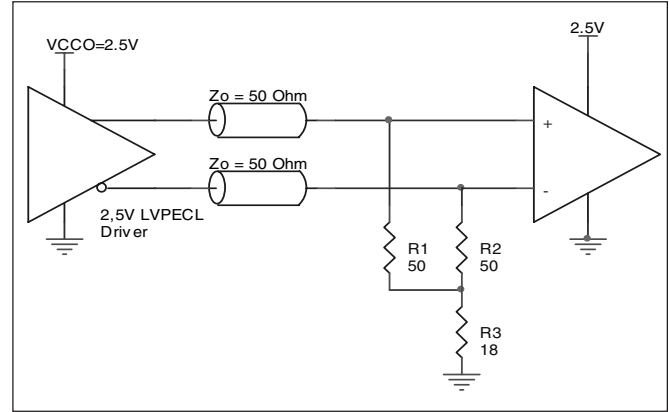


FIGURE 5B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

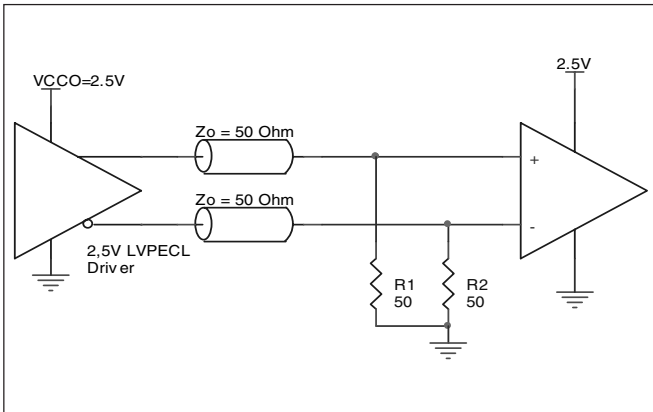


FIGURE 5C. 2.5V LVPECL TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS85352I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS85352I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC,MAX} * I_{EE,MAX} = 3.465V * 170mA = 589.1mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**

If all outputs are loaded, the total power is $12 * 30mW = 360mW$

Total Power_{MAX} (3.465V, with all outputs switching) = $589.1mW + 360mW = 949.1mW$

2. Junction Temperature.

Junction temperature, T_j, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_{total} + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_{total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 22.6°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 0.949W * 22.6^\circ C/W = 106.4^\circ C$. This is well below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 48-PIN TQFP, FORCED CONVECTION

	θ_{JA} by Velocity (Linear Feet per Minute)		
	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	27.6°C/W	22.6°C/W	20.7°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7*.

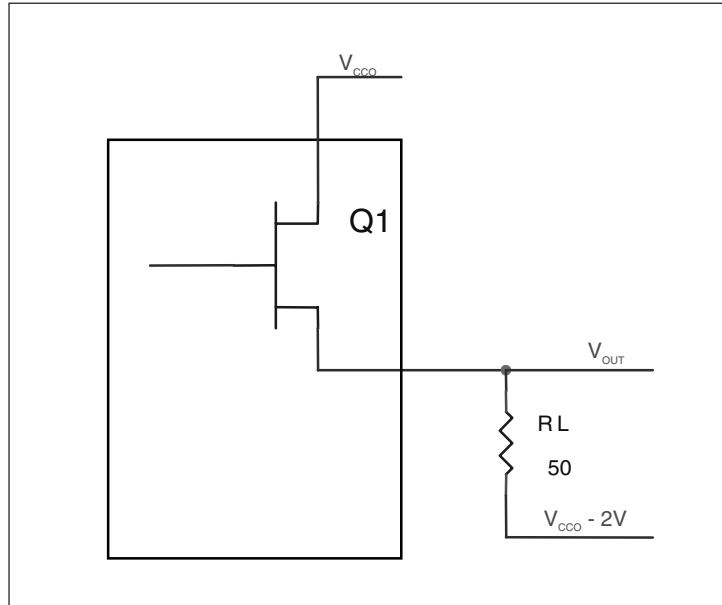


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCO_MAX} - 0.9V$

$$(V_{CCO_MAX} - V_{OH_MAX}) = 0.9V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCO_MAX} - 1.7V$

$$(V_{CCO_MAX} - V_{OL_MAX}) = 1.7V$$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair = Pd_H + Pd_L = 30mW

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 48 LEAD TQFP, E-PAD

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	27.6°C/W	22.6°C/W	20.7°C/W

TRANSISTOR COUNT

The transistor count for ICS85352I is: 2252

PACKAGE OUTLINE - Y SUFFIX FOR 48L TQFP, E-PAD

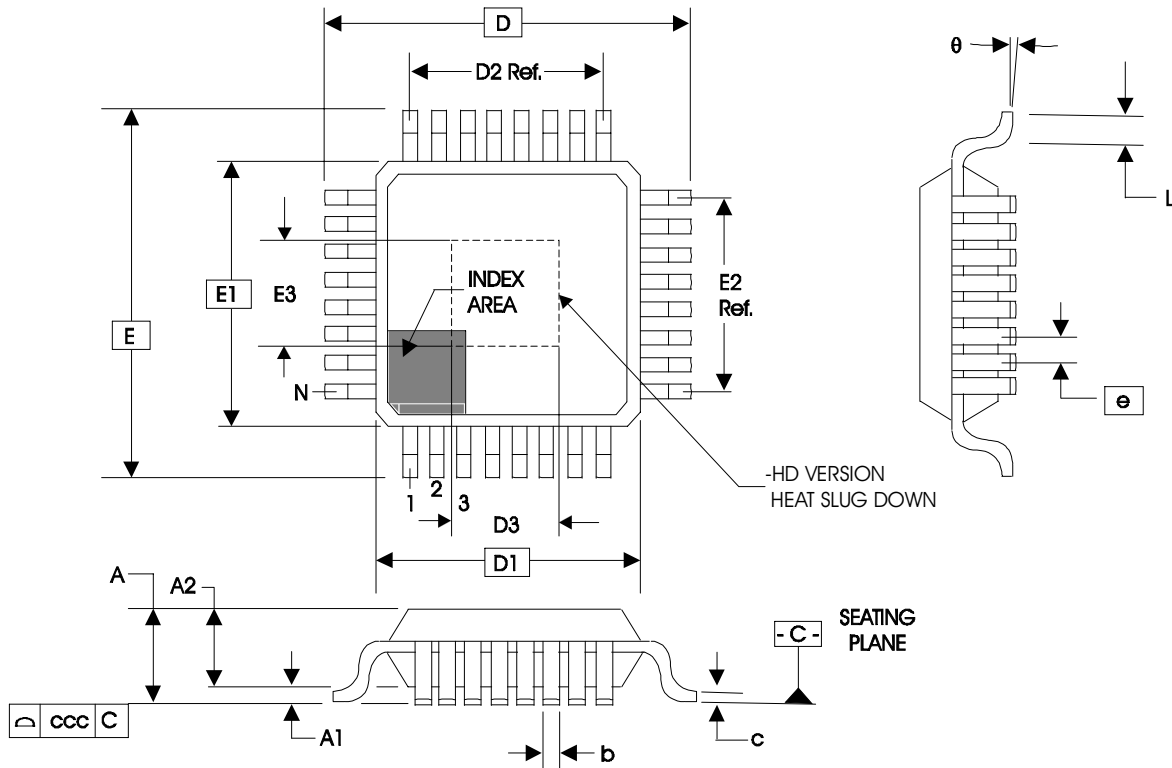


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	ABC - HD		
	MINIMUM	NOMINAL	MAXIMUM
N	48		
A	--	--	1.20
A1	0.05	--	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09		0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	4.00 BASIC		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	4.00 BASIC		
e	0.5 BASIC		
L	0.45	0.60	0.75
θ	0°		7°
ccc	--	--	0.08
D3 & E3	2.0		7.0

Reference Document: JEDEC Publication 95, MS-026 REV. A

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS85352AYI	ICS85352AYI	48 Lead TQFP, E-PAD	tray	-40°C to 85°C
ICS85352AYIT	ICS85352AYI	48 Lead TQFP, E-PAD	1000 tape & reel	-40°C to 85°C
ICS85352AYILF	ICS85352AYIL	48 Lead "Lead-Free" TQFP, E-PAD	tray	-40°C to 85°C
ICS85352AYILFT	ICS85352AYIL	48 Lead "Lead-Free" TQFP, E-PAD	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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REVISION HISTORY SHEET

Rev	Table	Page	Description of Change	Date
A	T9	1	Features Section - added lead-free bullet.	7/6/06
		6	Added <i>Recommendations for Unused Input and Output Pins</i> .	
		7	Added <i>Thermal Release Path</i> .	
	T4A	15	Ordering Information Table - added lead-free part number, marking and note.	
B		3	Power Supply DC Characteristics Table - corrected V_{CC} min. from 3.475V to 3.135V.	9/27/06

ICS85352I

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