Analog Multiplexers/ Demultiplexers with Injection Current Effect Control

Automotive Customized

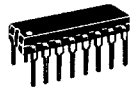
MC74HC4851A
MC74HC4852A
MC74HC4853A

These devices are pin compatible to standard HC405x and MC1405xB analog mux/demux devices, but feature injection current effect control. This makes them especially suited for usage in automotive applications where voltages in excess of normal logic voltage are common.

The injection current effect control allows signals at disabled analog input channels to exceed the supply voltage range without affecting the signal of the enabled analog channel. This eliminates the need for external diode/ resistor networks typically used to keep the analog channel signals within the supply voltage range.

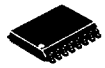
The devices utilize low power silicon gate CMOS technology. The Channel Select and Enable inputs are compatible with standard CMOS outputs.

- Injection Current Cross–Coupling Less than 1mV/mA (See Figure 11)
- Pin Compatible to HC405X and MC1405XB Devices
- Power Supply Range (V_{CC} – GND) = 2.0 to 6.0 V
- In Compliance With the Requirements of JEDEC Standard No. 7A
- Chip Complexity: 154 FETs or 36 Equivalent Gates



N SUFFIX
16–LEAD PLASTIC DIP PACKAGE
CASE 648–08

D SUFFIX
16–LEAD PLASTIC SOIC PACKAGE
CASE 751B–05



DW SUFFIX
16–LEAD PLASTIC WIDE SOIC PACKAGE
CASE 751G–02

DT SUFFIX
16–LEAD PLASTIC TSSOP PACKAGE
CASE 948F–01

ORDERING INFORMATION

MC74HCXXXXAN	Plastic
MC74HCXXXXAD	SOIC
MC74HCXXXXADW	SOIC Wide
MC74HCXXXXADT	TSSOP

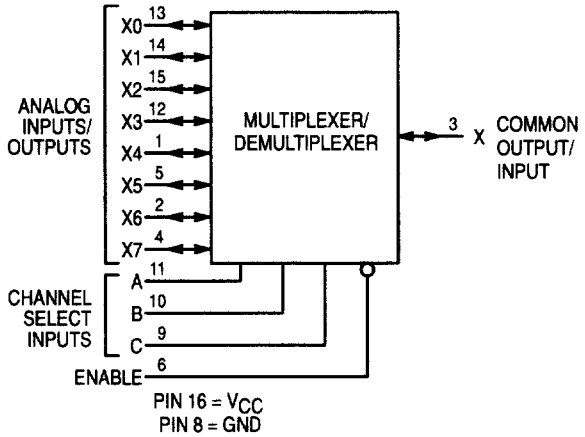


Figure 1. MC74HC4851A Logic Diagram
Single–Pole, 8–Position Plus Common Off

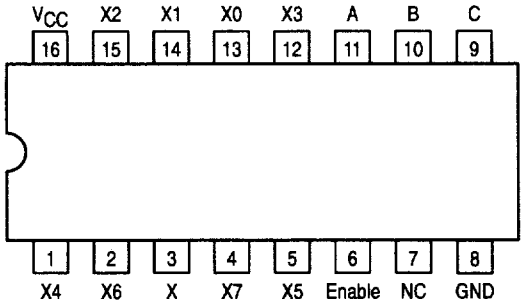


Figure 2. MC74HC4851A 16–Lead Pinout (Top View)

FUNCTION TABLE – MC74HC4851A

Control Inputs				
	Select			
Enable	C	B	A	ON Channels
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

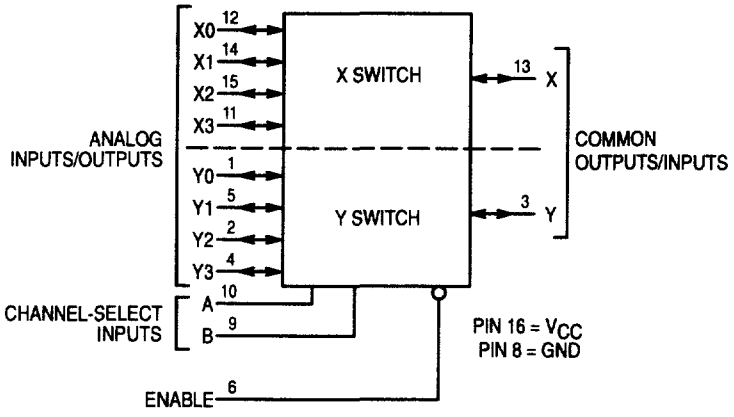


Figure 3. MC74HC4852A Logic Diagram
Double–Pole, 4–Position Plus Common Off

FUNCTION TABLE – MC74HC4852A

Control Inputs				
Enable	Select B	Select A	ON Channels	
L	L	L	Y0	X0
L	L	H	Y1	X1
L	H	L	Y2	X2
L	H	H	Y3	X3
H	X	X	NONE	

X = Don't Care

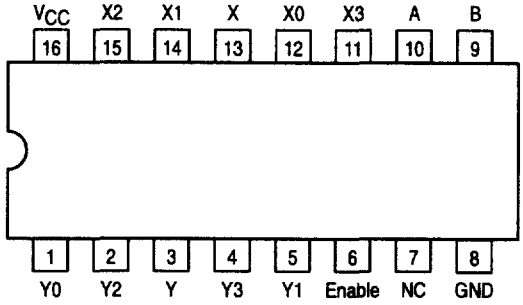
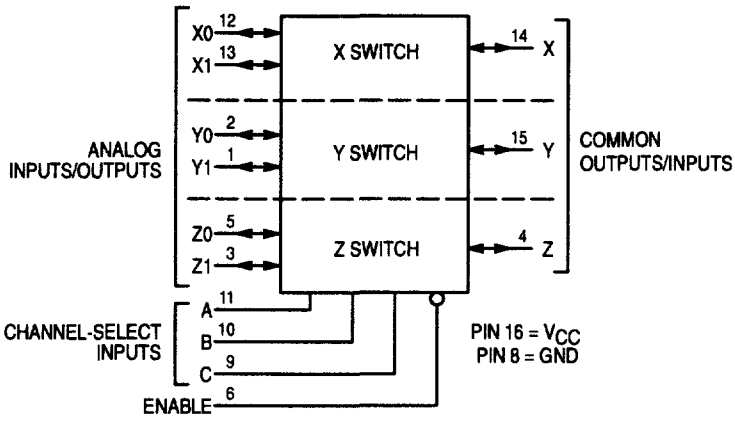


Figure 4. MC74HC4852A 16–Lead Pinout (Top View)



NOTE: This device allows independent control of each switch. Channel–Select Input A controls the X–Switch, Input B controls the Y–Switch and Input C controls the Z–Switch

Figure 5. MC74HC4853A Logic Diagram
Triple Single–Pole, Double–Position Plus Common Off

FUNCTION TABLE – MC74HC4853A

Control Inputs						
Enable	Select C	Select B	Select A	ON Channels		
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	NONE		

X = Don't Care

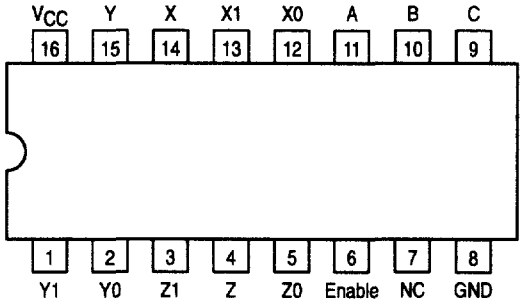


Figure 6. MC74HC4853A 16–Lead Pinout (Top View)

MAXIMUM RATINGS*

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage	(Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Any Pin)	(Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin		± 25	mA
P_D	Power Dissipation in Still Air,	Plastic DIP†	750	mW
		SOIC Package†	500	
		TSSOP Package†	450	
T_{stg}	Storage Temperature Range		– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package		260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	(Referenced to GND)	2.0	6.0	V
V_{in}	DC Input Voltage (Any Pin)	(Referenced to GND)	GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		0.0	1.2	V
T_A	Operating Temperature Range, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time	V_{CC} = 2.0 V	0	1000	ns
	(Channel Select or Enable Inputs)	V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

* For voltage drops across switch greater than 1.2V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) V_{EE} = GND, Except Where Noted

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0	1.50	1.50	1.50	V
			3.0	2.10	2.10	2.10	
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0	0.50	0.50	0.50	V
			3.0	0.90	0.90	0.90	
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	
I_{in}	Maximum Input Leakage Current on Digital Pins (Enable/A/B/C)	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in(digital)}$ = V_{CC} or GND $V_{in(analog)}$ = GND	6.0	2	20	40	µA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

DC CHARACTERISTICS — Analog Section

Symbol	Parameter	Condition	V_{CC}	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
R_{on}	Maximum "ON" Resistance	$V_{in} = V_{IL}$ or V_{IH}; $V_{IS} = V_{CC}$ to GND; $I_S \leq 2.0$ mA	2.0 3.0 4.5 6.0	1700 1100 550 400	1750 1200 650 500	1800 1300 750 600	Ω
ΔR_{on}	Delta "ON" Resistance	$V_{in} = V_{IL}$ or V_{IH}; $V_{IS} = V_{CC}/2$ $I_S \leq 2.0$ mA	2.0 3.0 4.5 6.0	300 460 80 60	400 200 100 80	500 240 120 100	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel Common Channel	$V_{in} = V_{CC}$ or GND	 6.0	 ±0.1 ±0.2	 ±0.5 ±2.0	 ±1.0 ±4.0	µA
I_{on}	Maximum On–Channel Leakage Channel–to–Channel	$V_{in} = V_{CC}$ or GND	 6.0	 ±0.2	 ±2.0	 ±4.0	µA

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	–55 to 25°C	≤85°C	≤125°C	Unit
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Analog Input to Analog Output	2.0 3.0 4.5 6.0	160 80 40 30	180 90 45 35	200 100 50 40	ns
t_{PHL}, $t_{PHZ,PZH}$ t_{PLH}, $t_{PLZ,PZL}$	Maximum Propagation Delay, Enable or Channel–Select to Analog Output	2.0 3.0 4.5 6.0	260 160 80 60	280 180 90 70	300 200 100 80	ns
C_{in}	Maximum Input Capacitance — Digital Pins (All Switches Off) — Any Single Analog Pin (All Switches Off) — Common Analog Pin		10 35 130	10 35 130	10 35 130	pF
C_{PD}	Power Dissipation Capacitance — Typical	5.0	20			pF

INJECTION CURRENT COUPLING SPECIFICATIONS (V_{CC} = 5V, T_A = –55°C to +125°C)

Symbol	Parameter	Typ	Max	Unit	Condition
$V\Delta_{out}$	Maximum Shift of Output Voltage of Enabled Analog Channel	0.1 1.0 0.5 5.0	0.5 5.0 2.0 20	mV	I_{in}* ≤ 1mA, $R_S \leq 3{,}9k\Omega$ I_{in}* ≤ 10mA, $R_S \leq 3{,}9k\Omega$ I_{in}* ≤ 1mA, $R_S \leq 20k\Omega$ I_{in}* ≤ 10mA, $R_S \leq 20k\Omega$

* I_{in} = Total current injected into all disabled channels.

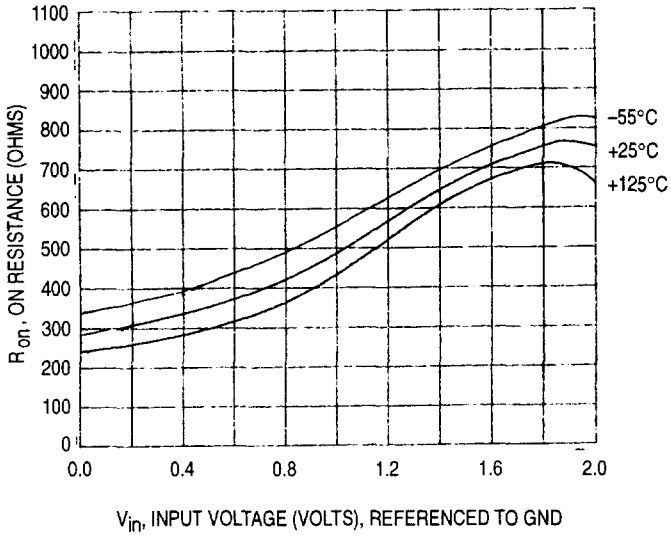


Figure 7. Typical On Resistance V_{CC} = 2V

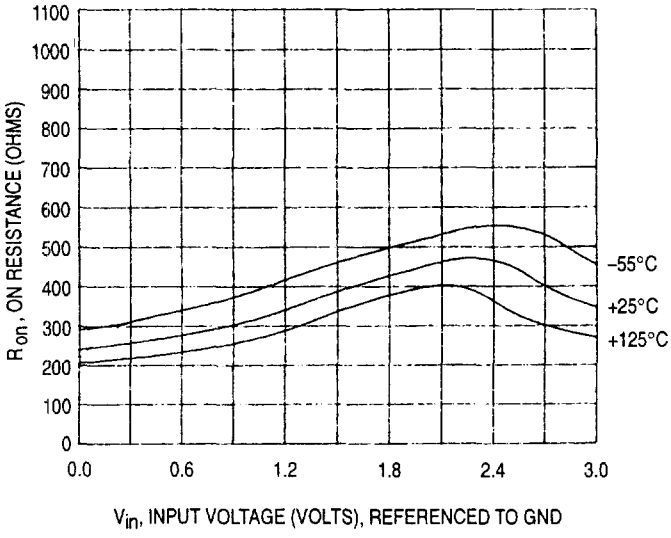


Figure 8. Typical On Resistance V_{CC} = 3V

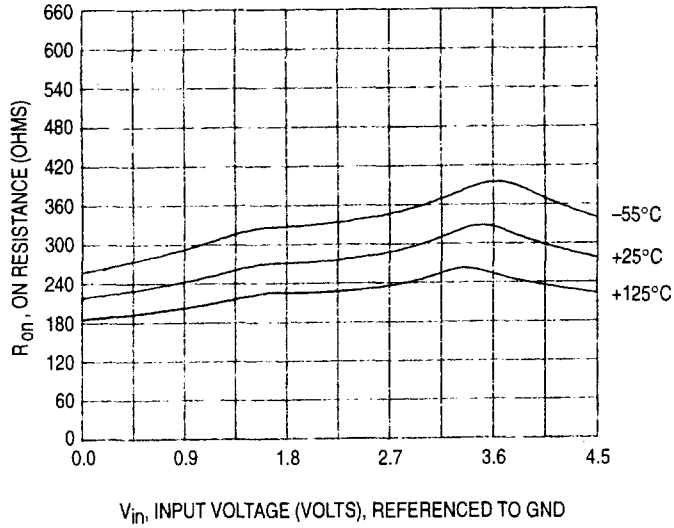


Figure 9. Typical On Resistance V_{CC} = 4.5V

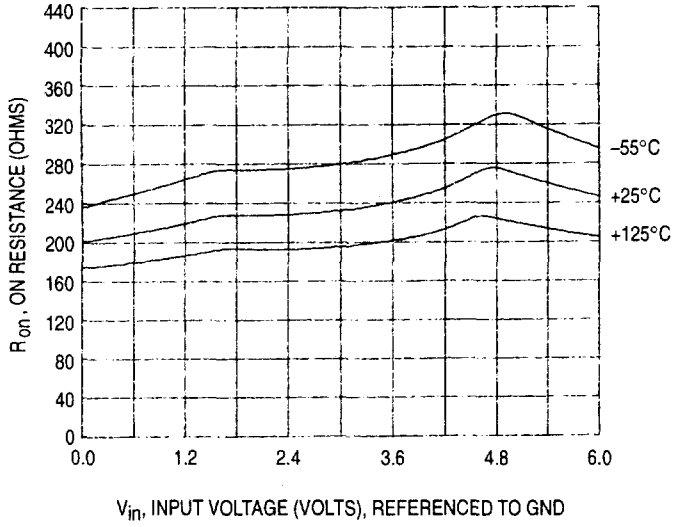


Figure 10. Typical On Resistance V_{CC} = 6V

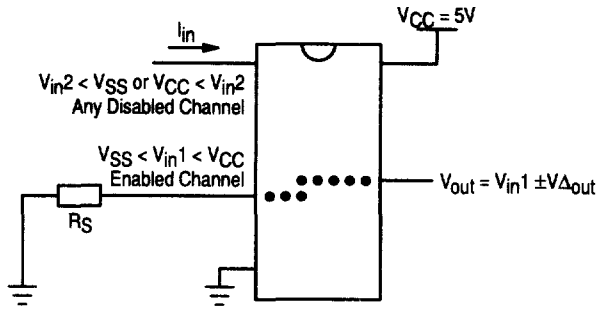


Figure 11. Injection Current Coupling Specification

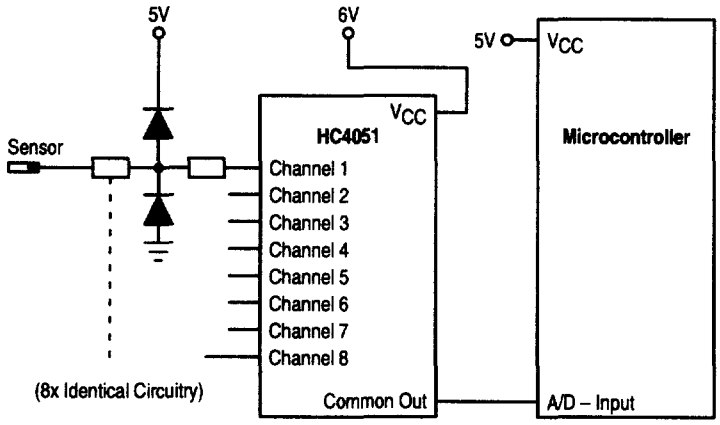


Figure 12. Actual Technology
Requires 32 passive components and one extra 6V regulator
to suppress injection current into a standard HC4051 multiplexer

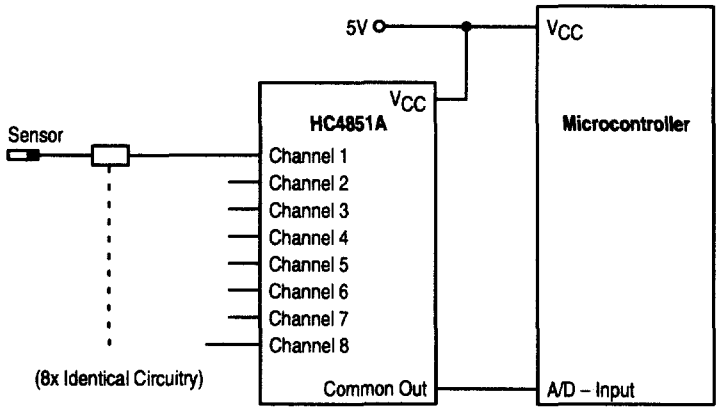


Figure 13. MC74HC4851A Solution
Solution by applying the HC4851A multiplexer

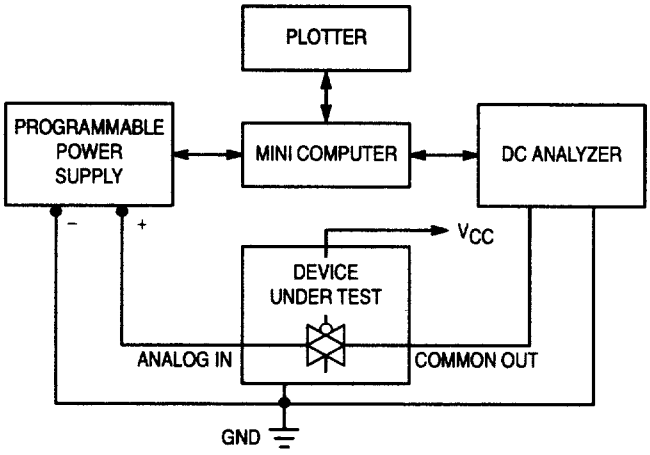


Figure 14. On Resistance Test Set–Up

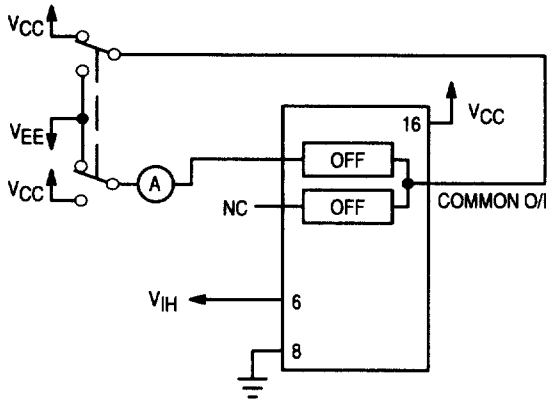


Figure 15. Maximum Off Channel Leakage Current, Any One Channel, Test Set–Up

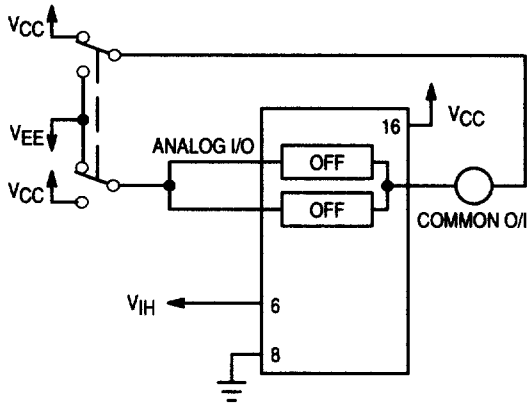


Figure 16. Maximum Off Channel Leakage Current, Common Channel, Test Set–Up

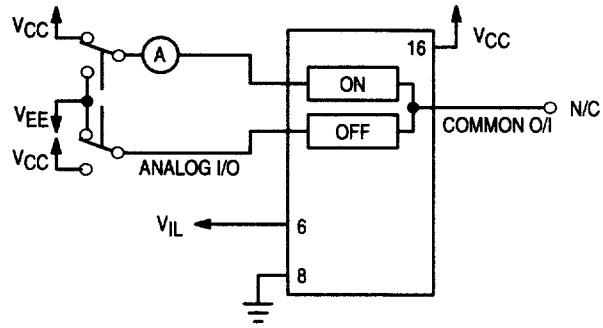


Figure 17. Maximum On Channel Leakage Current, Channel to Channel, Test Set–Up

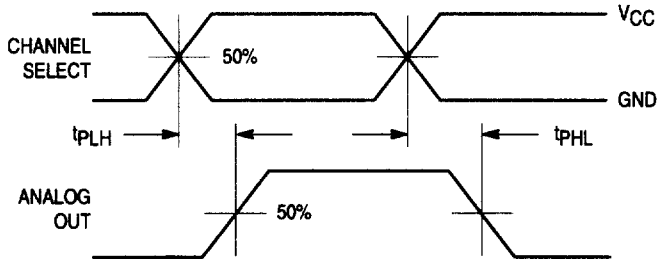
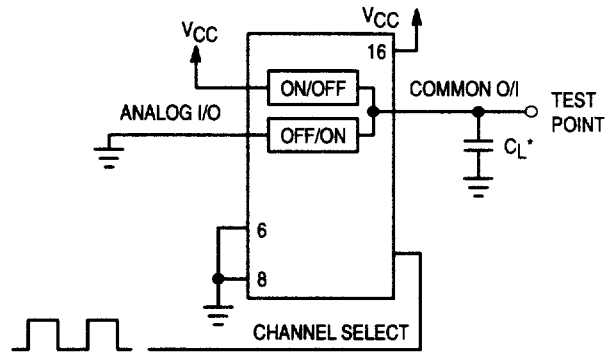


Figure 18. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 19. Propagation Delay, Test Set–Up Channel Select to Analog Out

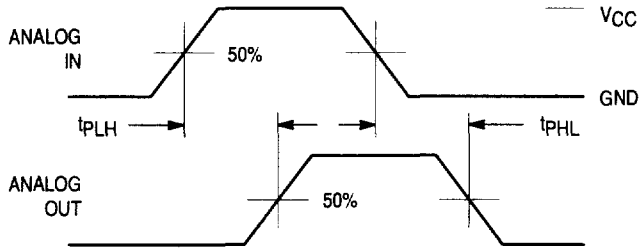
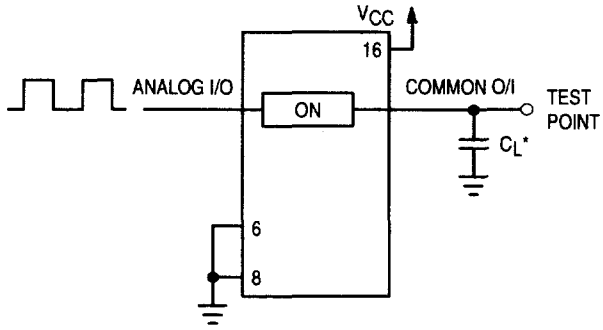


Figure 20. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 21. Propagation Delay, Test Set–Up Analog In to Analog Out

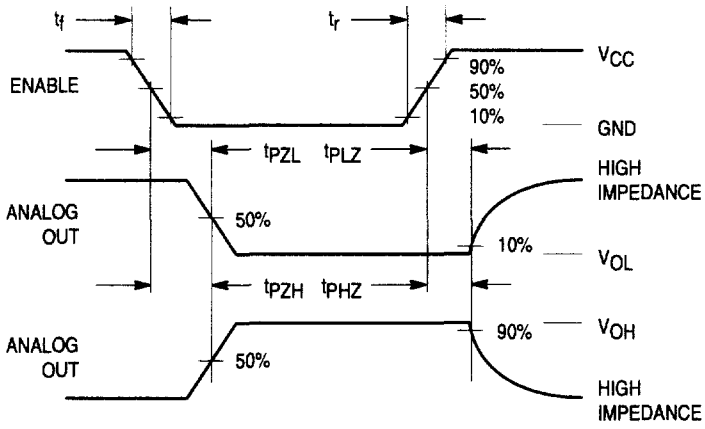


Figure 22. Propagation Delays, Enable to Analog Out

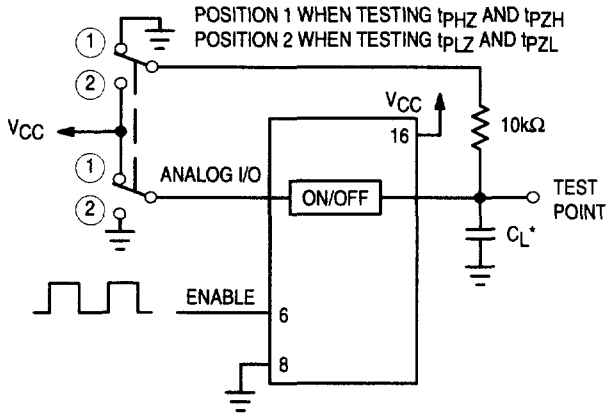


Figure 23. Propagation Delay, Test Set–Up Enable to Analog Out

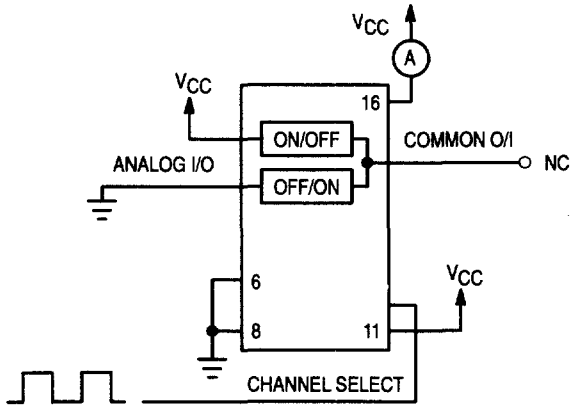


Figure 24. Power Dissipation Capacitance, Test Set–Up

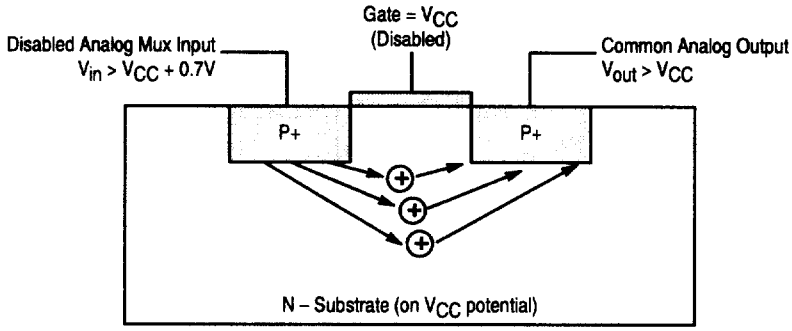


Figure 25. Diagram of Bipolar Coupling Mechanism
Appears if V_{in} exceeds V_{CC}, driving injection current into the substrate

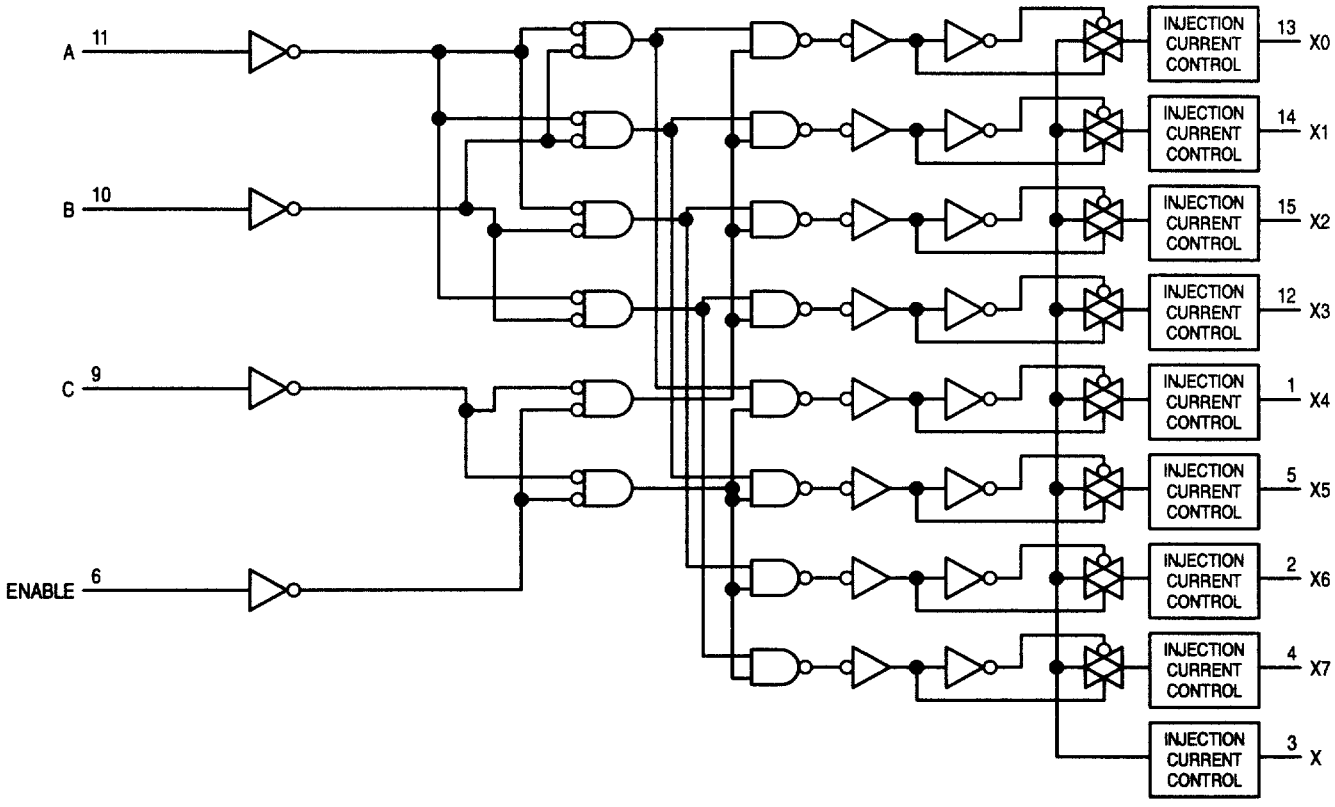


Figure 26. Function Diagram, HC4851A

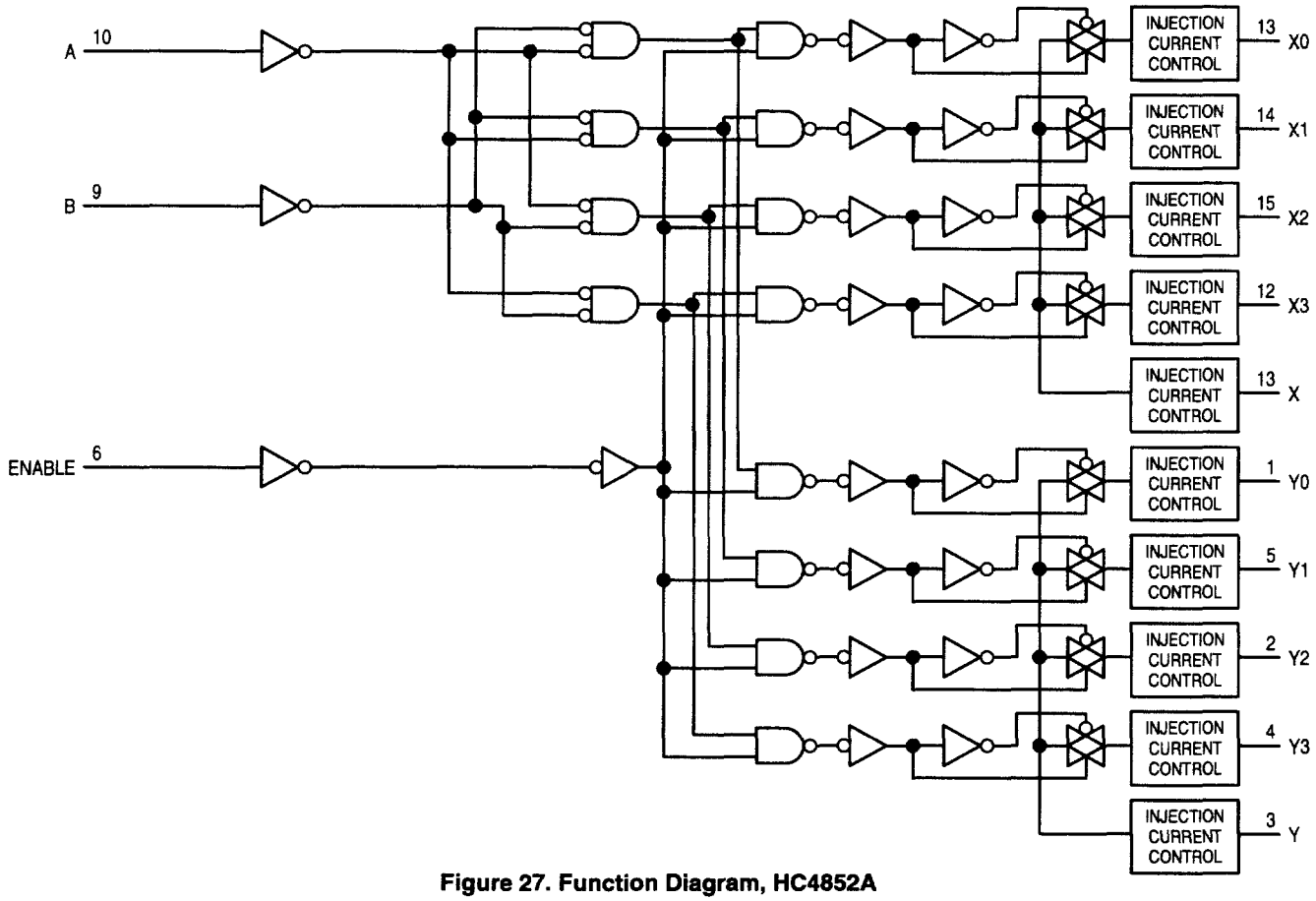


Figure 27. Function Diagram, HC4852A

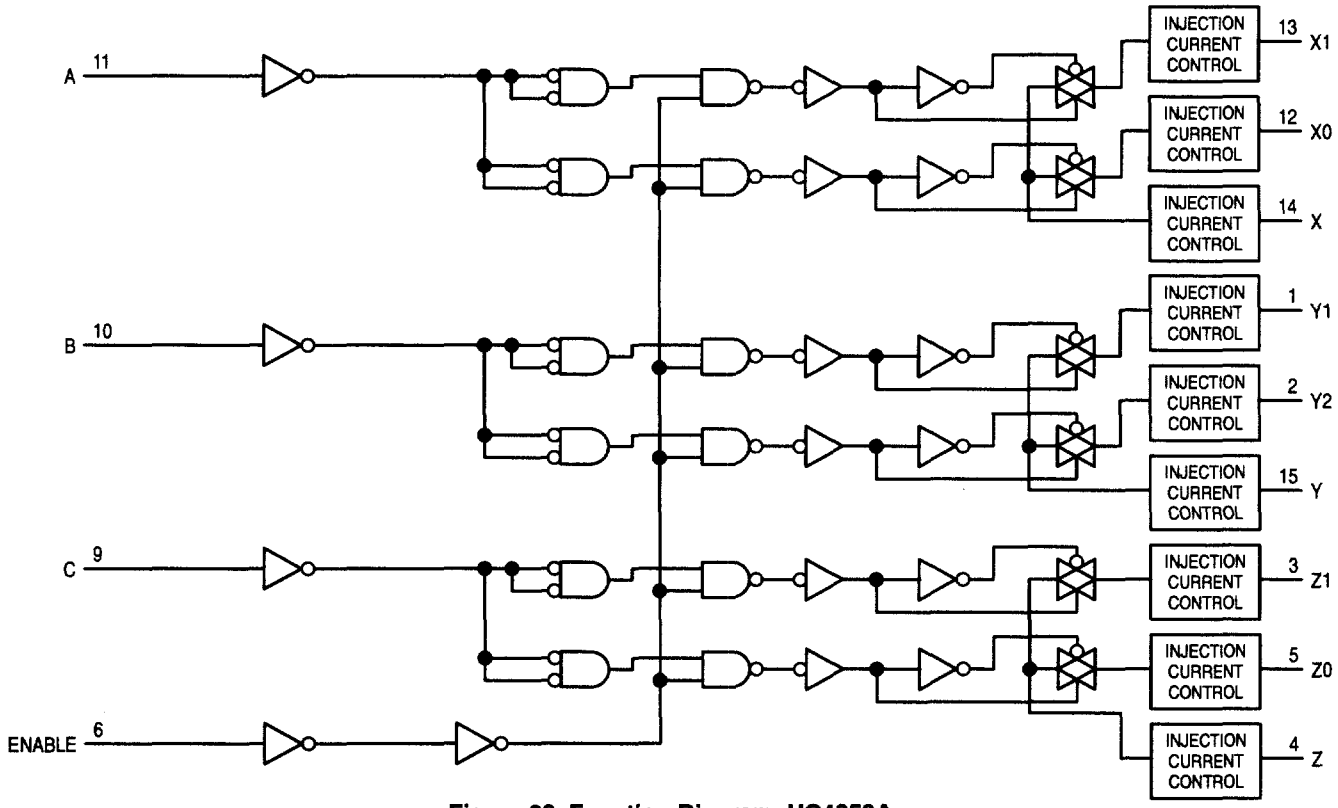
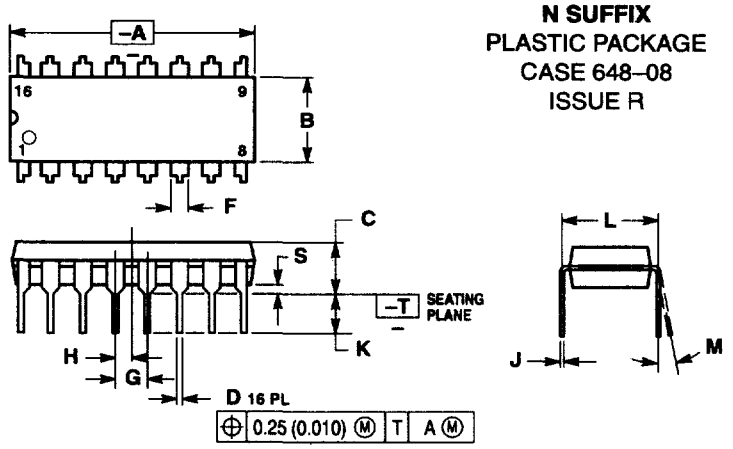


Figure 28. Function Diagram, HC4853A

OUTLINE DIMENSIONS

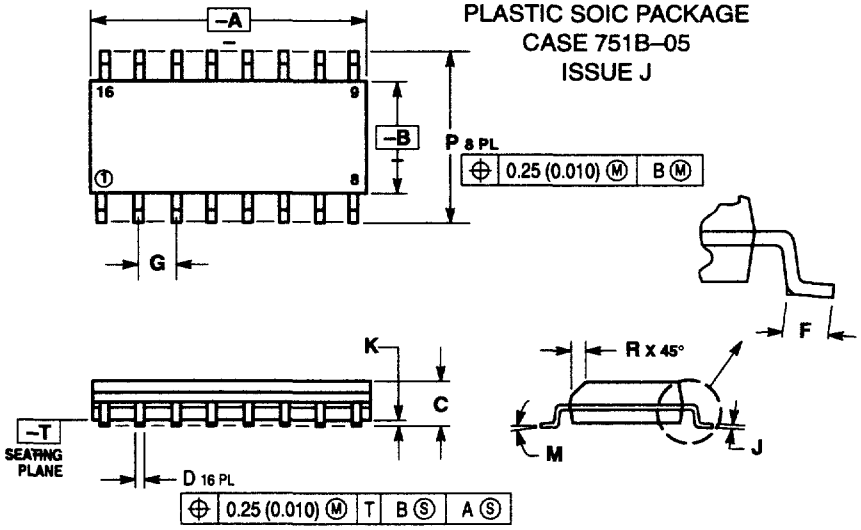
N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

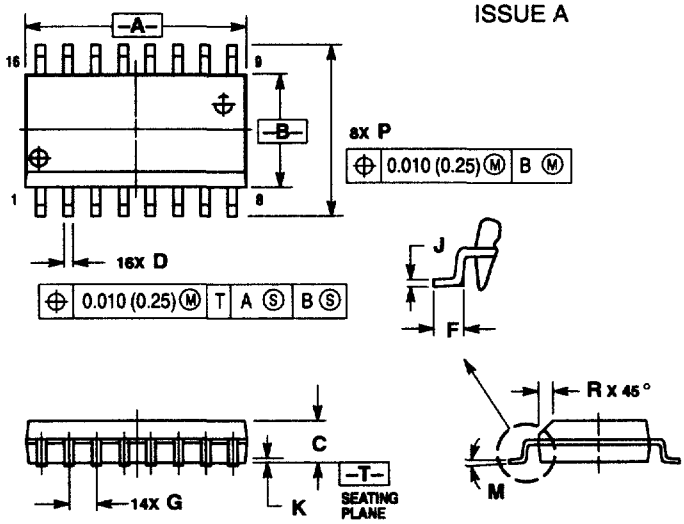
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751G–02
ISSUE A

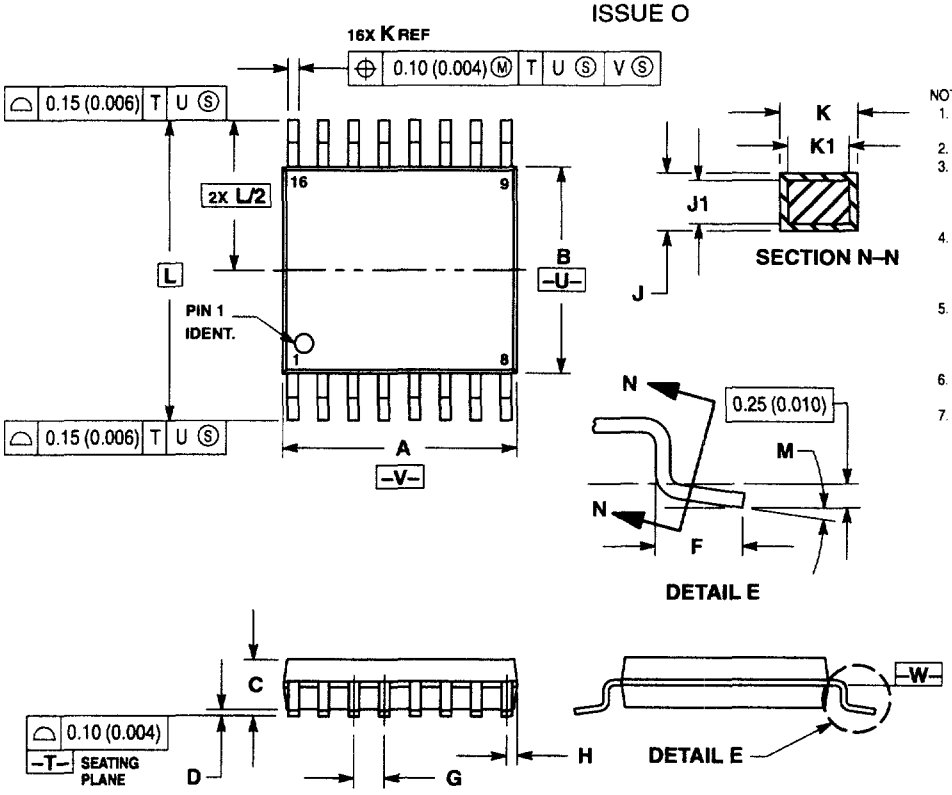


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

OUTLINE DIMENSIONS

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948F–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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