# MOTOROLA

## 8-CHANNEL DATA SELECTOR

The MC14512B is an 8-channel data selector constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

- Diode Protection on All Inputs
- Single Supply Operation
- 3-State Output (Logic "1", Logic "0", High Impedance)
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

## CMOS MSI
(LOW-POWER COMPLEMENTARY MOS)

## 8-CHANNEL DATA SELECTOR

| | |
|---|---|
| **L SUFFIX** | **P SUFFIX** |
| CERAMIC PACKAGE | PLASTIC PACKAGE |
| CASE 620 | CASE 648 |

### ORDERING INFORMATION

A Series: −55°C to +125°C
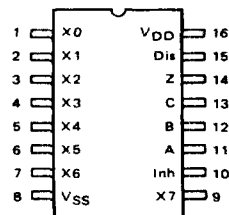MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

### MAXIMUM RATINGS* (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage | −0.5 to +18.0 | V |
| $V_{in}$, $V_{out}$ | Input or Output Voltage (DC or Transient) | −0.5 to $V_{DD}$ +0.5 | V |
| $I_{in}$, $I_{out}$ | Input or Output Current (DC or Transient), per Pin | ±10 | mA |
| $P_D$ | Power Dissipation, per Package† | 500 | mW |
| $T_{stg}$ | Storage Temperature | −65 to +150 | °C |
| $T_L$ | Lead Temperature (8-Second Soldering) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

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### PIN ASSIGNMENT

| | | | |
|---|---|---|---|
| 1 | X0 | $V_{DD}$ | 16 |
| 2 | X1 | Dis | 15 |
| 3 | X2 | Z | 14 |
| 4 | X3 | C | 13 |
| 5 | X4 | B | 12 |
| 6 | X5 | A | 11 |
| 7 | X6 | Inh | 10 |
| 8 | $V_{SS}$ | X7 | 9 |

### TRUTH TABLE

| C | B | A | INHIBIT | DISABLE | Z |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | X0 |
| 0 | 0 | 1 | 0 | 0 | X1 |
| 0 | 1 | 0 | 0 | 0 | X2 |
| 0 | 1 | 1 | 0 | 0 | X3 |
| 1 | 0 | 0 | 0 | 0 | X4 |
| 1 | 0 | 1 | 0 | 0 | X5 |
| 1 | 1 | 0 | 0 | 0 | X6 |
| 1 | 1 | 1 | 0 | 0 | X7 |
| X | X | X | 1 | 0 | 0 |
| X | X | X | X | 1 | High Impedance |

X = Don't Care

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.

# MC14512B

| Characteristic | Symbol | $V_{DD}$ Vdc | $T_{low}$* Min | $T_{low}$* Max | 25°C Min | 25°C Typ # | 25°C Max | $T_{high}$* Min | $T_{high}$* Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage "0" Level | $V_{OL}$ | 5.0 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | Vdc |
| $V_{in}$ = $V_{DD}$ or 0 | | 10 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | |
| | | 15 | — | 0.05 | — | 0 | 0.05 | — | 0.05 | |
| "1" Level | $V_{OH}$ | 5.0 | 4.95 | — | 4.95 | 5.0 | — | 4.95 | — | Vdc |
| $V_{in}$ = 0 or $V_{DD}$ | | 10 | 9.95 | — | 9.95 | 10 | — | 9.95 | — | |
| | | 15 | 14.95 | — | 14.95 | 15 | — | 14.95 | — | |
| Input Voltage "0" Level | $V_{IL}$ | | | | | | | | | Vdc |
| ($V_O$ = 4.5 or 0.5 Vcc) | | 5.0 | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | |
| ($V_O$ = 9.0 or 1.0 Vcc) | | 10 | — | 3.0 | — | 4.50 | 3.0 | — | 3.0 | |
| ($V_O$ = 13.5 or 1.5 Vdc) | | 15 | — | 4.0 | — | 6.75 | 4.0 | — | 4.0 | |
| "1" Level | $V_{IH}$ | | | | | | | | | Vdc |
| ($V_O$ = 0.5 or 4.5 Vcc) | | 5.0 | 3.5 | — | 3.5 | 2.75 | — | 3.5 | — | |
| ($V_O$ = 1.0 or 9.0 Vcc) | | 10 | 7.0 | — | 7.0 | 5.50 | — | 7.0 | — | |
| ($V_O$ = 1.5 or 13.5 Vdc) | | 15 | 11.0 | — | 11.0 | 8.25 | — | 11.0 | — | |
| Output Drive Current (AL Device) | $I_{OH}$ | | | | | | | | | mAdc |
| ($V_{OH}$ = 2.5 Vdc) Source | | 5.0 | −3.0 | — | −2.4 | −4.2 | — | −1.7 | — | |
| ($V_{OH}$ = 4.6 Vdc) | | 5.0 | −0.64 | — | −0.51 | −0.88 | — | −0.36 | — | |
| ($V_{OH}$ = 9.5 Vdc) | | 10 | −1.6 | — | −1.3 | −2.25 | — | −0.9 | — | |
| ($V_{OH}$ = 13.5 Vdc) | | 15 | −4.2 | — | −3.4 | −8.8 | — | −2.4 | — | |
| ($V_{OL}$ = 0.4 Vdc) Sink | $I_{OL}$ | 5.0 | 0.64 | — | 0.51 | 0.88 | — | 0.36 | — | mAdc |
| ($V_{OL}$ = 0.5 Vdc) | | 10 | 1.6 | — | 1.3 | 2.25 | — | 0.9 | — | |
| ($V_{OL}$ = 1.5 Vdc) | | 15 | 4.2 | — | 3.4 | 8.8 | — | 2.4 | — | |
| Output Drive Current (CL/CP Device) | $I_{OH}$ | | | | | | | | | mAdc |
| ($V_{OH}$ = 2.5 Vdc) Source | | 5.0 | −2.5 | — | −2.1 | −4.2 | — | −1.7 | — | |
| ($V_{OH}$ = 4.6 Vdc) | | 5.0 | −0.52 | — | −0.44 | −0.88 | — | −0.36 | — | |
| ($V_{OH}$ = 9.5 Vdc) | | 10 | −1.3 | — | −1.1 | −2.25 | — | −0.9 | — | |
| ($V_{OH}$ = 13.5 Vdc) | | 15 | −3.6 | — | −3.0 | −8.8 | — | −2.4 | — | |
| ($V_{OL}$ = 0.4 Vdc) Sink | $I_{OL}$ | 5.0 | 0.52 | — | 0.44 | 0.88 | — | 0.36 | — | mAdc |
| ($V_{OL}$ = 0.5 Vdc) | | 10 | 1.3 | — | 1.1 | 2.25 | — | 0.9 | — | |
| ($V_{OL}$ = 1.5 Vdc) | | 15 | 3.6 | — | 3.0 | 8.8 | — | 2.4 | — | |
| Input Current (AL Device) | $I_{in}$ | 15 | — | ±0.1 | — | ±0.00001 | ±0.1 | — | ±1.0 | $\mu$Adc |
| Input Current (CL/CP Device) | $I_{in}$ | 15 | — | ±0.3 | — | ±0.00001 | ±0.3 | — | ±1.0 | $\mu$Adc |
| Input Capacitance ($V_{in}$ = 0) | $C_{in}$ | — | — | — | — | 5.0 | 7.5 | — | — | pF |
| Quiescent Current (AL Device) (Per Package) | $I_{DD}$ | 5.0 | — | 5.0 | — | 0.005 | 5.0 | — | 150 | $\mu$Adc |
| | | 10 | — | 10 | — | 0.010 | 10 | — | 300 | |
| | | 15 | — | 20 | — | 0.015 | 20 | — | 600 | |
| Quiescent Current (CL/CP Device) (Per Package) | $I_{DD}$ | 5.0 | — | 20 | — | 0.005 | 20 | — | 150 | $\mu$Adc |
| | | 10 | — | 40 | — | 0.010 | 40 | — | 300 | |
| | | 15 | — | 80 | — | 0.015 | 80 | — | 600 | |
| Total Supply Current**† (Dynamic plus Quiescent, Per Package) ($C_L$ = 50 pF on all outputs, all buffers switching) | $I_T$ | 5.0 | $I_T$ = (0.8 $\mu$A/kHz) f + $I_{DD}$ | | | | | | | $\mu$Adc |
| | | 10 | $I_T$ = (1.6 $\mu$A/kHz) f + $I_{DD}$ | | | | | | | |
| | | 15 | $I_T$ = (2.4 $\mu$A/kHz) f + $I_{DD}$ | | | | | | | |
| Three-State Leakage Current (AL Device) | $I_{TL}$ | 15 | — | ±0.1 | — | ±0.00001 | ±0.1 | — | ±3.0 | $\mu$Adc |
| Three-State Leakage Current (CL/CP Device) | $I_{TL}$ | 15 | — | ±1.0 | — | ±0.00001 | ±1.0 | — | ±7.5 | $\mu$Adc |

*$T_{low}$ = −55°C for AL Device, −40°C for CL/CP Device.
$T_{high}$ = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ V f k}$$

where: $I_T$ is in $\mu$A (per package), $C_L$ in pF. V = ($V_{DD}$ − $V_{SS}$) in volts, f in kHz is input frequency, and k = 0.001.

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## SWITCHING CHARACTERISTICS ($C_L = 50$ pF, $T_A = 25°C$. See Figure 1)

| Characteristic | Symbol | $V_{DD}$ | All Types | | Unit |
|---|---|---|---|---|---|
| | | | Typ # | Max | |
| Output Rise and Fall Time | $t_{TLH}$, | | | | ns |
| $t_{TLH}$, $t_{THL} = (1.5$ ns/pF$) C_L + 25$ ns | $t_{THL}$ | 5.0 | 100 | 200 | |
| $t_{TLH}$, $t_{THL} = (0.75$ ns/pF$) C_L + 12.5$ ns | | 10 | 50 | 100 | |
| $t_{TLH}$, $t_{THL} = (0.55$ ns/pF$) C_L + 9.5$ ns | | 15 | 40 | 80 | |
| Propagation Delay Time (Figure 2) | $t_{PLH}$ | | | | ns |
| Inhibit, Control, or Data to Z | | 5.0 | 330 | 650 | |
| | | 10 | 125 | 250 | |
| | | 15 | 85 | 170 | |
| Propagation Delay Time (Figure 2) | $t_{PHL}$ | | | | ns |
| Inhibit, Control, or Data to Z | | 5.0 | 330 | 650 | |
| | | 10 | 125 | 250 | |
| | | 15 | 85 | 170 | |
| 3-State Output Delay Times (Figure 3) | $t_{PHZ}$, $t_{PLZ}$, | 5.0 | 60 | 150 | ns |
| "1" or "0" to High Z, and | $t_{PZH}$, $t_{PZL}$ | 10 | 35 | 100 | |
| High Z to "1" or "0" | | 15 | 30 | 75 | |

*The formulas given are for the typical characteristics only at 25°C

#Data labelled "Typ" is not to be used for design purposes but is
 intended as an indication of the IC's potential performance

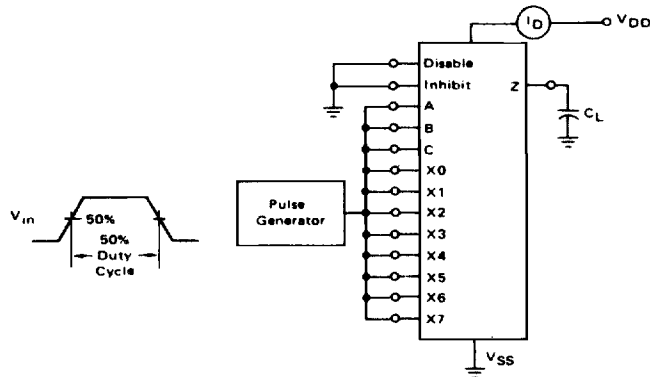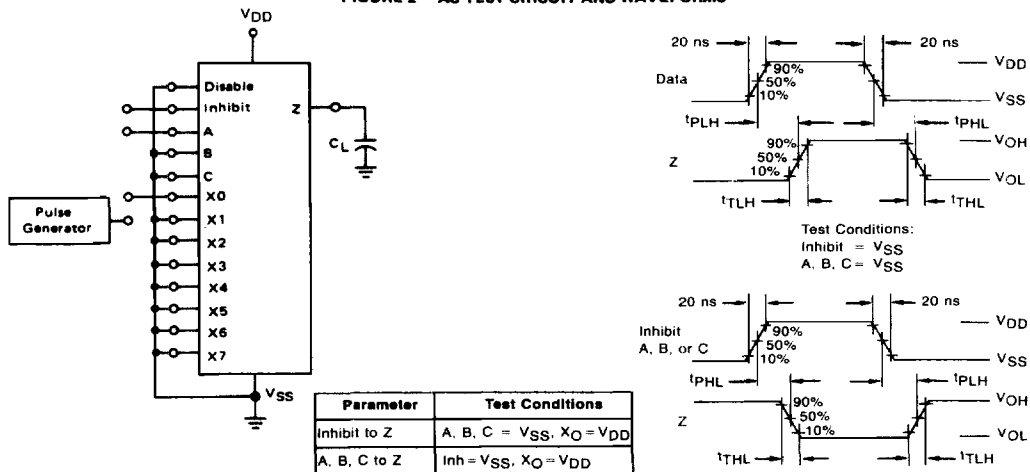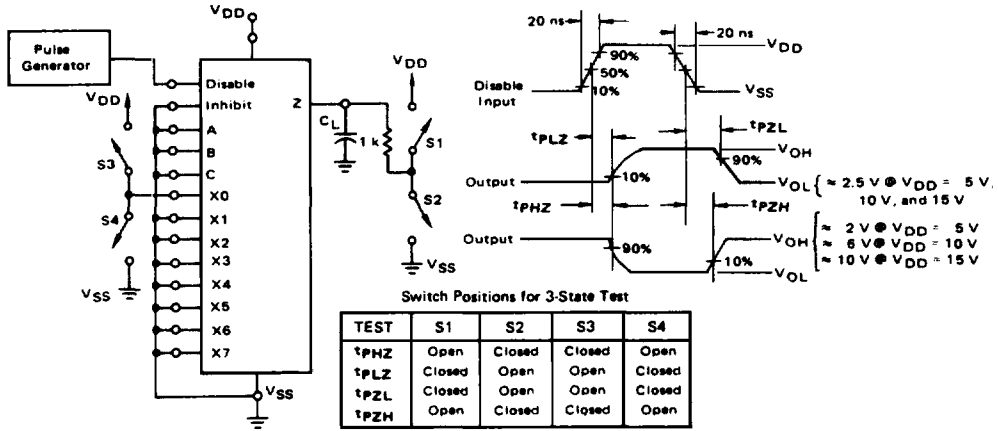### FIGURE 1 — POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



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### FIGURE 2 — AC TEST CIRCUIT AND WAVEFORMS



| Parameter | Test Conditions |
|---|---|
| Inhibit to Z | A, B, C = $V_{SS}$, $X_O = V_{DD}$ |
| A, B, C to Z | Inh = $V_{SS}$, $X_O = V_{DD}$ |

# MC14512B

FIGURE 3 – 3-STATE AC TEST CIRCUIT AND WAVEFORM

## LOGIC DIAGRAM



Switch Positions for 3-State Test

| TEST | S1 | S2 | S3 | S4 |
|------|-----|--------|--------|--------|
| $t_{PHZ}$ | Open | Closed | Closed | Open |
| $t_{PLZ}$ | Closed | Open | Open | Closed |
| $t_{PZL}$ | Closed | Open | Open | Closed |
| $t_{PZH}$ | Open | Closed | Closed | Open |

### 3-STATE MODE OF OPERATION

Output terminals of several MC14512B 8-Bit Data Selectors can be connected to a single data bus as shown. One MC14512B is selected by the 3-state control, and the remaining devices are disabled into a high -impedance "off" state. The number of 8-bit data selectors, N, that may be connected to a bus line is determined from the output drive current, $I_{OD}$, 3-state or disable output leakage current, $I_{TL}$, and the load current, $I_L$, required to drive the bus line (including fanout to other device inputs), and can be calculated by:

$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic state of the bus line.

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