MP3900

High Efficiency Boost Controller

The Future of Analog IC Technology

DESCRIPTION

The MP3900 is a boost controller that drives an external MOSFET capable of handling 10A current. It has an operational current of typically 180µA and can accommodate off-line, Telecom and non-isolated applications. Internal undervoltage lockout, slope compensation and peak current limiting are all provided to minimize the external component count. In a boost application, with an output voltage of less than 30V, the current sense pin can connect directly to the drain of the external switch. This eliminates the requirement for an additional current sensing element and its associated efficiency loss.

While designed for boost applications, the MP3900 can also be used for other topologies including Forward, Flyback and Sepic. The 10V gate driver voltage minimizes the power loss of the external MOSFET while allowing the use of a wide variety of standard threshold devices.

The MP3900 is available in 8-pin MSOP and SOIC packages.

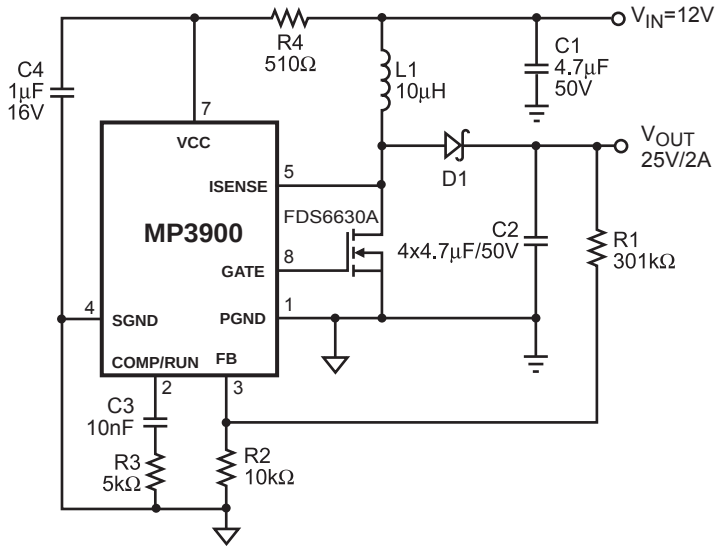
FEATURES

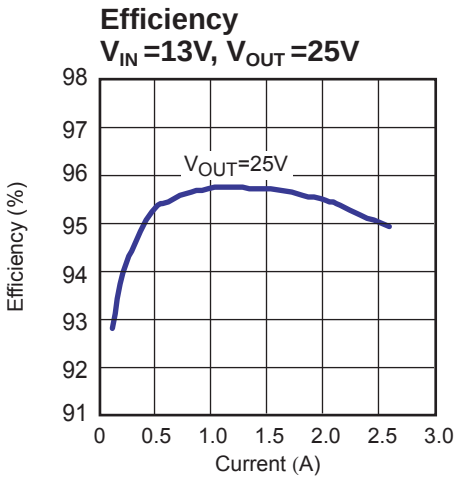
- Current Mode Control
- 10V MOSFET Gate Driver
- Undervoltage Lockout
- Internal Soft-Start
- Cycle-by-Cycle Current Limiting
- Slope Current Compensation
- Lossless Current Sense (V_{ISENSE}<30V)
- 10µA Shutdown Current
- 180µA Quiescent Current
- 330KHz Constant Frequency Operation
- Applicable to Boost, SEPIC, Flyback and Forward Topologies
- Available in an 8-Pin MSOP/SOIC Packages

APPLICATIONS

- TV CCFL Power Generation
- Telecom Isolated Power
- Brick Modules
- Off-line Controller

TYPICAL APPLICATION



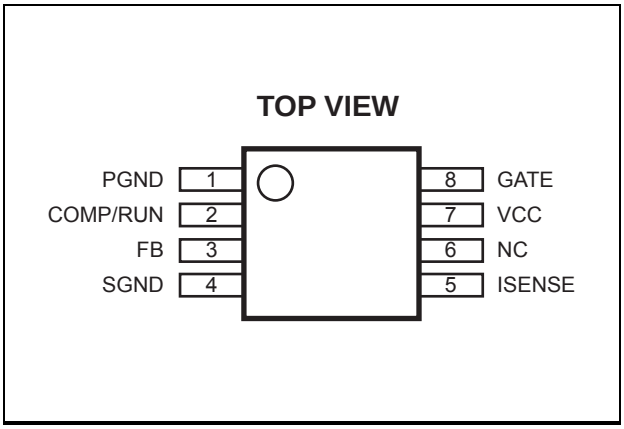


ORDERING INFORMATION

Part Number*	Package	Top Marking	Temperature
MP3900DK	MSOP8	3900D	–40°C to +85°C
MP3900DS	SOIC8	MP3900DS	

* For Tape & Reel, add suffix –Z (e.g. MP3900DK–Z). For RoHS compliant packaging, add suffix –LF (e.g. MP3900DK–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

VCC .....–0.3V to +12V
VCC Maximum Current..... 30mA
ISENSE.....–0.3V to +30V
FB .....–0.3V to +5V
COMP/RUN .....–0.3V to +3V
Continuous Power Dissipation (T_A = +25°C) (2)
MSOP8 ..... 0.67W
SOIC8 ..... 1.1W
Junction Temperature.....125°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

VCC Current .....1mA to 25mA
Operating Temperature..... –40°C to +85°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
MSOP8	150	65	°C/W
SOIC8	90	45	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} = 10V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VCC Undervoltage Lockout (VCC UVLO Turn_On Threshold)		Internal Divider (I_Q)	8.6	8.9	9.2	V
VCC On/Off Voltage Hysteresis (VCC UVLO Turn_On/Off Hysteresis)			2.0	2.3		V
COMP Run Threshold			0.120	0.160	0.200	V
Shutdown Current	I_S	COMP/RUN = 0V, V_{IN} = 8V		8	20	µA
Quiescent Current (Operation)	I_Q	Output not switching, V_{FB} = 1V, V_{CC} = 9V		180	280	µA
Gate Driver Impedance (Sourcing)		V_{CC} = 10V, V_{GATE} = 5V		16		Ω
Gate Driver Impedance (Sinking)		V_{CC} = 10V, I_{GATE} = 5mA		4.0	6.0	Ω
Error Amplifier Transconductance		V_{FB} connected to $V_{COMP/RUN}$. Force ±10µA to $V_{COMP/RUN}$.	0.26	0.36	0.46	mA/V
Maximum Comp Current		Sourcing and Sinking		40		µA
EA Translator Gain (5)	A_{ET}		0.28	0.32	0.36	V/V
Switching Frequency	f_S		270	330	390	KHz
Thermal Shutdown (5)				150		°C
Maximum Duty Cycle			77	80	83	%
Minimum On Time	t_{ON}			110	150	ns
ISENSE Limit			175	200	225	mV
FB Voltage	V_{FB}		0.790	0.816	0.840	V
FB Bias Current	I_{FB}	Current flowing out of part		50		nA
ISENSE Bias Current (5)	I_{SENSE}	Current flowing out of part		50		nA

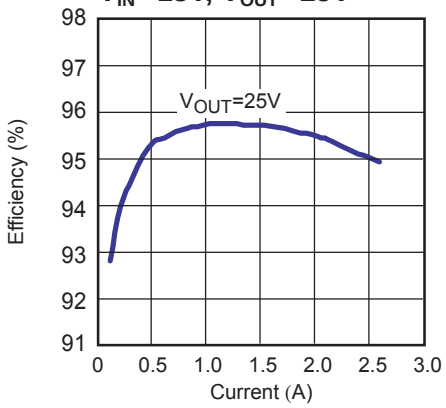
Note:

5) Guaranteed by design.

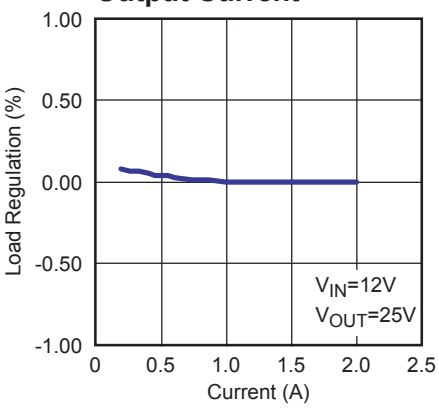
TYPICAL PERFORMANCE CHARACTERISITCS

V_{IN} = 12V, C1 = 4.7µF, C2 = 4x4.7µF, L = 10µH and T_A = +25°C, unless otherwise noted.

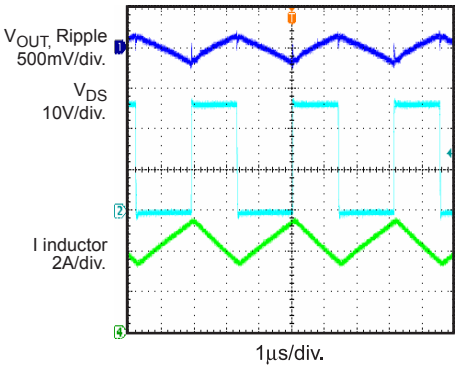
Efficiency
V_{IN} =13V, V_{OUT} =25V



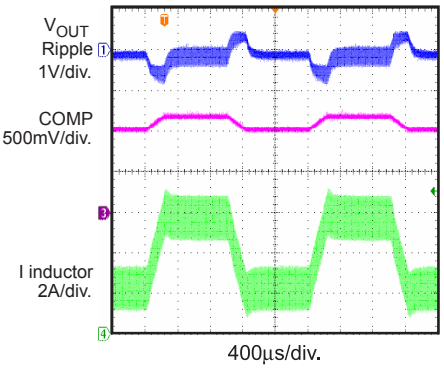
Load Regulation vs. Output Current



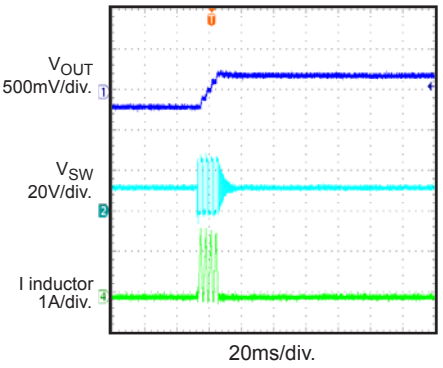
Switching Waveform
V_{IN} = 12V, V_{OUT} = 25V, I_O = 2A, f_{SW} = 322.1kHz



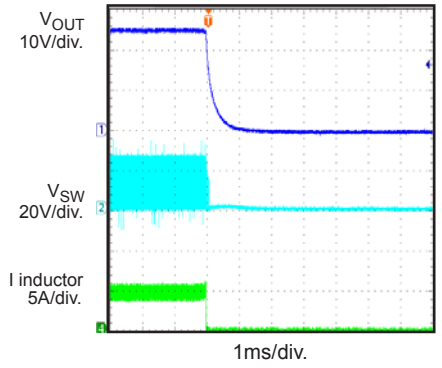
Load Transient Response
V_{IN} = 12V, V_{OUT} = 25V, I_O = 1A to 2.5A



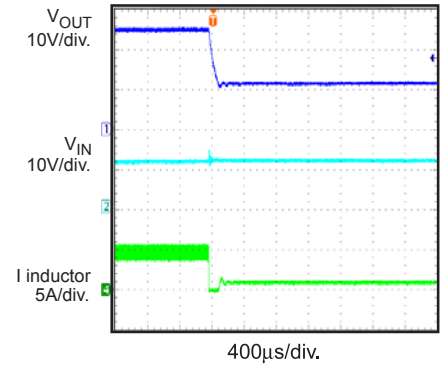
No Load Waveform
V_{IN} = 12V, V_{OUT} = 25V, I_O = 0A



Shut Down with Input Voltage
V_{IN} = 12V, V_{OUT} = 25V, I_O = 2A



Shut Down with COMP
V_{IN} = 12V, V_{OUT} = 25V, I_O = 2A



PIN FUNCTIONS

Pin #	Name	Description
1	PGND	Power Ground Pin which is gate driver return.
2	COMP/RUN	Enable and Compensation. An internal 0.5μA current charges the pin components above the 0.14V Run threshold to turn on the part. Below this threshold, the part is shut down, drawing typically 3μA from V_{CC}.
3	FB	Feedback forces this pin voltage to the 0.8V internal reference potential. Do not allow this pin to rise above 1.2V in the application. If this pin is higher than 1.3V, the IC will go into test mode and turn off the gate driver.
4	SGND	Signal Ground. The SGND and PGND pins should be tied together and returned directly to the ground connection side of the output capacitor.
5	ISENSE	Current Sense. An internal clamp will limit this pin voltage to typically 36V. Do not connect this pin directly to the drain of the external MOSFET if the voltage swing exceeds 30V in the particular application. During normal operation, this pin will sense the voltage across the external MOSFET or sense resistor if one is used, limiting the peak inductor current on a cycle-by-cycle basis.
6	NC	No Connect.
7	VCC	Input Supply. Decouple this pin as close as possible to the SGND pin.
8	GATE	This pin drives the external power MOSFET device.

OPERATION

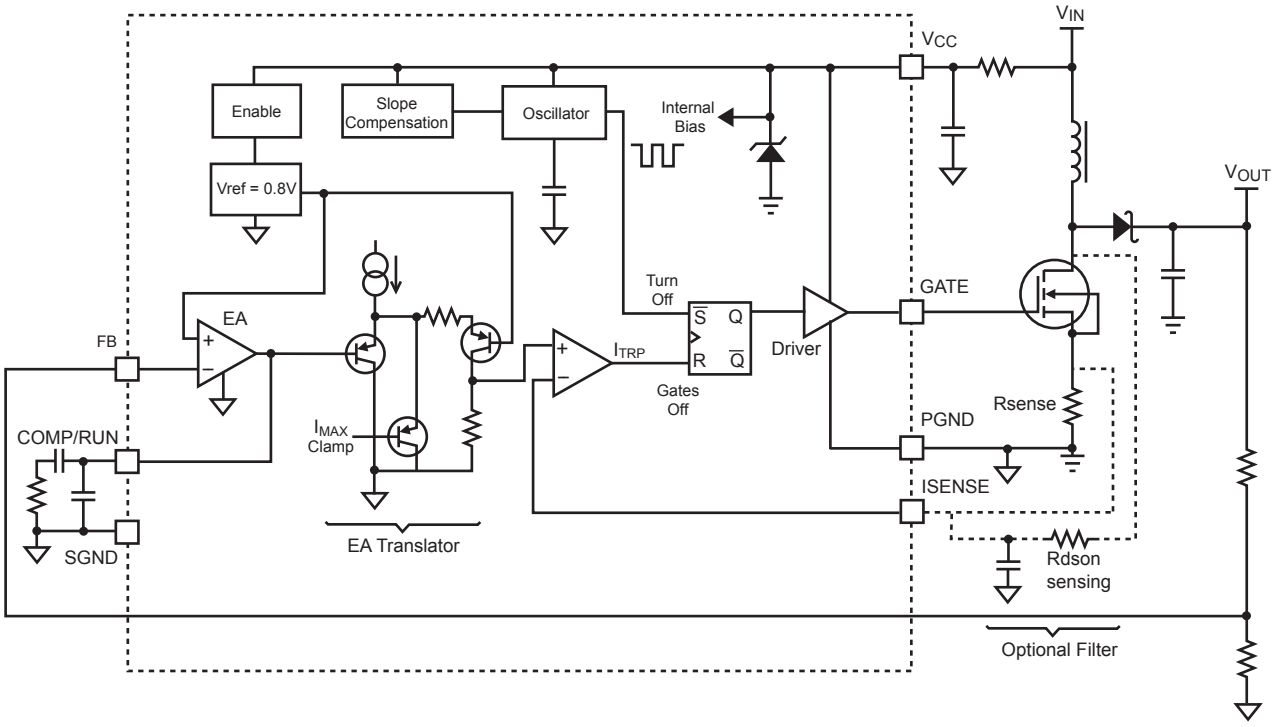


Figure 1—Functional Block Diagram

The MP3900 uses a constant frequency, peak current mode architecture to regulate the feedback voltage. The operation of the MP3900 can be understood with the block diagram of Figure 1.

At the beginning of each cycle the external N-Channel MOSFET is turned on, forcing the current in the inductor to increase. The current through the FET can either be sensed through a sensing resistor or across the external FET directly. This voltage is then compared to a voltage related to the COMP/RUN node voltage. The voltage at the COMP/RUN pin is an amplified voltage of the difference between the 0.8V reference and the feedback node voltage.

When the voltage at the ISENSE node rises above the voltage set by the COMP/RUN pin, the external FET is turned off. The inductor current then flows to the output capacitor through the Schottky diode. The inductor current is controlled by the COMP/RUN voltage, which itself is controlled by the output voltage. The peak inductor current is internally limited by the I_{MAX} clamp voltage that limits the voltage applied to the I_{TRP} comparator input.

Thus the output voltage controls the inductor current to satisfy the load. This current mode architecture improves transient response and control loop stability over a voltage mode architecture.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

Set the output voltage by selecting the resistive voltage divider ratio. If we use 10kΩ for the low-side resistor (R2) of the voltage divider, we can determine the high-side resistor (R1) by the equation:

$$R1 = \frac{R2 \times (V_{OUT} - V_{REF})}{V_{REF}}$$

Where V_{OUT} is the output voltage.

For R2=10kΩ, V_{OUT}=25V and V_{REF}=0.8V, then R1=301kΩ.

Selecting the Inductor and Current Sensing Resistor

The inductor is required to transfer the energy between the input source and the output capacitors. A larger value inductor results in less ripple current that results in lower peak inductor current, and therefore reduces the stress on the power MOSFET. However, the larger value inductor has a larger physical size, higher series resistance, and/or lower saturation current.

A good rule of thumb is to allow the peak-to-peak ripple current to be approximately 30-50% of the maximum input current. Make sure that the peak inductor current is below 80% of the IC's maximum current limit at the operating duty cycle to prevent loss of regulation. Make sure that the inductor does not saturate under the worst-case load transient and startup conditions. The required inductance value can be calculated by :

$$L = \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{V_{OUT} \times f_{SW} \times \Delta I}$$

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{LOAD(MAX)}}{V_{IN(MIN)} \times \eta}$$

$$\Delta I = (30\% - 50\%) I_{IN(MAX)}$$

Where $I_{LOAD(MAX)}$ is the maximum load current, ΔI is the peak-to-peak inductor ripple current and η is the efficiency. For a typical design, boost converter efficiency can reach 85%~95%.

For $V_{IN(MIN)}$=10V, V_{OUT}=25V, $I_{LOAD(MAX)}$=2A, the ripple percentage being 30%, η=95% and f_{SW}=330kHz, then L=10μH. In this case, use a 8.8μH inductor (i.e. Sumida CDRH127/LDNP-100MC).

The switch current is usually used for the peak current mode control. In order to avoid hitting the current limit, the voltage across the sensing resistor R_{SENSE} should be less than 80% of the worst case current limit voltage, 200mV.

$$R_{SENSE} = \frac{0.8 \times 0.2}{I_{L(PEAK)}}$$

Where $I_{L(PEAK)}$ is the peak value of the inductor current.

For $I_{L(PEAK)}$=5.3A, R_{SENSE}=30mΩ.

In cases where the $R_{DS(ON)}$ of the power MOSFET is used as the sensing resistor, be sure that the $R_{DS(ON)}$ is lower than the value calculated above, 30mΩ

Another factor to take into consideration is the temperature coefficient of the MOSFET $R_{DS(ON)}$. As the temperature increases, the $R_{DS(ON)}$ also increases.. Device vendors will usually provide an $R_{DS(ON)}$ vs. temperature curve and the temperature coefficient in the datasheet. Generally, the MOSFET on resistance will double from 25°C to 125°C.

Selecting the Input Capacitor

An input capacitor (C1) is required to supply the AC ripple current to the inductor, while limiting noise at the input source. A low ESR capacitor is required to keep the noise to the IC at a minimum. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice.

The capacitance can be calculated as:

$$C_1 \approx \frac{\Delta I}{8 \times \Delta V_{IN(RIPPLE)} \times f_{SW}}$$

Where ΔI is the peak-to-peak inductor ripple current and $\Delta V_{IN(RIPPLE)}$ is the input voltage ripple. When using ceramic capacitors, take into account the vendor specified voltage and temperature coefficients for the particular dielectric being used.

For example, 2.2uF capacitance is sufficient to achieve less then 1% input voltage ripple. Meanwhile, it requires an adequate ripple current rating. Use a capacitor with RMS current rating greater than the inductor ripple current (see Selecting the Inductor to determine the inductor ripple current).

In addition, a smaller high quality ceramic 0.1μF~1μF capacitor may be placed to absorb the high frequency noise. If using this technique, it is recommended that the larger capacitor be a tantalum or electrolytic type.

Selecting the Output Capacitor

Typically, a boost converter has significant output voltage ripple because the current through the output diode is discontinuous. During the diode off state, all of the load current is supplied by the output capacitor.

Low ESR capacitors are preferred to keep the output voltage ripple to a minimum. The characteristics of the output capacitor also affect the stability of the regulation control system. Ceramic, tantalum or low ESR electrolytic capacitors are recommended. In the case of ceramic capacitors, the impedance of the capacitor at the switching frequency is dominated by the capacitance, and so the output voltage ripple is mostly independent of the ESR. The output voltage ripple is estimated to be:

$$V_{RIPPLE} \approx \frac{\left(1-\frac{V_{IN}}{V_{OUT}}\right)\times I_{LOAD}}{C2\times f_{SW}}$$

Where V_{RIPPLE} is the output ripple voltage, V_{IN} and V_{OUT} are the DC input and output voltages respectively, I_{LOAD} is the load current, f_{SW} is the switching frequency and C2 is the output capacitor.

In the case of tantalum or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency. Therefore, the output ripple is calculated as:

$$V_{RIPPLE(pk\_pk)} \approx \frac{I_{LOAD}\times R_{ESR}\times V_{OUT}}{V_{IN}}$$

Where R_{ESR} is the equivalent series resistance of the output capacitors.

For the application shown in page 1, use ceramic capacitor as an example. For $V_{IN(MIN)}$=10V, V_{OUT}=25V, $I_{LOAD(MAX)}$=2A, and V_{RIPPLE}=1% of the output voltage, the capacitance C_2=14.5μF. Please note that the ceramic capacitance could dramatically decrease as the voltage across the capacitor increases. As a result, larger capacitance is recommended. In this example, place four 4.7μF ceramic capacitors in parallel. The voltage rating is also chosen as 50V.

In the meantime, the RMS current rating of the output capacitor needs to be sufficient to handle the large ripple current. The RMS current is given by:

$$I_{RIPPLE(RMS)} \approx \sqrt{\left(I_{IN(MAX)}^2 - 2\times I_{LOAD}\times I_{IN(MAX)}\right)\times\frac{V_{IN}}{V_{OUT}} + I_{LOAD}^2}$$

$$I_{RIPPLE(RMS)} \approx \sqrt{D(1-D)\times I_{INMAX}^2} < 0.5\times I_{INMAX}$$

For $I_{IN(MAX)}$=5.3A, I_{LOAD}=2A, V_{IN}=12V and V_{OUT}=25V, $I_{RIPPLE(RMS)}$=2.64A. Make sure that the output capacitor can handle such an RMS current.

In addition, a smaller high quality ceramic 0.1μF~1uF capacitor needs to be placed at the output to absorb the high frequency noise during the commutation between the power MOSFET and the output diode. Basically, the high frequency noise is caused by the parasitic inductance of the trace and the parasitic capacitors of devices. The ceramic capacitor should be placed as close as possible to the power MOSFET and output diode in order to minimize the parasitic inductance and maximize the absorption.

Selecting the Power MOSFET

The MP3900 is capable of driving a wide variety of N-Channel power MOSFETS. The critical parameters of selection of a MOSFET are:

1. Maximum drain to source voltage, $V_{DS(MAX)}$
2. Maximum current, $I_{D(MAX)}$
3. On-resistance, $R_{DS(ON)}$
4. Gate source charge Q_{GS} and gate drain charge Q_{GD}
5. Total gate charge, Q_G

Ideally, the off-state voltage across the MOSFET is equal to the output voltage. Considering the voltage spike when it turns off, $V_{DS(MAX)}$ should be greater than 1.5 times of the output voltage.

The maximum current through the power MOSFET happens when the input voltage is minimum and the output power is maximum. The maximum RMS current through the MOSFET is given by

$$I_{RMS(MAX)} = I_{IN(MAX)} \times \sqrt{D_{MAX}}$$

Where:

$$D_{MAX} \approx \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}}$$

The current rating of the MOSFET should be greater than 1.5 times $I_{RMS,}$

The on resistance of the MOSFET determines the conduction loss, which is given by:

$$P_{cond} = I_{RMS}{}^2 \times R_{DS(on)} \times k$$

Where k is the temperature coefficient of the MOSFET. If the $R_{DS(ON)}$ of the MOSFET is used as the current sensing resistor, make sure the voltage drop across the device does not exceed the current limit value of 190mV.

The switching loss is related to Q_{GD} and Q_{GS1} which determine the commutation time. Q_{GS1} is the charge between the threshold voltage and the plateau voltage when a driver charges the gate, which can be read in the chart of V_{GS} vs. Q_G of the MOSFET datasheet. Q_{GD} is the charge during the plateau voltage. These two parameters are needed to estimate the turn on and turn off loss.

$$P_{SW} = \frac{Q_{GS1} \times R_G}{V_{DR} - V_{TH}} \times V_{DS} \times I_{IN} \times f_{SW} + \frac{Q_{GD} \times R_G}{V_{DR} - V_{PLT}} \times V_{DS} \times I_{IN} \times f_{SW}$$

Where V_{TH} is the threshold voltage, V_{PLT} is the plateau voltage, R_G is the gate resistance, V_{DS} is the drain-source voltage. Please note that the switching loss is the most difficult part in the loss estimation. The formula above provides a simple physical expression. If more accurate estimation is required, the expressions will be much more complex.

For extended knowledge of the power loss estimation, readers should refer to the book "Power MOSFET Theory and Applications" written by Duncan A. Grant and John Gowar.

The total gate charge, Q_G, is used to calculate the gate drive loss. The expression is

$$P_{DR} = Q_G \times V_{DR} \times f_{SW}$$

where V_{DR} is the drive voltage.

For the application in page 1, a FDS6630 or equivalent MOSFET is chosen. Read from the datasheet: $R_{DS(ON)}$=28mΩ, k = 0.5, Q_{GD}=0.9nC, Q_{GS1}=1nC, V_{TH}=1.7V, V_{PLT}=3V and Q_G=5nC @ 10V. The MP3900 has its gate driving resistance of around 20Ω at V_{DR}=10V and V_{GATE} = 5V.

Based on the loss calculation above, the conduction loss is around 0.629W. The switching loss is around 0.171W, and the gate drive loss is 0.015W.

Selecting the Output Diode

The output rectifier diode supplies current to the inductor when the MOSFET is off. To reduce losses due to diode forward voltage and recovery time, use a Schottky diode. The diode should be rated for a reverse voltage greater than the output voltage used. Considering the voltage spike during the commutation period, the voltage rating of the diode should be set as 1.5 times the output voltage. For high output voltages (150V or above), a Schottky diode might not be practical. A high-speed ultra-fast recovery silicon rectifier is recommended.

Observation of the boost converter circuit shows that the average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The average current rating must be greater than 1.5 times of the maximum load current, and the peak current rating must be greater than the peak inductor current.

For the application in page 1, a Vishay SS16 Schottky diode or equivalent part is chosen.

Boost Converter: Compensation Design

The output of the transconductance error amplifier (COMP) is used to compensate the regulation control system. The system uses two poles and one zero to stabilize the control loop. The poles are f_{P1}, which is set by the output capacitor (C2) and load resistance and f_{P2}, which starts from origin. The zero (f_{Z1}) is set by the compensation capacitor (C3) and the compensation resistor (R3). These parameters are determined by the equations:

$$f_{P1} = \frac{1}{\pi \times C2 \times R_{LOAD}}$$

$$f_{Z1} = \frac{1}{2 \times \pi \times C3 \times R3}$$

Where R_{LOAD} is the load resistance.

The DC mid-band loop gain is:

$$A_{VDC} = \frac{0.5 \times G_{EA} \times V_{IN} \times R_{LOAD} \times V_{REF} \times R3 \times A_{ET}}{V_{OUT}^2 \times R_{SENSE}}$$

where V_{REF} is the voltage reference, 0.8V. A_{ET} is the gain of error amplifier translator and G_{EA} is the error amplifier transconductance.

The ESR zero in this example locates at very high frequency. Therefore, it is not taken into design consideration.

There is also a right-half-plane zero (f_{RHPZ}) that exists in continuous conduction mode (inductor current does not drop to zero on each cycle) step-up converters. The frequency of the right half plane zero is:

$$f_{RHPZ} = \frac{V_{IN}^2 \times R_{LOAD}}{2 \times \pi \times L \times V_{OUT}^2}$$

The right-half-plane zero increases the gain and reduces the phase simultaneously, which results in smaller phase margin and gain margin. The worst case happens at the condition of minimum input voltage and maximum output power.

In order to achieve system stability, f_{z1} is placed close to f_{P1} to cancel the pole. R3 is adjusted to change the voltage gain. Make sure the bandwidth is about 1/10 of the lower one of the ESR zero and the right-half-plane zero.

$$\frac{1}{\pi \times C2 \times R_{LOAD}} = \frac{1}{2 \times \pi \times C3 \times R3}$$

$$R3 = \frac{V_{OUT}^2 \times 2 \times \pi \times C2 \times f_c \times R_{SENSE}}{G_{EA} \times V_{REF} \times V_{IN} \times A_{ET}}$$

Based on these equations, R3 and C3 can be solved.

For the application in page 1, f_{p1} = 1.35KHz, ESR zero is much higher than the switching frequency and f_{RHPZ}=45.8KHz. Set f_{z1} to 3.18KHz and make the crossover frequency 8.5kHz, then R3=5kΩ and C3=10nF. Choose 5kΩ and 10nF.

In cases where the ESR zero is in a relatively low frequency region and results in insufficient gain margin, an optional capacitor (C5) (shown in Figure 2) should be added. Then a pole, formed by C5 and R3, should be placed at the ESR zero to cancel the adverse effect.

$$C5 = \frac{1}{2 \times \pi \times R3 \times f_{ESRz}}$$

Layout Consideration

High frequency switching regulators require very careful layout for stable operation and low noise. Keep the high current path as short as possible between the MOSFET drain, output diode, output capacitor and GND pin for minimal noise and ringing. The V_{CC} capacitor must be placed close to the VCC pin for best decoupling. All feedback components must be kept close to the FB pin to prevent noise injection on the FB pin trace. The ground return of the input and output capacitors should be tied closed to the GND pin. See the MP3900 demo board layout for reference.

TYPICAL APPLICATION CIRCUIT

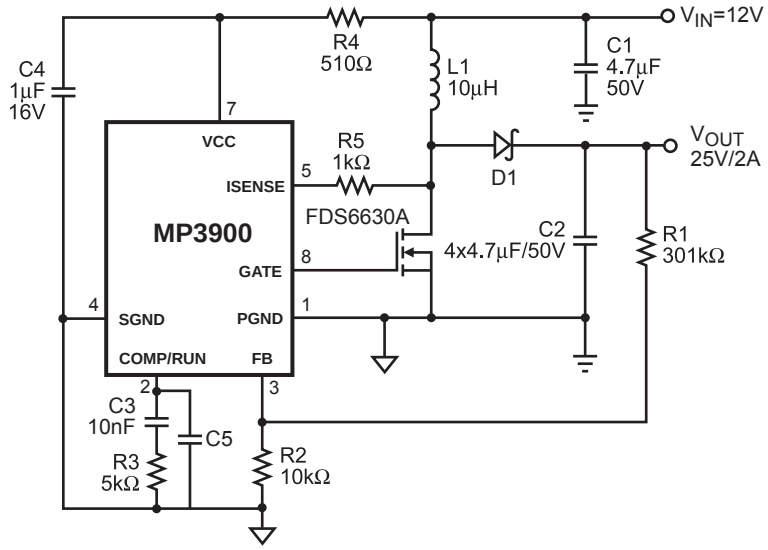
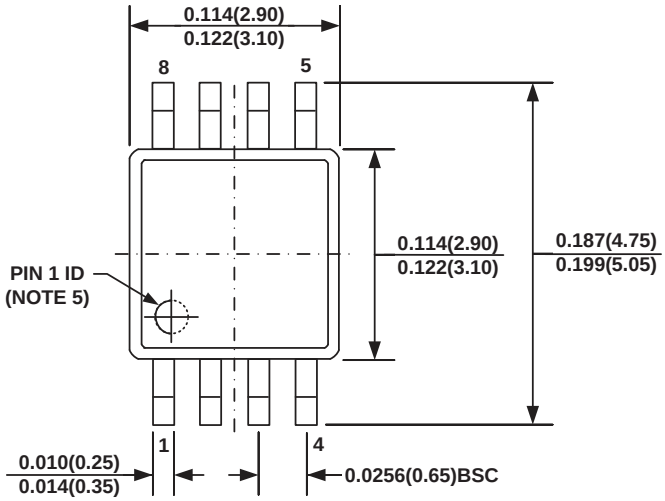


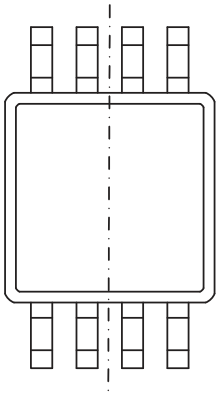
Figure 2—MP3900 for Boost Controller Application

PACKAGE INFORMATION

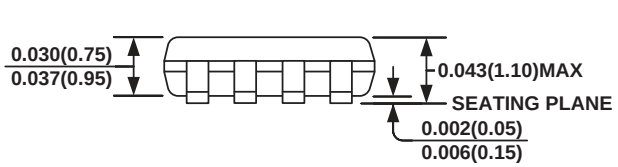
MSOP8



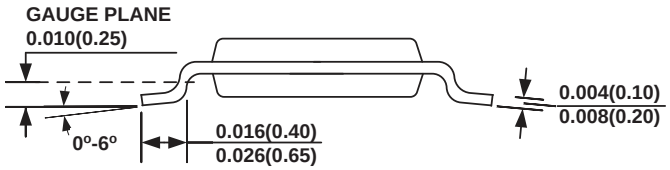
TOP VIEW



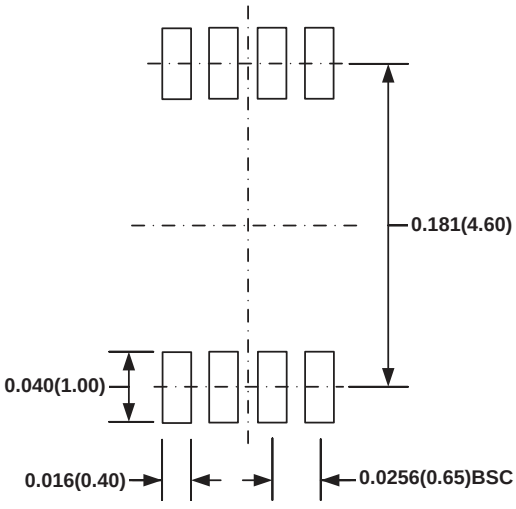
BOTTOM VIEW



FRONT VIEW



SIDE VIEW

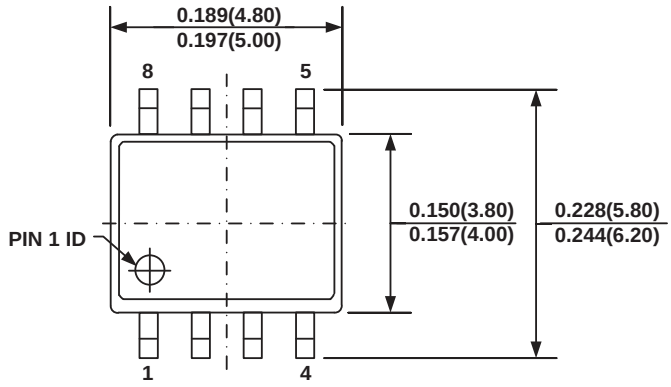


RECOMMENDED LAND PATTERN

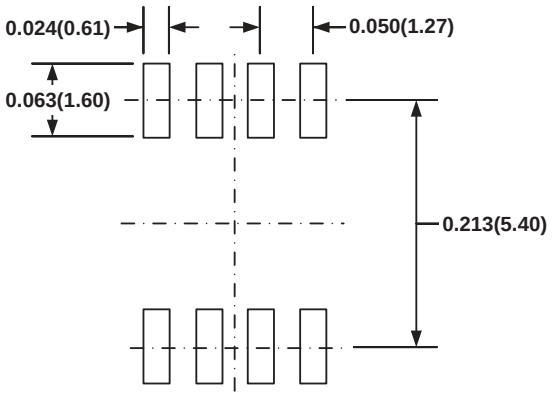
NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-187, VARIATION AA.
7) DRAWING IS NOT TO SCALE.

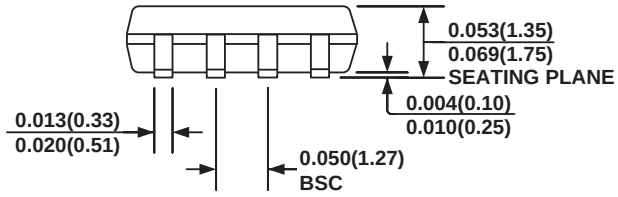
SOIC8



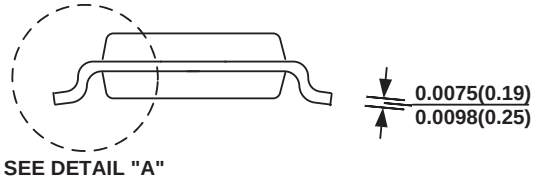
TOP VIEW



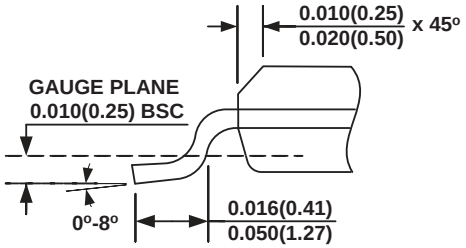
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.