

Low Profile, High Current IHLP® Inductors



Manufactured under one or more of the following:
US Patents; 6,198,375/6,204,744/6,449,829/6,460,244.
 Several foreign patents, and other patents pending.

STANDARD ELECTRICAL SPECIFICATIONS					
L_0 INDUCTANCE $\pm 20\%$ AT 100 kHz, 0.25 V, 0 A (μH)	DCR TYP. 25 °C (m Ω)	DCR MAX. 25 °C (m Ω)	HEAT RATING CURRENT DC TYP. (A) ⁽³⁾	SATURATION CURRENT DC TYP. (A) ⁽⁴⁾	SFR TYP. (MHz)
0.22	1.26	1.35	34.0	22.0	117
0.33	2.01	2.15	27.5	16.0	108
0.47	2.22	2.38	25.0	14.0	80
0.68	3.01	3.22	22.2	14.5	62
0.82	3.63	3.88	19.5	15.0	57
1.0	4.33	4.63	18.2	12.0	49
2.2	8.8	9.41	14.5	10.2	25
3.3	14.0	14.9	10.5	9.7	22
4.7	21.1	22.6	8.0	8.7	17
5.6	26.7	28.6	7.4	7.6	15
6.8	31.2	33.4	7.0	6.7	13
8.2	42.1	45.0	5.7	6.6	12.6
10.0	48.4	51.8	5.4	6.4	12
15.0	61.0	65.3	4.9	3.7	10.3
22.0	88.0	94.2	4.3	3.3	8.2
33.0	135	144	3.2	3.2	6.7

Notes

- (1) All test data is referenced to 25 °C ambient
- (2) Operating temperature range - 55 °C to + 125 °C
- (3) DC current (A) that will cause an approximate ΔT of 40 °C
- (4) DC current (A) that will cause L_0 to drop approximately 20 %
- (5) The part temperature (ambient + temp. rise) should not exceed 125 °C under worst case operating conditions. Circuit design, component placement, PWB trace size and thickness, airflow and other cooling provisions all affect the part temperature. Part temperature should be verified in the end application.

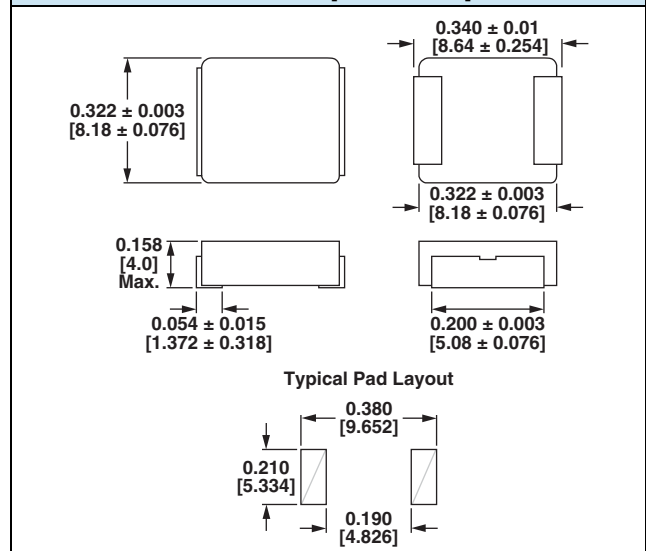
FEATURES

- Shielded construction
- Excellent DC/DC energy storage up to 1 MHz to 2 MHz. Filter inductor applications up to SFR (see table below)
- Operating temperature up to 125 °C
- Lowest DCR/ μH , in this package size
- Handles high transient current spikes without saturation
- Ultra low buzz noise, due to composite construction
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912


RoHS
 COMPLIANT

APPLICATIONS

- PDA/notebook/desktop/server applications
- High current POL converters
- Low profile, high current power supplies
- Battery powered devices
- DC/DC converters in distributed power systems
- DC/DC converter for Field Programmable Gate Array (FPGA)

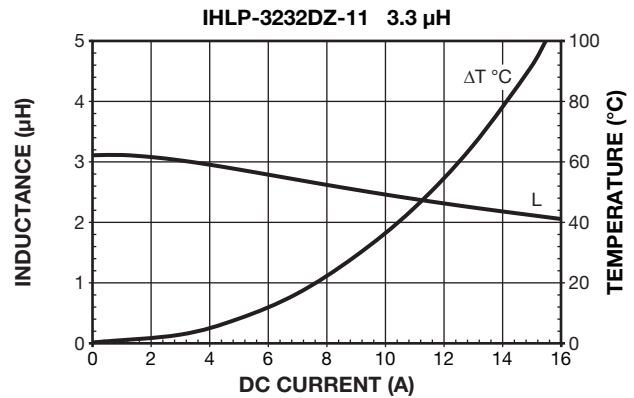
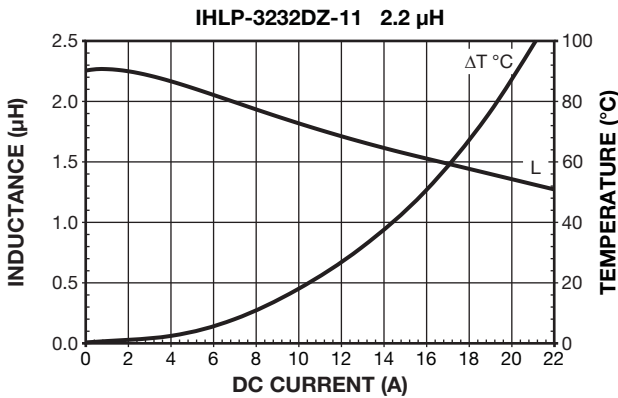
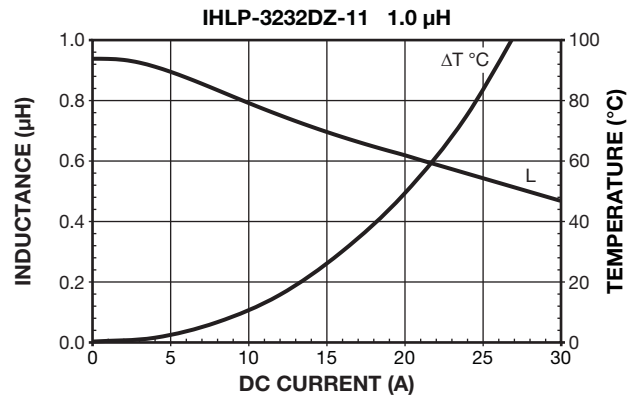
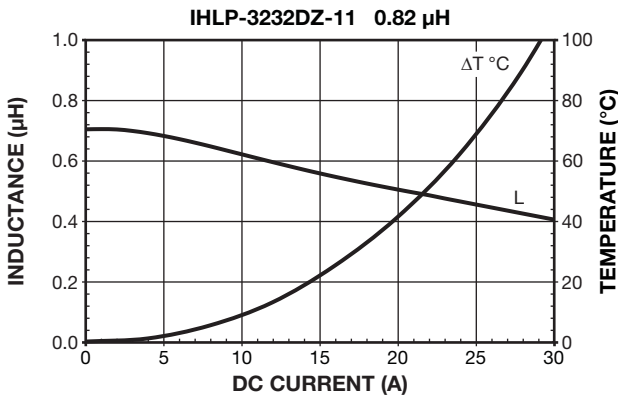
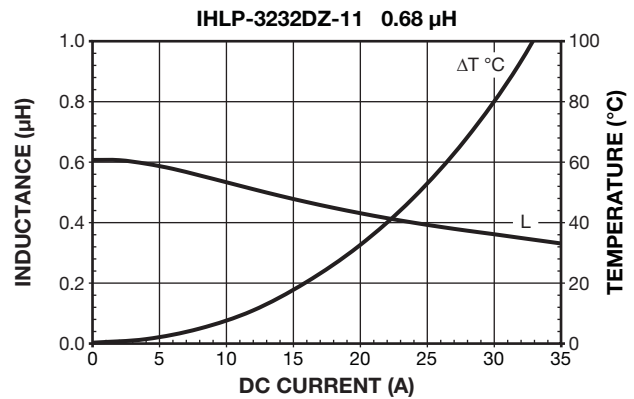
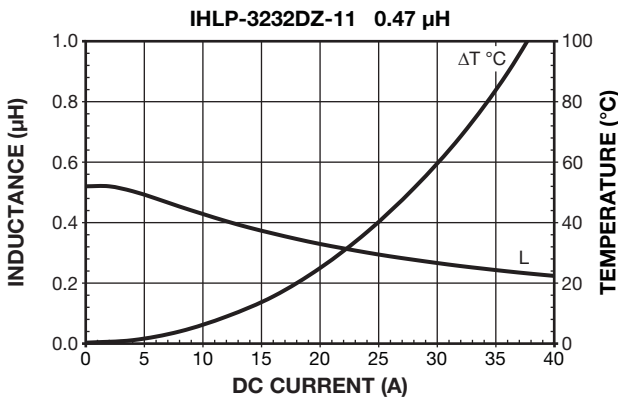
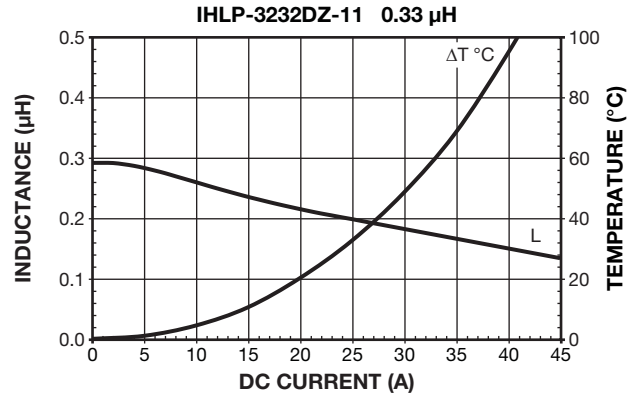
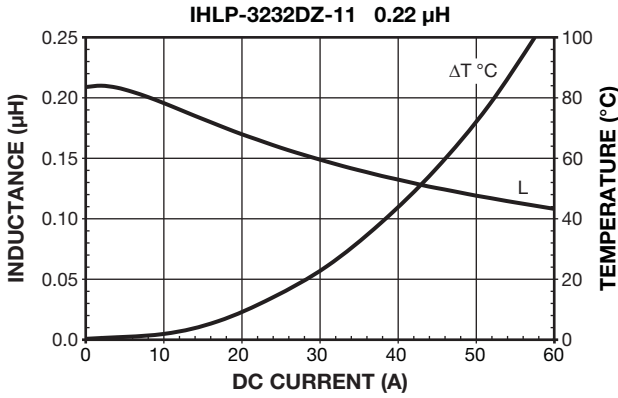
DIMENSIONS in inches [millimeters]


DESCRIPTION				
IHLP-3232DZ-11	33 μH	$\pm 20\%$	ER	e3
MODEL	INDUCTANCE VALUE	INDUCTANCE TOLERANCE	PACKAGE CODE	JEDEC LEAD (Pb)-FREE STANDARD

GLOBAL PART NUMBER																	
I	H	L	P	3	2	3	2	D	Z	E	R	3	3	0	M	1	1
PRODUCT FAMILY				SIZE				PACKAGE CODE		INDUCTANCE VALUE			TOL.	SERIES			

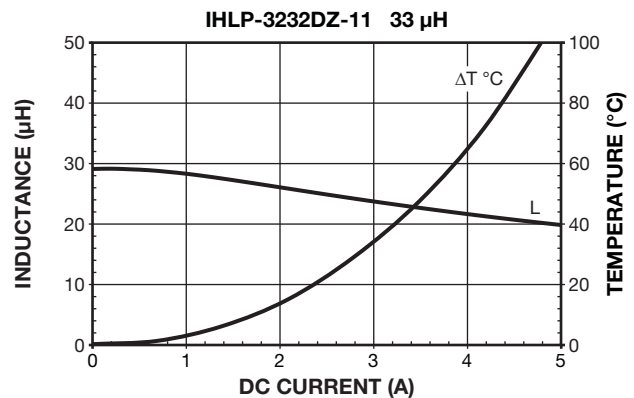
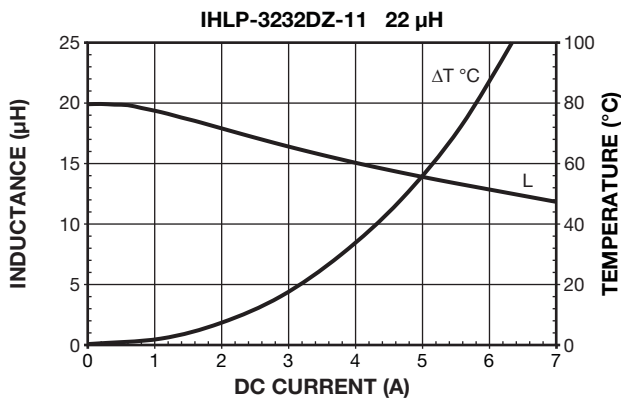
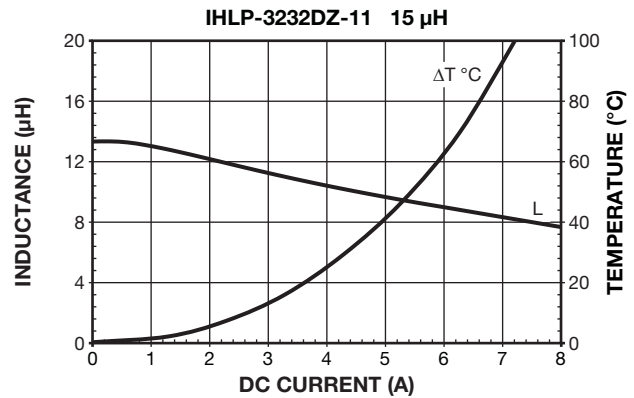
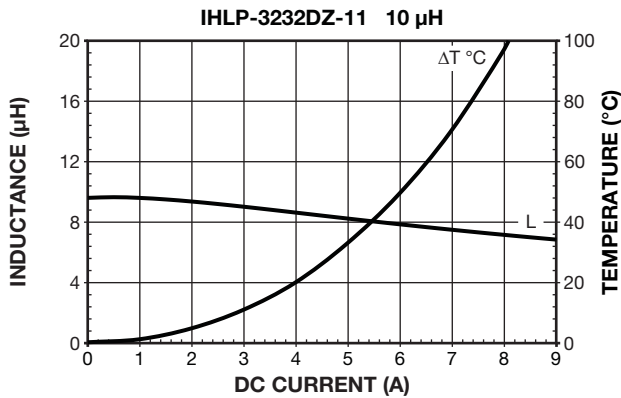
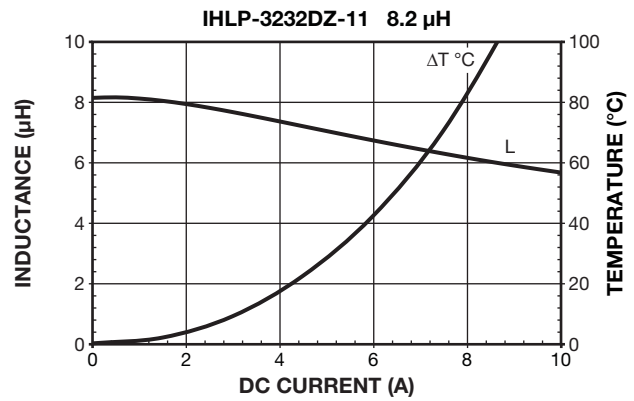
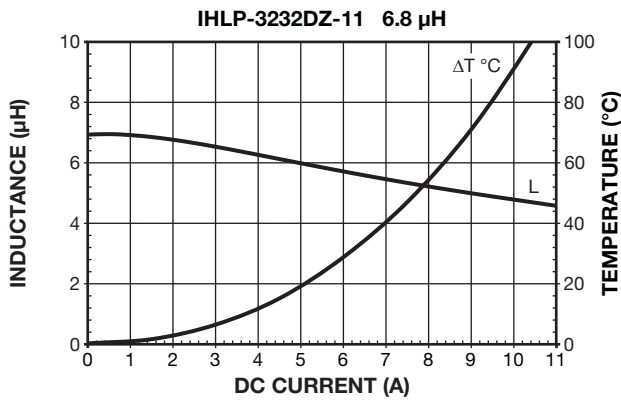
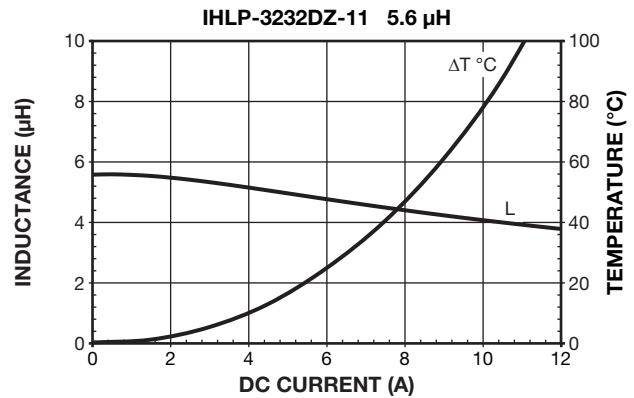
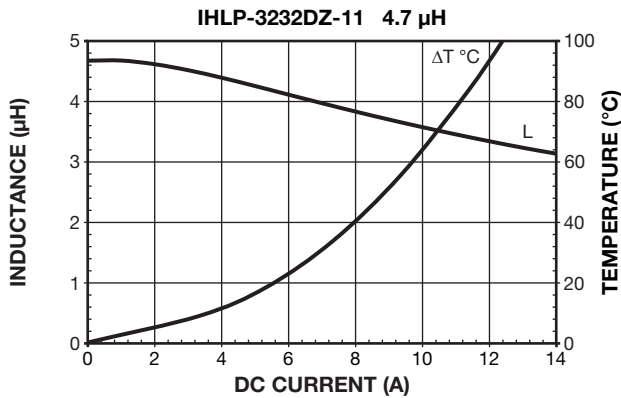


PERFORMANCE GRAPHS



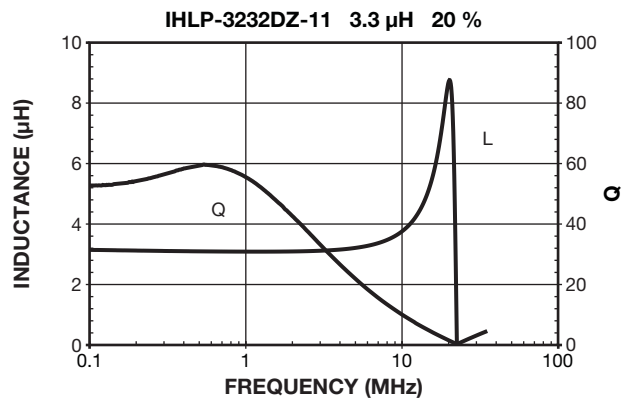
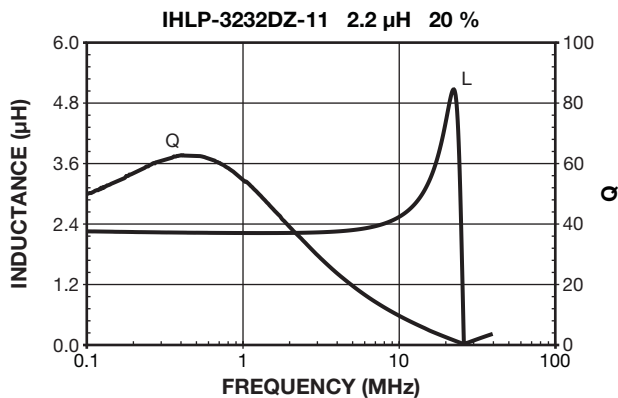
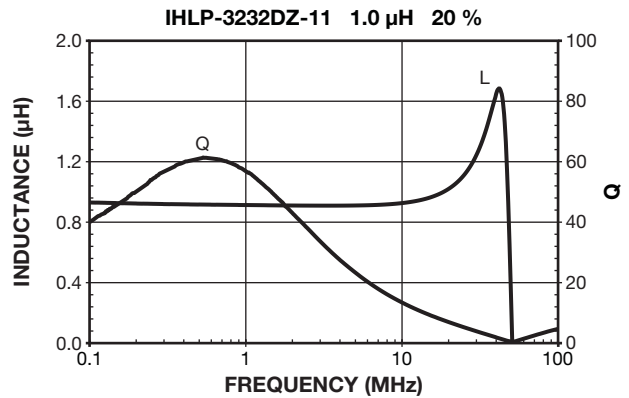
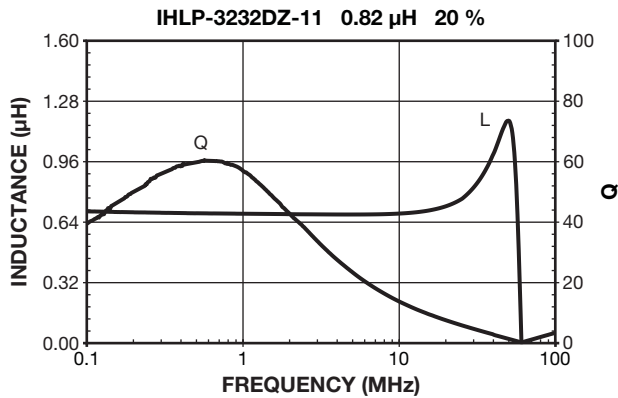
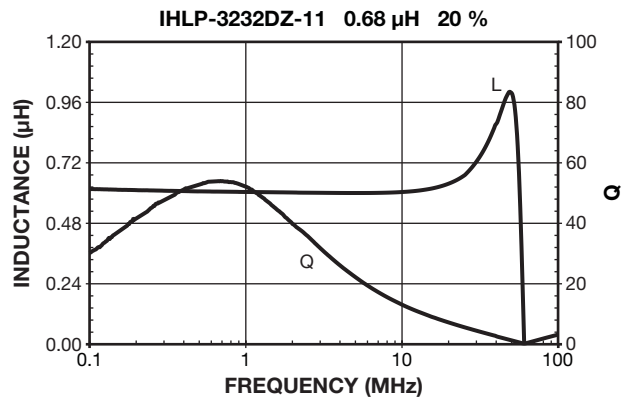
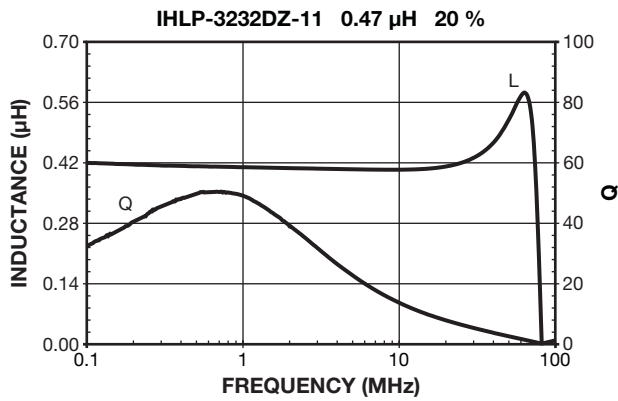
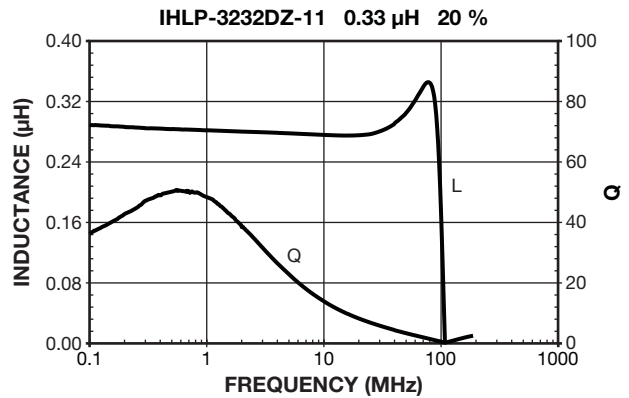
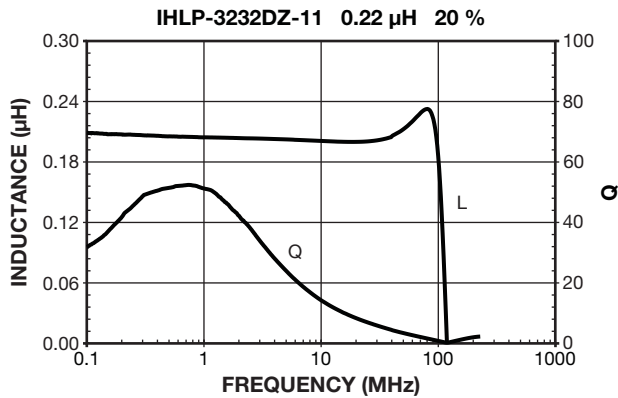


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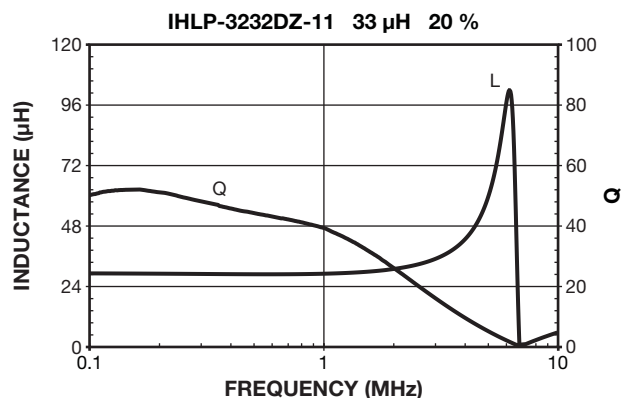
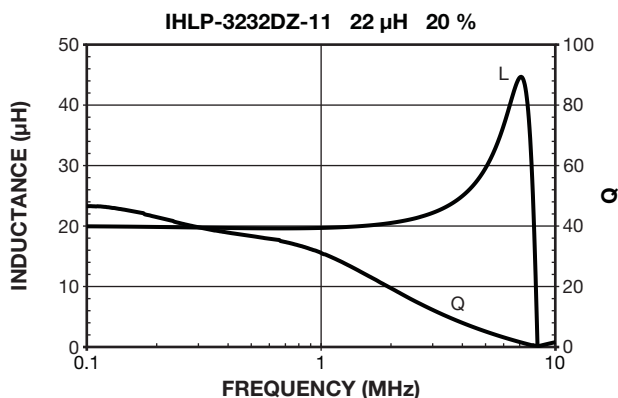
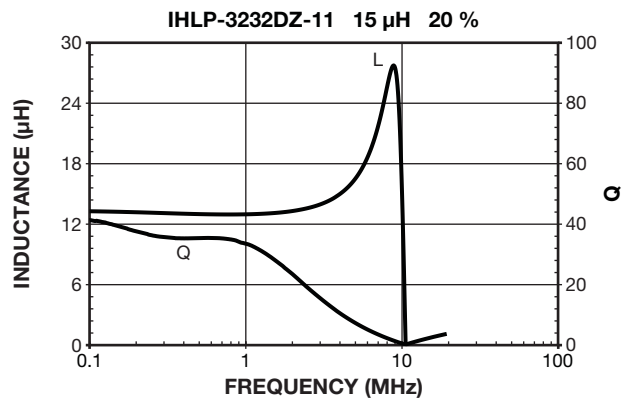
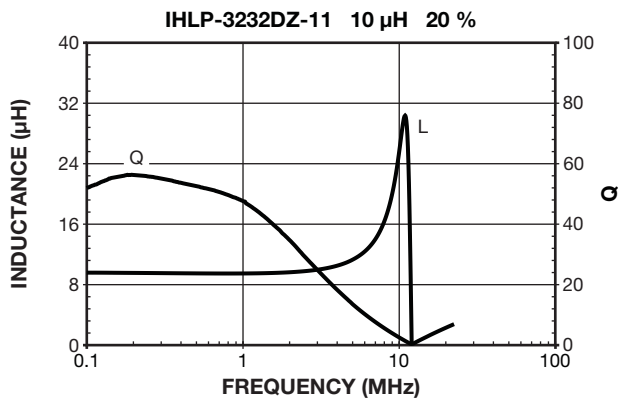
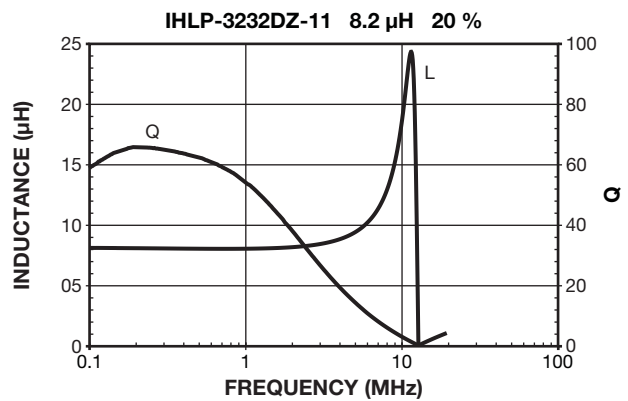
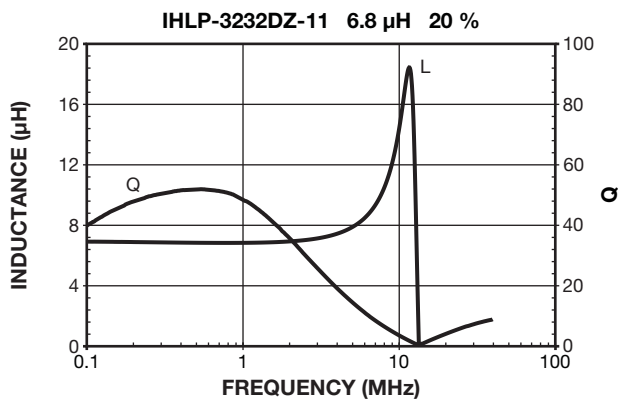
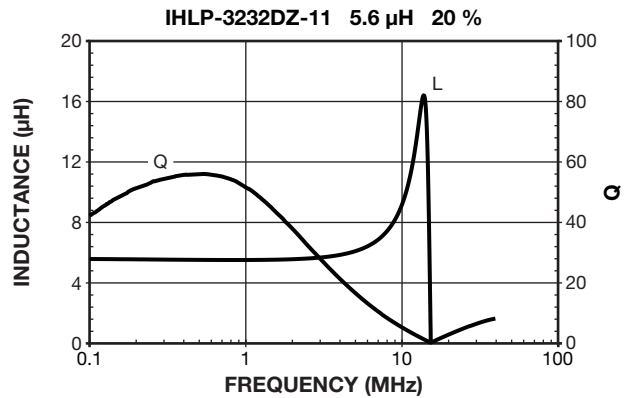
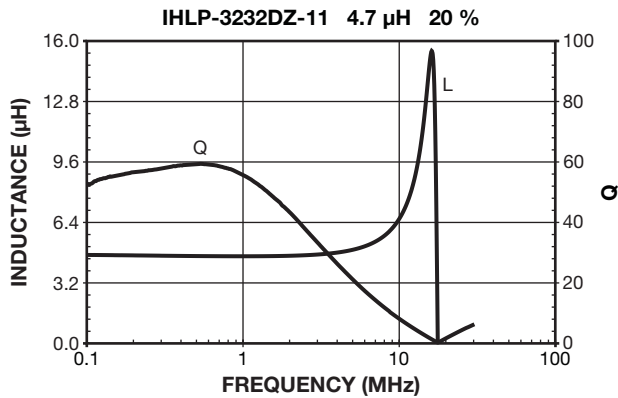


PERFORMANCE GRAPHS: INDUCTANCE AND Q VS. FREQUENCY





PERFORMANCE GRAPHS: INDUCTANCE AND Q VS. FREQUENCY





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