HOLT INTEGRATED CIRCUITS INC.

HI-8483

ARINC 429 Dual Line Receiver

February 2012

GENERAL DESCRIPTION

The HI-8483 bus interface unit is a dual differential line receiver in accordance with the requirements of the ARINC 429 bus specification. The device translates incoming ARINC 429 signals to normal CMOS/TTL levels on each of its two independent receive channels. The HI-8483 is a functional alternative to the Fairchild/Raytheon RM3283 and DEI3283.

Two TTL compatible self-test inputs for testing the ARINC channels are available. They can be used to override the ARINC input data and set the channel outputs to a known state. The self-test mode checks the entire circuit including the analog line receivers and digital logic.

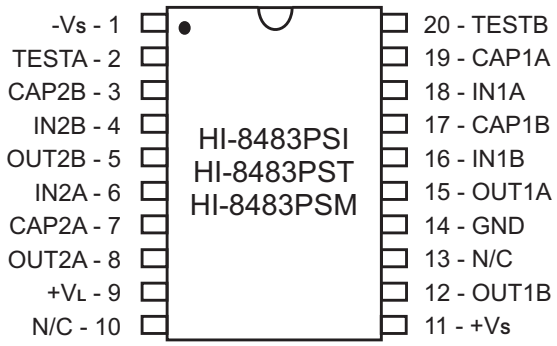
All the ARINC inputs have built-in hysteresis to reject noise that may be present on the ARINC bus. Additional input noise filtering can also be accomplished with external capacitors.

The HI-8483 is available in a variety of ceramic & plastic packages including Small Outline (SOIC), DIP & Leadless Chip Carrier (LCC).

FEATURES

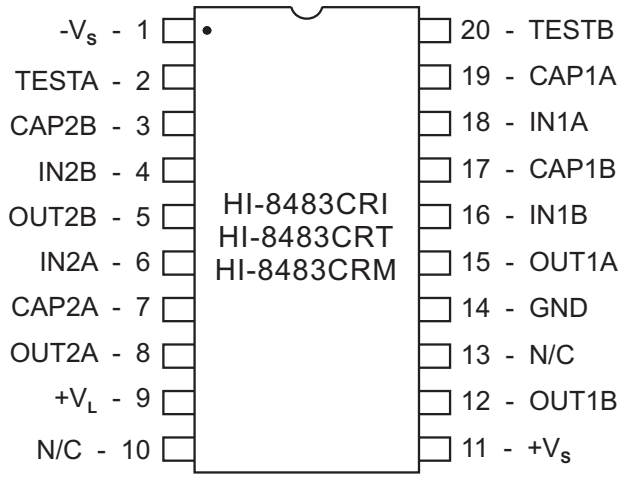
- Replacement for RM3283 and DEI3283
- Converts ARINC 429 levels to digital data
- Input hysteresis for superior noise rejection
- TTL and CMOS outputs and test inputs
- Military screening available
- 20-Pin SOIC, DIP & LCC packages are available

PIN CONFIGURATIONS (Top Views)



20 - Pin Plastic Small Outline package (SOIC)

(See ordering information for additional pin configurations)



20 - Pin Ceramic Dual In Line package (CERDIP)

(See ordering information for additional pin configurations)

TRUTH TABLE

ARINC INPUTS	TEST INPUTS		OUTPUTS	
V (A) - V (B)	TEST A	TEST B	OUT A	OUT B
Null	0	0	0	0
Zero	0	0	0	1
One	0	0	1	0
Don't Care	0	1	0	1
Don't Care	1	0	1	0
Don't Care	1	1	0	0

PIN DESCRIPTIONS

SIGNAL	FUNCTION	DESCRIPTION
CAP1A	INPUT	Filter capacitor input for terminal A of channel 1
CAP1B	INPUT	Filter capacitor input for terminal B of channel 1
CAP2A	INPUT	Filter capacitor input for terminal A of channel 2
CAP2B	INPUT	Filter capacitor input for terminal B of channel 2
GND	POWER	Chip 0V supply
IN1A	ARINC INPUT	ARINC 429 input terminal A of channel 1
IN1B	ARINC INPUT	ARINC 429 input terminal B of channel 1
IN2A	ARINC INPUT	ARINC 429 input terminal A of channel 2
IN2B	ARINC INPUT	ARINC 429 input terminal B of channel 2
OUT1A	OUTPUT	TTL output terminal A of channel 1
OUT1B	OUTPUT	TTL output terminal B of channel 1
OUT2A	OUTPUT	TTL output terminal A of channel 2
OUT2B	OUTPUT	TTL output terminal B of channel 2
TESTA	INPUT	Test input terminal A
TESTB	INPUT	Test input terminal B
+VL	POWER	+5 Volts +/- 10%
+VS	POWER	+15 Volts +/- 10%
-VS	POWER	-15 Volts +/- 10%

BLOCK DIAGRAM

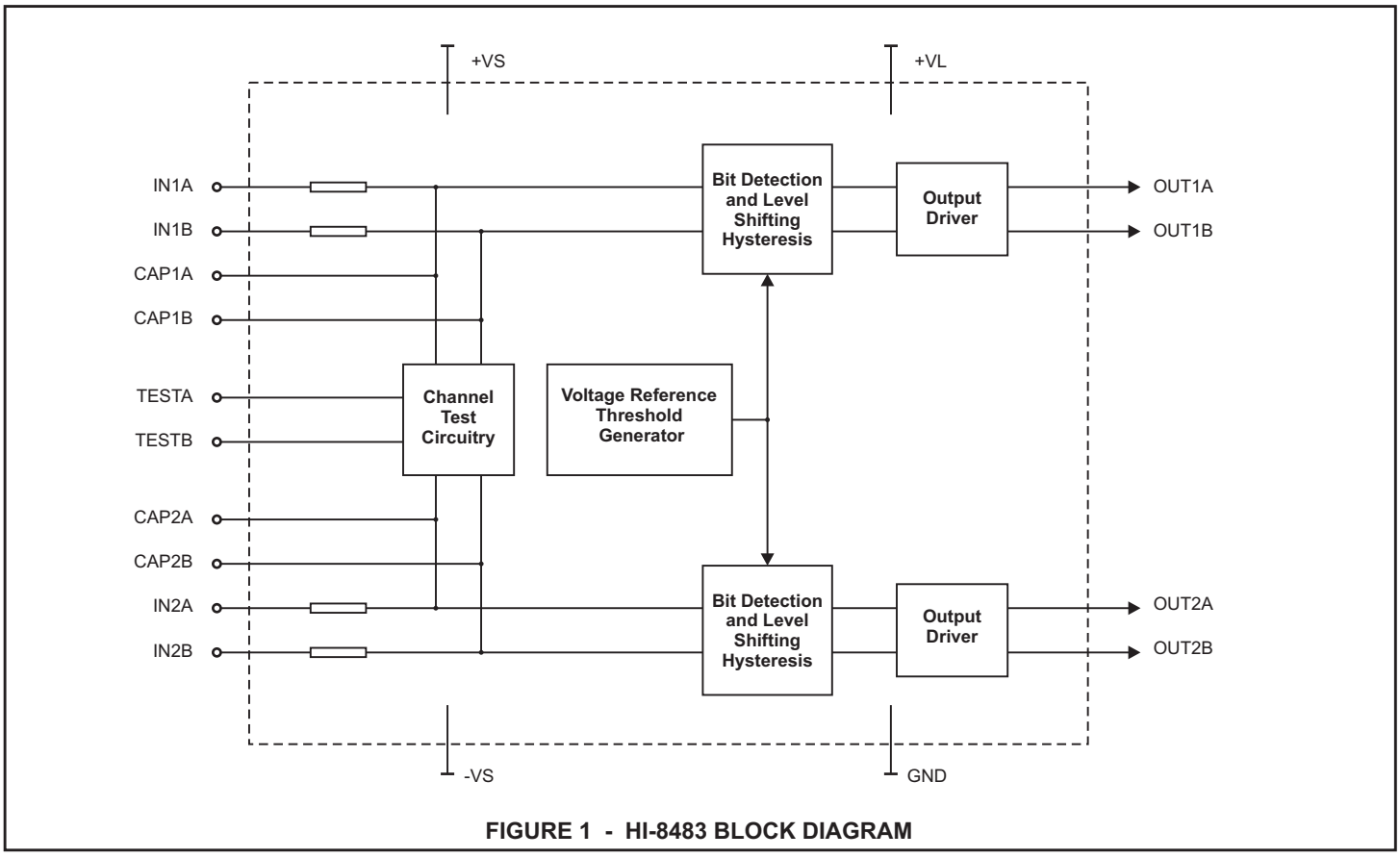


FIGURE 1 - HI-8483 BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

The HI-8483 contains two independent ARINC 429 receive channels, which take differently encoded ARINC level data and convert it to serial TTL level data. The HI-8483 provides two complete analog line receivers and no external components are required.

Input level-shifting resistor networks allow ARINC input voltage transients up to +/- 200V without damage to the HI-8483.

Each channel is identical, featuring symmetrical delays for better high-speed performance. Input common mode rejection is excellent and threshold voltage is stable, independent of supply voltage. Data outputs are TTL and CMOS compatible.

Two TTL compatible test inputs (TESTA and TESTB) used to simultaneously test both ARINC channels are available. They can be used to override the ARINC input data and set the channel outputs to a known state.

The HI-8483 contains two discrete ARINC 429 receiver channels. Each channel contains three main sections: a resistor input network, a window comparator, and a logic output buffer stage. The first stage provides over-voltage protection and biases the signal using voltage dividers, providing excellent input common mode rejection. The TESTA and TESTB inputs are provided to set the outputs to a predetermined state for built-in channel test capability. If the test inputs are not used they should be grounded.

The window comparator section detects data from the input resistor network. An ARINC “high” state generates a logic “1” at OUTA and an ARINC “low” state generates a logic “1” at OUTB. An ARINC “null” state at the inputs forces both outputs to logic “0”. Threshold and hysteresis voltages are generated by an on-chip voltage reference to maintain stable switching characteristics over temperature and supply voltage variations.

The output stage generates a TTL compatible logic output capable of driving 3 mA of load.

ARINC LEVELS

The ARINC 429 specification requires the following detection levels:

STATE	DIFFERENTIAL VOLTAGE
ONE	+6.5V to +13V
NULL	+2.5V to -2.5V
ZERO	-6.5V to -13V

The HI-8483 guarantees recognition of these levels with a common mode voltage with respect to GND less than ±13V for the worst case condition.

NOISE

The input hysteresis is set to reject voltage level transitions in the undefined region between the maximum ZERO level and the minimum NULL level and the undefined region between the maximum NULL level and the minimum ONE level. Therefore, once a valid input differential voltage threshold is detected, the outputs will remain at a valid logic state until a new valid input voltage is detected.

The noise filter capacitors are optional and are added to provide extra noise immunity by limiting the bandwidth of the input signal before it reaches the window comparator stage. Two capacitors are required for each channel and they must be of the same value. The suggested capacitor value for 100KHz operation is 39 pF. For lower data rates, larger values of capacitance may be used to yield better noise performance. To get optimum performance, the following equation can be used to calculate capacitor value for a specific data rate:

$$C_{FILTER} = \frac{3.95 \times 10^6}{F_0}$$

Where:
C_{FILTER} is the capacitor value in pF
F_0 is the input frequency 10 KHz <= F_0 <= 150 KHz

TYPICAL APPLICATIONS

APPLICATIONS

The standard connections for the HI-8483 are shown in Figure 2. Decoupling of the supply should be done near the IC to avoid propagation of noise spikes due to switching transients. The ground (GND) connection should be sturdy and isolated from large switching currents to provide a quiet ground reference.

The HI-8483 can be used with HI-8570 or HI-8585 Line Drivers to provide a complete analog ARINC 429 interface solution. A simple application, which can be used in systems requiring a repeater type circuit for long transmissions or for test interfaces, is given in Figure 3. More HI-8570 or HI-8585 drivers may be added to test multiple ARINC channels, as shown.

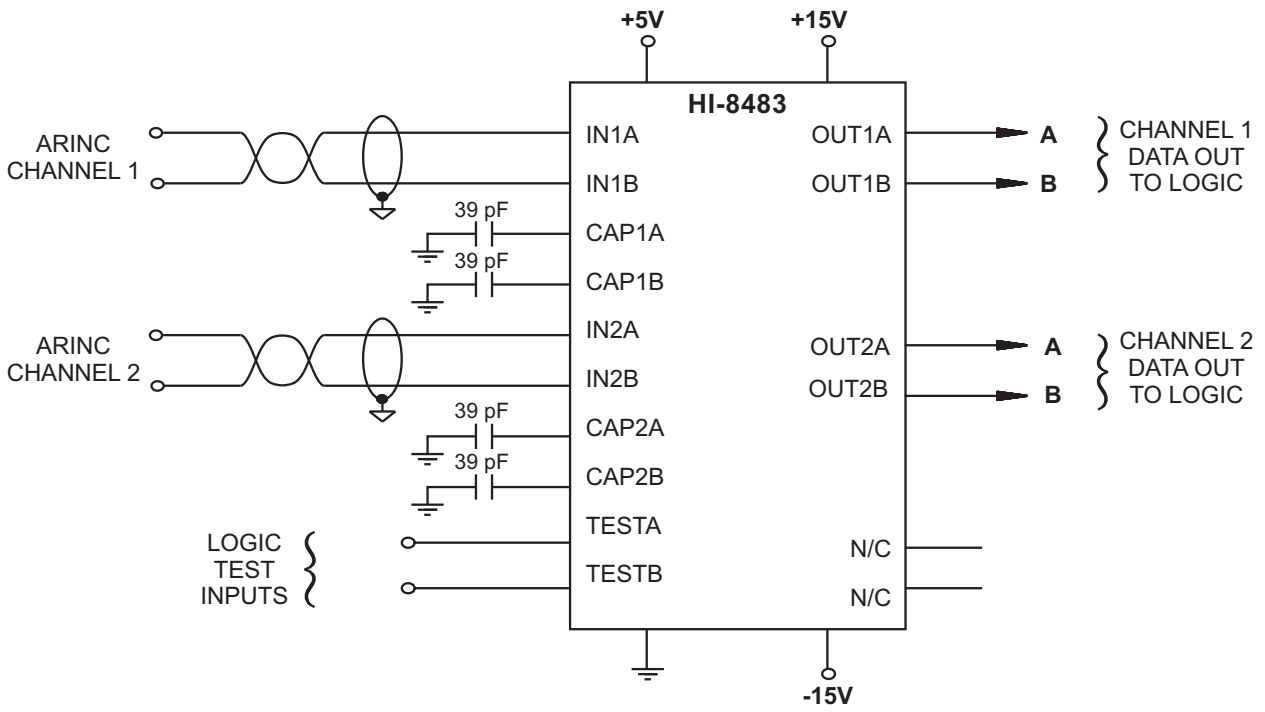


FIGURE 2 - ARINC RECEIVER STANDARD CONNECTIONS

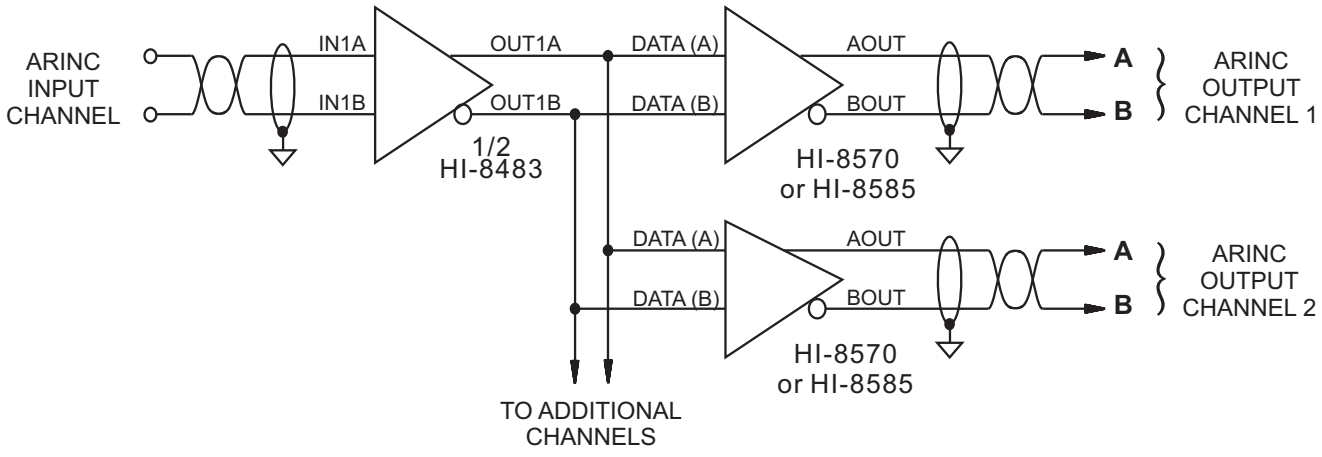


FIGURE 3 - ARINC REPEATER CIRCUIT

TIMING DIAGRAMS

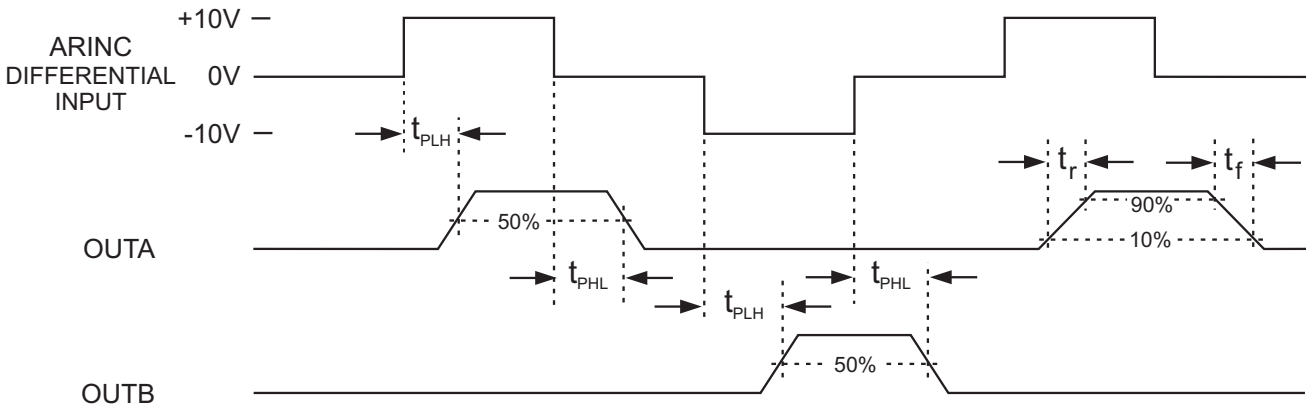


FIGURE 4

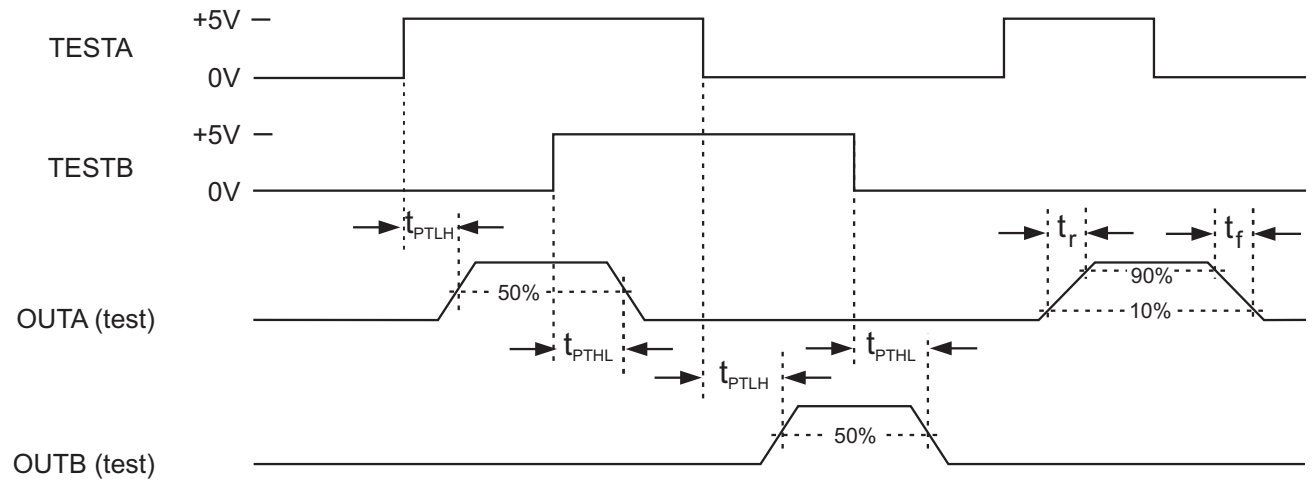


FIGURE 5

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to Gnd = 0V)

Supply Voltage, +Vs: .....+20 VDC -Vs: .....-20 VDC +Vs to -Vs: .....+36 VDC +VL: .....+7 VDC	Voltage at ARINC Inputs: .....-200V to +200V
	Voltage at Any Other Input: .....-0.3V to VL + 0.3V
	Output Short Circuit Protected: .....Not Protected
Operating Temperature Range: (Industrial) .....-40°C to +85°C (Hi-Temp) .....-55°C to +125°C (Military) .....-55°C to +125°C	Storage Temperature Range: .....-65°C to +150°C
	Soldering Temperature: (Ceramic).....60 sec. at +300°C (Plastic - leads).....10 sec. at +280°C (Plastic - body) .....+260°C Max.
Internal Power Dissipation: 900mW	

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

±13.5V ≤ Vs ≤ ±16.5V, +4.5V ≤ VL ≤ +5.5V, Operating temperature range (unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supplies						
+VS (+15V) Supply Current	I_{CC}	+/-VS = +/- 16.5V, VL = 5.0V Test Inputs = 0V Test Inputs = 5V			 6.0 6.0	 mA mA
-VS (-15V) Supply Current	I_{EE}	+/-VS = +/- 16.5V, VL = 5.0V Test Inputs = 0V Test Inputs = 5V			 12.0 18.5	 mA mA
+VL (+5V) Supply Current	I_L	+/-VS = +/- 16.5V, VL = 5.0V Test Inputs = 0V Test Inputs = 5V			 9.0 17.5	 mA mA
ARINC 429 Inputs						
Null - to - One Transition V(INA) - V(INB)	V_{HH}	+/-VS = +/- 15.0V, VL = 5.0V Test inputs = 0V, V(INB) = -2.50V TA = 25°C	5.70		6.30	V
One - to - Null Transition V(INA) - V(INB)	V_{HL}	+/-VS = +/- 15.0V, VL = 5.0V Test inputs = 0V, V(INB) = -2.50V	4.50		5.50	V
One - to - Null Transition Hysteresis	V_{HHYS}	VHH - VHL TA = 25°C	0.8		1.2	V
Null - to - Zero Transition V(INA) - V(INB)	V_{LL}	+/-VS = +/- 15.0V, VL = 5.0V Test inputs = 0V, V(INB) = +2.50V TA = 25°C	-6.30		-5.70	V
Zero - to - Null Transition V(INA) - V(INB)	V_{LH}	+/-VS = +/- 15.0V, VL = 5.0V Test inputs = 0V, V(INB) = +2.50V	-5.50		-4.50	V
Zero - to - Null Transition Hysteresis	V_{LHYS}	VLL - VLH TA = 25°C	-1.2		-0.8	V
Input Common-Mode Voltage Range	V_{CM}		-13		+13	V
Input Resistor Value: Unpowered	R_{IN}	INA to CAPA, INB to CAPB	8.5	10	11.5	KΩ
Input Resistance: Differential (Unpowered) To GND (Unpowered)	R_I R_G	INA to INB, INA to GND, INB to GND	30 20	50 30		KΩ KΩ
Input Current: Input Sink Input Source	I_{IH} I_{IL}		 -450		200	µA µA
Input Capacitance: Differential (Guaranteed but not tested) To GND To V_{DD}	C_I C_G C_H	INA to INB			10 10 10	pF pF pF

ELECTRICAL CHARACTERISTICS (Cont.)

±13.5V ≤ V_S ≤ ±16.5V, +4.5V ≤ V_L ≤ +5.5V, Operating temperature range (unless otherwise noted)

PARAMETER		SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Logic Inputs (TESTA, TESTB)							
Input Voltage:	Input Voltage HI Input Voltage LO	V_{IH} V_{IL}	VS = +/-15V, VL=4.5V	2.0		 0.9	V V
Input Current:	Input Sink Input Source	I_{IH} I_{IL}	V_{IH} = 5V, VS = +/-15V, VL=5V V_{IL} = 0.8V, VS = +/-15V, VL=5V	 -40		300	µA µA
Logic Outputs (OUTA, OUTB)							
Output Voltage:	Input Voltage HI	V_{OH}	VS = +/-15V, VL=5V I_{OH} = -100 µA (TA = 25°C) I_{OH} = -2.8 mA	 4.0 3.5			 V V
	Input Voltage LO	V_{OL}	VS = +/-15V, VL=5V I_{OL} = 100 µA (TA = 25°C) I_{OL} = 2.0 mA			 0.1 0.8	 V V
Timing Parameters							
Output Rise Time		t_r	CL - 60 pF	10		70	ns
Output Fall Time		t_f	CL - 60 pF	10		70	ns
Propagation Delay	INA/B to OUTA/B rising edge	t_{PLH}	CAPA, CAPB, CL = 60 pF		700		ns
	INA/B to OUTA/B falling edge	t_{PHL}	CAPA, CAPB, CL = 60 pF		700		ns
	Matching of TPLH and TPHL	t_{DTP}	| TPLH - TPHL |			500	ns
	TESTA/B to OUTA/B rising edge	t_{PTLH}	CL = 60 pF, VIN = 0.8V/2.0V		700		ns
	TESTA/B to OUTA/B falling edge	t_{PTHL}	CL = 60 pF, VIN = 0.8V/2.0V		700		ns

ORDERING INFORMATION & THERMAL CHARACTERISTICS

HI - 8483PS x x (Plastic Wide Body SOIC)

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO
M	-55°C TO +125°C	M	YES

PART NUMBER	PACKAGE DESCRIPTION	THERMAL RES. θ_{JC}	THERMAL RES. θ_{JA}
PS	20 PIN PLASTIC SOIC WIDE BODY PACKAGE (20HW)	17°C/W	90°C/W

ORDERING INFORMATION & THERMAL CHARACTERISTICS (Cont.)

HI - 8483CR x (20-pin CerDIP)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN	LEAD FINISH
I	-40°C TO +85°C	I	NO	Tin / Lead (Sn / Pb) Solder
T	-55°C TO +125°C	T	NO	Tin / Lead (Sn / Pb) Solder
M	-55°C TO +125°C	M	YES	Tin / Lead (Sn / Pb) Solder

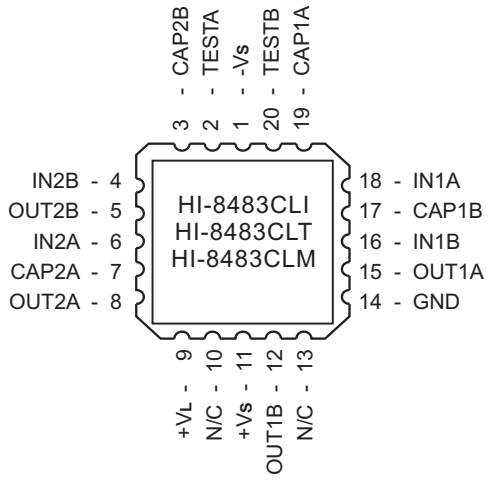
PART NUMBER	PACKAGE DESCRIPTION	THERMAL RES.	
		θ_{JC}	θ_{JA}
CR	20 PIN CERDIP (20D)	28°C/W	90°C/W

HI - 8483CL x (20-pin Ceramic LCC)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN	LEAD FINISH
I	-40°C TO +85°C	I	NO	Gold
T	-55°C TO +125°C	T	NO	Gold
M	-55°C TO +125°C	M	YES	Tin / Lead (Sn / Pb) Solder

PART NUMBER	PACKAGE DESCRIPTION	THERMAL RES.	
		θ_{JC}	θ_{JA}
CL	20 PIN CERAMIC LEADLESS CHIP CARRIER (20S)	25°C/W	85°C/W

ADDITIONAL HI-8483 PIN CONFIGURATION



20 - Pin Ceramic Leadless Chip Carrier (LCC)

(See first page of data sheet for additional pin configurations)

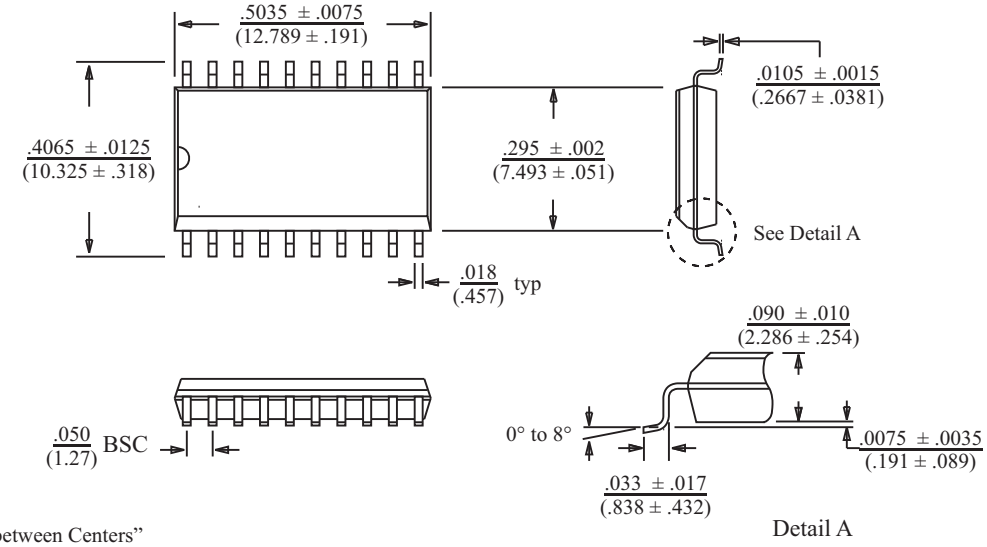
REVISION HISTORY

Dwg. No.	Rev.	Date	Description of Change
DS8483	NEW	03/22/10	Initial Release
	A	02/29/12	Correct typo in part numbers on Ordering Information, page 8. Change soldering temperature (Plastic - body) in Absolute Maximum Ratings from 220C to 260C.

20-PIN PLASTIC SMALL OUTLINE (SOIC) - WB
(Wide Body)

inches (millimeters)

Package Type: 20HW

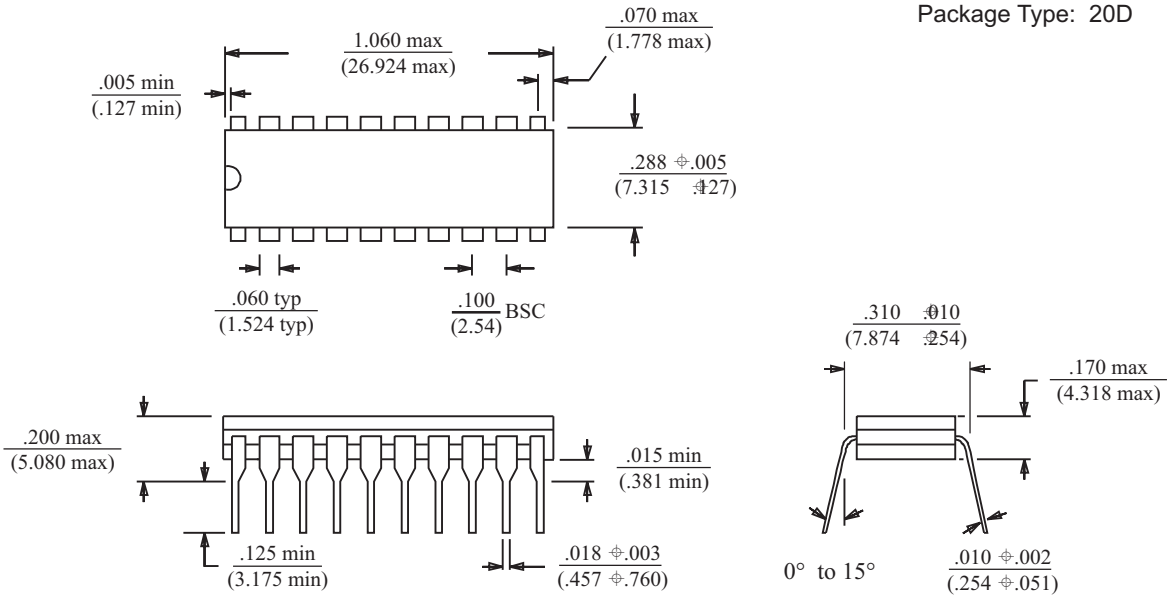


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

20-PIN CERDIP

inches (millimeters)

Package Type: 20D

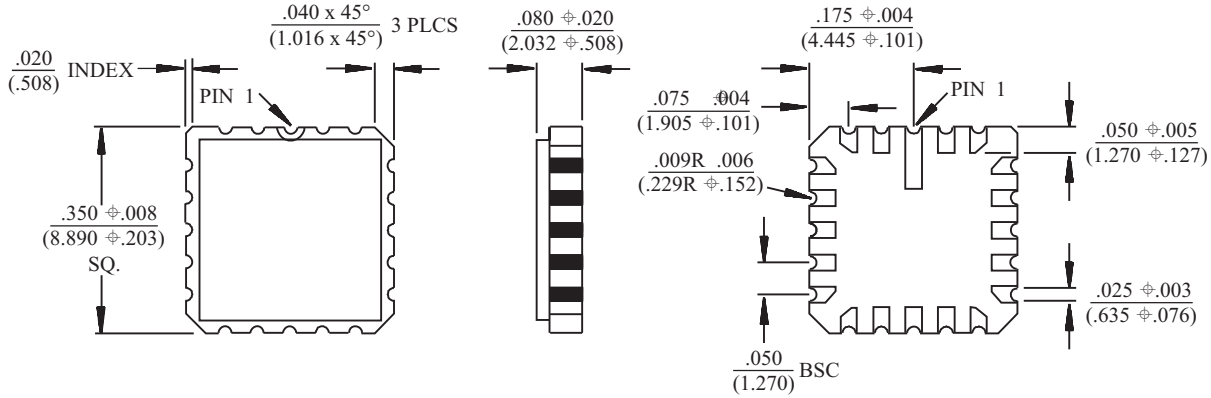


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

20-PIN CERAMIC LEADLESS CHIP CARRIER

inches (millimeters)

Package Type: 20S



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)