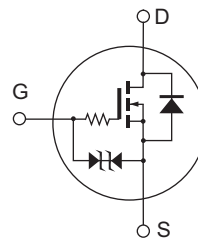


Features

- Low on-resistance
 $R_{DS(on)} = 0.2 \Omega$ typ. ($V_{GS} = 4 \text{ V}$, $I_D = 500 \text{ mA}$)
- 2.5 V gate drive devices.
- Small package (MPAK)

Outline

RENESAS Package code: PLSP0003ZB-A
(Package name: MPAK)



1. Source
2. Gate
3. Drain

Note: Marking is "ZZ-"

2SK2980

(Ta = 25°C)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	+12	V
		-10	V
Drain current	I_D	1.0	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	4	A
Channel dissipation	P_{ch} ^{Note2}	0.8	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$

2. Value at when using alumina ceramic board (12.5 x 20 x 0.7 mm)

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 100\mu A$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	+12	—	—	V	$I_G = +100\mu A$, $V_{DS} = 0$
		-10	—	—	V	$I_G = -100\mu A$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1.0	μA	$V_{DS} = 30V$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 5.0	μA	$V_{GS} = \pm 8V$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	$I_D = 10\mu A$, $V_{DS} = 5V$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.2	0.28	Ω	$I_D = 500mA$, $V_{GS} = 4V$ ^{Note3}
Static drain to source on state resistance	$R_{DS(on)}$	—	0.3	0.5	Ω	$I_D = 500mA$, $V_{GS} = 2.5V$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	1.2	2.0	—	S	$I_D = 500mA$, $V_{DS} = 10V$ ^{Note3}
Input capacitance	C_{iss}	—	155	—	pF	$V_{DS} = 10V$, $V_{GS} = 0$, $f = 1MHz$
Output capacitance	C_{oss}	—	75	—	pF	
Reverse transfer capacitance	C_{rss}	—	35	—	pF	
Turn-on delay time	$t_{d(on)}$	—	12	—	ns	$V_{GS} = 4V$, $I_D = 500mA$, $R_L = 20\Omega$
Rise time	t_r	—	30	—	ns	
Turn-off delay time	$t_{d(off)}$	—	35	—	ns	
Fall time	t_f	—	30	—	ns	

Note: 3. Pulse test