

FEATURES

Excellent Sonic Characteristics

Low Noise: 6 nV/√Hz

Low Distortion: 0.0006%

High Slew Rate: 22 V/μs

Wide Bandwidth: 9 MHz

Low Supply Current: 5 mA

Low Offset Voltage: 1 mV

Low Offset Current: 2 nA

Unity Gain Stable

SOIC-8 Package

APPLICATIONS

High Performance Audio

Active Filters

Fast Amplifiers

Integrators

GENERAL DESCRIPTION

The OP275 is the first amplifier to feature the Butler Amplifier front-end. This new front-end design combines both bipolar and JFET transistors to attain amplifiers with the accuracy and low noise performance of bipolar transistors, and the speed and sound quality of JFETs. Total Harmonic Distortion plus Noise equals that of previous audio amplifiers, but at much lower supply currents.

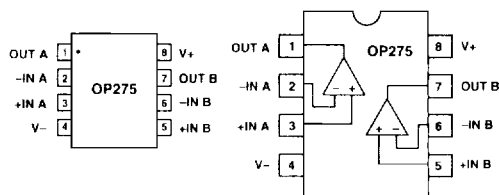
A very low *f*_c corner of below 6 Hz maintains a flat noise density response. Whether noise is measured at either 30 Hz or 1 kHz, it is only 6 nV/√Hz. The JFET portion of the input stage gives the OP275 its high slew rates to keep distortion low, even when large output swings are required, and the 22 V/μs slew rate of the OP275 is the fastest of any standard audio amplifier. Best of all, this low noise and high speed are accomplished using less than 5 mA of supply current, lower than any standard audio amplifier.

Improved dc performance is also provided with bias and offset currents greatly reduced over purely bipolar designs. Input offset voltage is guaranteed at 1 mV and is typically less than

PIN CONNECTIONS

8-Lead Narrow-Body SO
(S Suffix)

8-Lead Epoxy DIP
(P Suffix)



200 μV. This allows the OP275 to be used in many dc coupled or summing applications without the need for special selections or the added noise of additional offset adjustment circuitry.

The output is capable of driving 600 Ω loads to 10 V rms while maintaining low distortion. THD + Noise at 3 V rms is a low 0.0006%.

The OP275 is specified over the extended industrial (-40°C to +85°C) temperature range. OP275s are available in both plastic DIP and SOIC-8 packages. SOIC-8 packages are available in 2500 piece reels. Many audio amplifiers are not offered in SOIC-8 surface mount packages for a variety of reasons; however, the OP275 was designed so that it would offer full performance in surface mount packaging.

ORDERING GUIDE

Model	Temperature Range	Package Option*
OP275GP	-40°C to +85°C	8-Pin Plastic DIP
OP275GS	-40°C to +85°C	8-Pin SOIC
OP275GSR	-40°C to +85°C	SO-8 Reel, 2500 pcs.
OP275GBC	+25°C	DICE

*For outline information see Package Information section.

*Protected by U.S. Patent No. 5,101,126.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at <http://www.analog.com>.

OP275—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15.0\text{ V}$, $T_A = +25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE						
THD + Noise		$V_{in} = 3\text{ V rms}$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$		0.006		%
Voltage Noise Density	e_n	$f = 30\text{ Hz}$		7		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		6		$\text{nV}/\sqrt{\text{Hz}}$
Headroom		THD + Noise $\leq 0.01\%$, $R_L = 2\text{ k}\Omega$, $V_S = \pm 18\text{ V}$		>12.9		dBu
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			1	mV
Input Bias Current	I_B	$V_{CM} = 0\text{ V}$		100	350	nA
Input Offset Current	I_{OS}	$V_{CM} = 0\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		100	400	nA
Input Voltage Range	V_{CM}	$V_{CM} = 0\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		2	50	nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	-10.5		+10.5	V
Large Signal Voltage Gain	A_{VO}	$V_{CM} = \pm 10.5\text{ V}$, $40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	80	106		dB
		$R_L = 2\text{ k}\Omega$	250			V/mV
		$R_L = 2\text{ k}\Omega$, $40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	175			V/mV
		$R_L = 600\ \Omega$		200		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	$R_L = 2\text{ k}\Omega$	-13.5	± 13.9	+13.5	V
		$R_L = 2\text{ k}\Omega$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	-13	± 13.9	+13	V
		$R_L = 600\ \Omega$, $V_S = \pm 18\text{ V}$			-16/+14	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5\text{ V to } \pm 18\text{ V}$	85	111		dB
		$V_S = \pm 4.5\text{ V to } \pm 18\text{ V}$, $40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	80			dB
Supply Current	I_{SY}	$V_S = \pm 4.5\text{ V to } \pm 18\text{ V}$, $V_O = 0\text{ V}$, $R_L = \infty$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		4	5	mA
		$V_S = \pm 22\text{ V}$, $V_O = 0\text{ V}$, $R_L = \infty$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			5.5	mA
Supply Voltage Range	V_S		± 4.5		± 22	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$	15	22		V/ μs
Full-Power Bandwidth	BW _P					kHz
Gain Bandwidth Product	GBP			9		MHz
Phase Margin	ϕ_m			62		Degrees
Overshoot Factor		$V_{IN} = 100\text{ mV}$, $A_V = +1$, $R_L = 600\ \Omega$, $C_L = 100\text{ pF}$		10		%

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage	$\pm 22\text{ V}$
Input Voltage ²	$\pm 22\text{ V}$
Differential Input Voltage	$\pm 7.5\text{ V}$
Output Short-Circuit Duration to GND ³	Indefinite
Storage Temperature Range	
P, S Package	$-65^\circ\text{C to } +150^\circ\text{C}$
Operating Temperature Range	
OP275G	$40^\circ\text{C to } +85^\circ\text{C}$
Junction Temperature Range	
P, S Package	$-65^\circ\text{C to } +150^\circ\text{C}$
Lead Temperature Range (Soldering, 60 sec)	$+300^\circ\text{C}$

Package Type	θ_{JA} ⁴	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	$^\circ\text{C}/\text{W}$
8-Pin SOIC (S)	158	43	$^\circ\text{C}/\text{W}$

NOTES

¹Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

²For supply voltages greater than $\pm 22\text{ V}$, the absolute maximum input voltage is equal to the supply voltage.

³Shorts to either supply may destroy the device. See data sheet for full details.

⁴ θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.