LD1071

16 Channel Output LED Driver with 14 bit PWM Controller

Ver. 1.0 / Mar. 2009

LD1071 Revision History

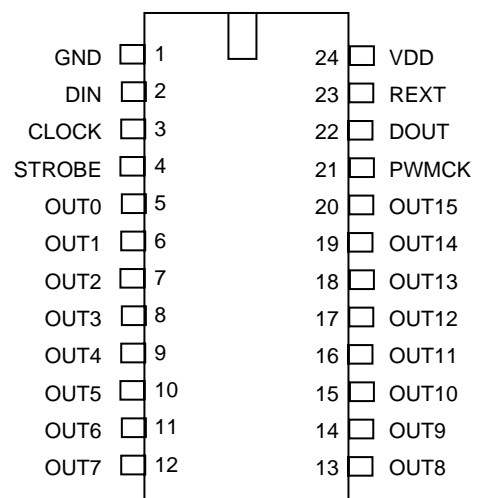| Version	Contents	Transfer Date
1.0	- First Version	2009.03.12

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DESCRIPTION

The LD1071 is specifically designed for LED and LED display applications using PWM(Pulse Width Modulation) control with 14 bit color depth. The LD1071 provides a constant output current for driving the LEDs against for the variation of LED forward voltage(Vf). The constant output current can be preset through an external resistor. Moreover, the preset output current with external resistor can be programmed up to 256 levels for LED global brightness adjustment. The LD1071 consists of 16 bit shift registers, latches, and-gates, constant current driver and 14 bit PWM controller.
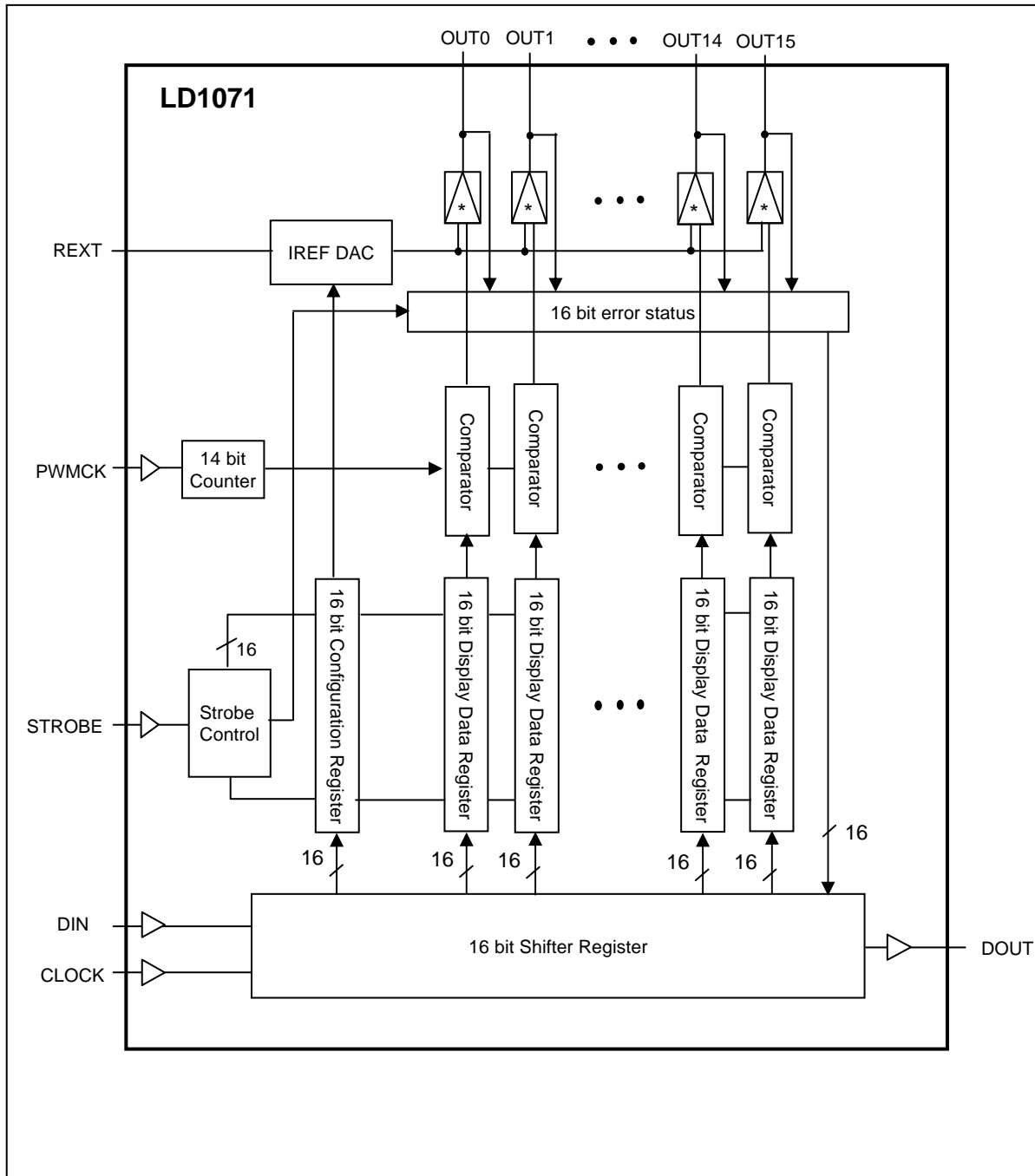
FEATURES

- **Output current : set-up at 5mA to 45mA with an external resistor**

   (when VDD=3.3V, Iout : 5mA ~ 30mA)
- **Include error detection circuit**
- **16 constant current output channels**
- **14 bit gray scale PWM control**
- **8 bit programmable output current control**
- **Constant current accuracy**
    - **Pin to pin deviation : < ± 3% (Max)**
    - **Chip to chip deviation : < ± 6% (Max)**
- **3.3V / 5V CMOS compatible input**
- **Package : LD1071-SP (SOP-24), LD1071-SS (SSOP-24)**
- **Maximum CLOCK input frequency : 25MHz**
- **Maximum PWMCK input frequency : 25MHz**

PIN CONFIGURATION

GND	1	24	VDD
DIN	2	23	REXT
CLOCK	3	22	DOUT
STROBE	4	21	PWMCK
OUT0	5	20	OUT15
OUT1	6	19	OUT14
OUT2	7	18	OUT13
OUT3	8	17	OUT12
OUT4	9	16	OUT11
OUT5	10	15	OUT10
OUT6	11	14	OUT9
OUT7	12	13	OUT8

PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	GND	**Ground signal**
2	DIN	**Serial input data**
3	CLOCK	**Shift input clock for serial input data DIN(Rising Edge Clocking)**
4	STROBE	**Data strobe signal. This pin is a pull-down type.**
5~12 13~20	OUTn	**Constant current outputs, n = 0 ~ 15**
21	PWMCK	**PWM gray scale clock signal. This pin is a pull-up type.**
22	DOUT	**Serial data output**
23	REXT	**Connect the resistor between this pin and GND to set up the constant output current for all the OUTn.**
24	VDD	**Power supply signal (3.3V/5V)**

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BLOCK DIAGRAM

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ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

PARAMETER		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD}	0~7.0	V
Output Voltage		V_{OUT}	-0.5~13.5	V
Output Current		I_{OUT}	450	mA
Input Voltage		V_{IN}	-0.4~V_{DD}+0.4	V
GND Terminal Current		I_{GND}	960	mA
CLOCK Frequency		f_{CK}	25	MHz
PWMCK Frequency		f_{PWMCK}	25	MHz
Power Dissipation	SOP	P_D	1.67	W
	SSOP		1.48	
Thermal Resistance (On PCB, TA = 25)	SOP	Rth(j-a)	75	/W
	SSOP		85	
Operating Temperature		T_{opr}	-40~85	°C
Storage Temperature		T_{stg}	-55~150	°C

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RECOMMENDED OPERATING CONDITIONS

DC CHARACTERISTICS		SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage		V_{DD}	4.5	5	5.5	V
LED Driver Output Voltage		V_{OUT}			13.5	V
Input Voltage	"H" Level	V_{IH}	$0.8V_{DD}$	-	V_{DD}	V
	"L" Level	V_{IL}	GND	-	$0.2V_{DD}$	
Output Voltage	DOUT	V_{OL}	-	-	$0.2V_{DD}$	V
		V_{OH}	$0.8V_{DD}$	-	-	
High Level Output Current		I_{OH}			-1	mA
Low Level Output Current		I_{OL}			1	mA
LED Driver Output Current		I_{OUT}			20	mA
Operating Free-air Temperature Range			-40		85	ºC
AC CHARACTERISTICS		SYMBOL	MIN.	TYP.	MAX.	UNIT
CLOCK Frequency		f_{CK}			25	MHz
PWMCK Frequency	@5V	f_{PWMCK}			25	MHz
	@3.3V	f_{PWMCK}			20	MHz
Pulse Width	CLOCK	t_{WH0} / t_{WL0}	20			ns
	PWMCK	t_{WH1}	40			ns
	STROBE	t_{WH2}	40			ns
Setup Time		t_{setup}	15			ns
Hold Time		t_{hold}	15			ns

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ELECTRICAL CHARACTERISTICS (VDD = 5V, Ta = 25ºC)

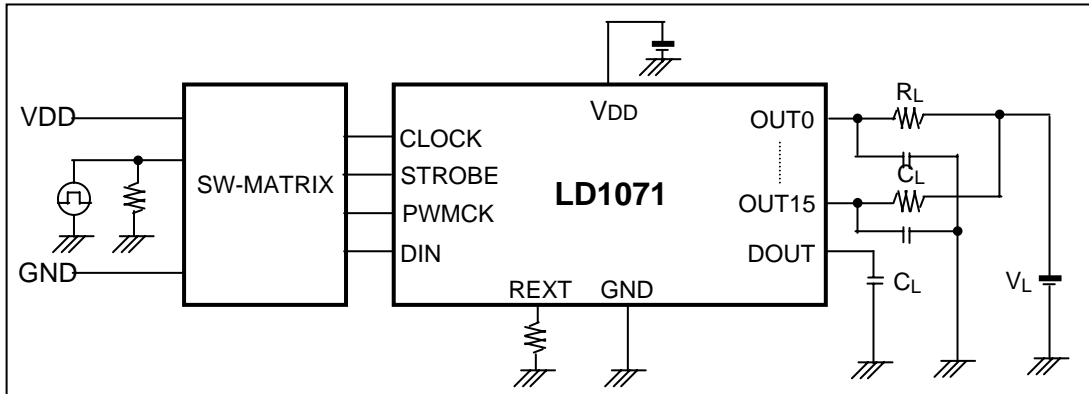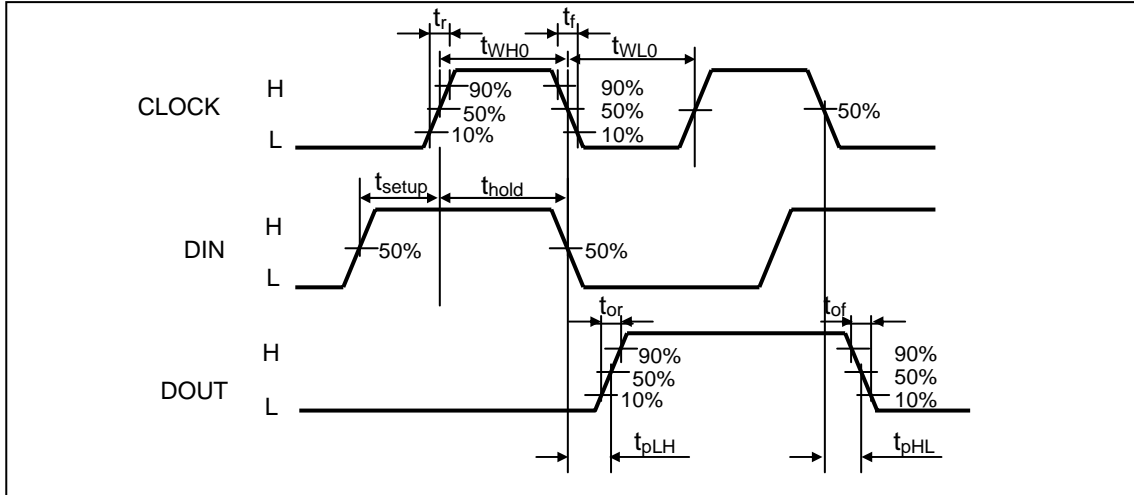| Parameter		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Voltage	H Level	VIH	-	0.7VDD		VDD	V
	L Level	VIL	-	GND		0.3VDD	
Output Leakage Current		IOZ	VOH=6.0V			1	uA
Output Voltage	DOUT	VOL	IOL=1mA			0.2VDD	V
		VOH	IOH=1mA	0.8VDD			
Output Current1 Pin to Pin Deviation		IOLPP1	REXT=500 IOUT=40 , VOUT=1.5V		± 1.5	± 3.0	%
Output Current1 Chip to Chip Deviation		IOLCC1	REXT=500 IOUT=40 , VOUT=1.5V		± 3.0	± 6.0	%
Output Current vs. Supply Voltage Regulation		%/VDD	REXT=500 IOUT=40 , VOUT=1.5V		± 0.5	± 1.0	%/V
Pull Up Resistor		RINUP	-	100	200	400	
Pull Down Resistor		RINDN	-	100	200	400	
Supply Current		IOFF1	REXT=Open, OUTn=OFF REF=FFh, PWM=Gray0	-	0.4	0.8	mA
		IOFF2	REXT=500 , OUTn=OFF REF=FFh, PWM=Gray0	-	4.5	7.0	

(Note) REF : Constant Current Control Value (CR[7:0] of Configuration Register)

DC CHARACTERISTIC TEST CIRCUIT

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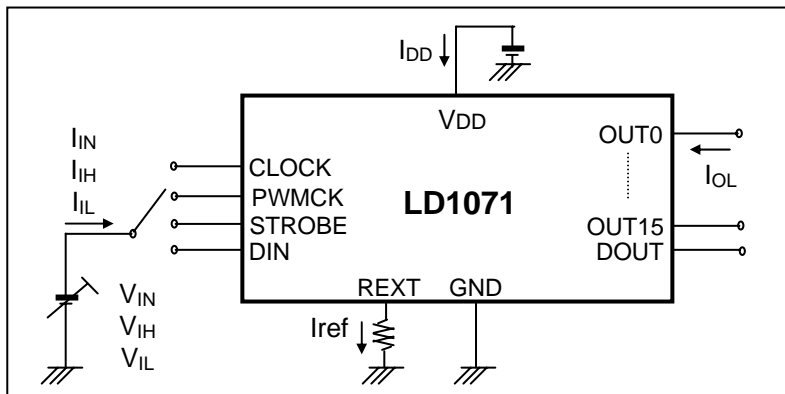
ELECTRICAL CHARACTERISTICS

(VDD = 3.3V, Ta = 25ºC)

Parameter		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Voltage	H Level	VIH	-	0.7VDD		VDD	V
	L Level	VIL	-	GND		0.3VDD	
Output Leakage Current		IOZ	VOH=6.0V			1	uA
Output Voltage	DOUT	VOL	IOL=1mA			0.2VDD	V
		VOH	IOH=1mA	0.8VDD			
Output Current1 Pin to Pin Deviation		IOLPP1	REXT=500 IOUT=36 , VOUT=1.5V		± 1.5	± 3.0	%
Output Current1 Chip to Chip Deviation		IOLCC1	REXT=500 IOUT=36 , VOUT=1.5V		± 3.0	± 6.0	%
Output Current vs. Supply Voltage Regulation		%/VDD	REXT=500 IOUT=36 , VOUT=1.5V		± 0.5	± 1.0	%/V
Pull Up Resistor		RINUP	-	150	300	500	
Pull Down Resistor		RINDN	-	150	300	500	
Supply Current		IOFF1	REXT=Open, OUTn=OFF REF=FFh, PWM=Gray0	-	0.4	0.6	mA
		IOFF2	REXT=500 , OUTn=OFF REF=FFh, PWM=Gray0	-	4.5	7.0	

(Note) REF : Constant Current Control Value (CR[7:0] of Configuration Register)

DC CHARACTERISTIC TEST CIRCUIT

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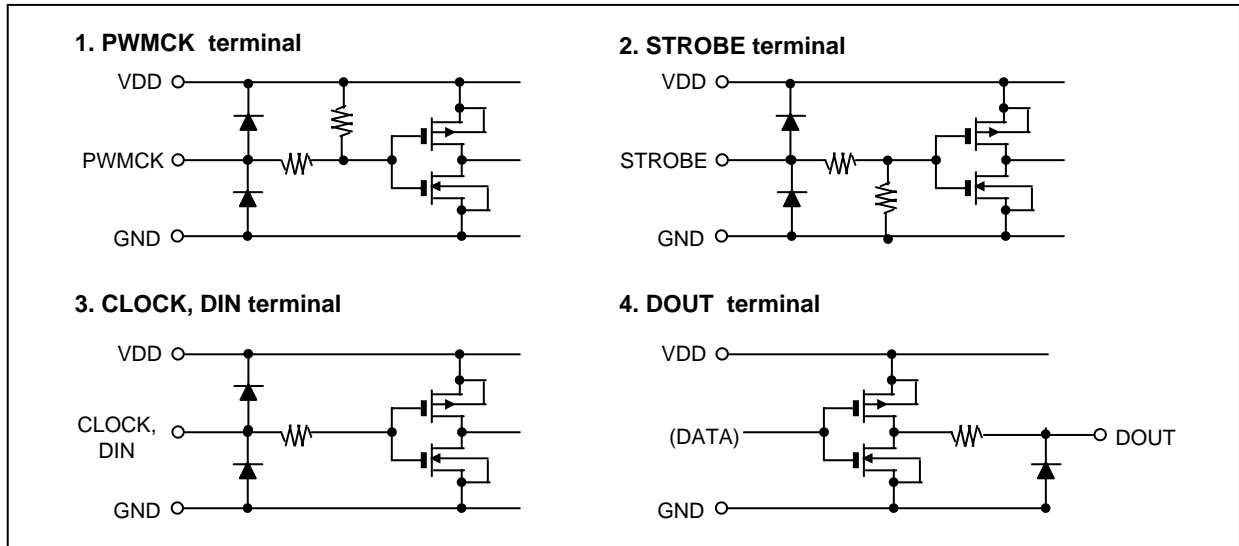16 Channel Output LED Driver with 14 bit PWM Controller
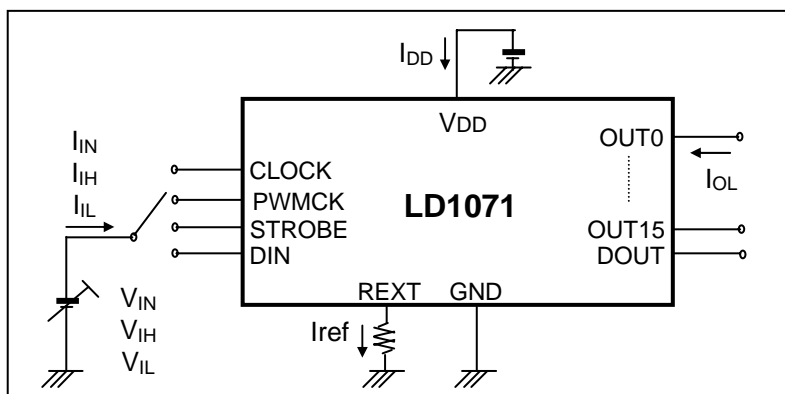
AC CHARACTERISTIC TEST CIRCUIT

SWITCHING CHARACTERISTICS

(Ta = 25°C unless otherwise noted)

PARAMETER		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	CLOCK-DOUT	t_{pLH}		-	10	20	ns
	PWMCK-OUTn			-	-	50	
Propagation Delay Time ("H" to "L")	CLOCK-DOUT	t_{pHL}		-	10	20	ns
	PWMCK-OUTn			-	-	30	
Maximum CLOCK Frequency		f_{CKMAX} (*1)		-	10	25	MHz
Maximum PWMCK Frequency		$f_{PWMCKMAX}$ (*1)		-	8	25	MHz
Pulse Width	CLOCK	t_{WH0} / t_{WL0}	V_{DD} = 5.0V V_{IH} = VDD V_{IL} = GND f_{CK} = 10MHz R_{EXT} = 1590 I_{OUT} = 19.1mA C_L = 10.0pF R_L = 150 VL = 4.5V	15	20	-	ns
	PWMCK	t_{WH1}		15	20	-	ns
	STROBE	t_{WH2}		15	20	-	ns
Data Set Up Time		$t_{setup (D)}$		10	15	-	ns
Data Hold Time		$t_{hold (D)}$		10	15	-	
STROBE Set Up Time	LH	$t_{STB}setup$		10	15	-	ns
	HL			10	15	-	
STROBE Hold Time	LH	$t_{STB}hold$		10	-	-	ns
	HL			10	-	-	
Maximum Clock Rise Time		t_r		-	-	30	ns
Maximum Clock Fall Time		t_f		-	-	30	
Output Rise Time (OUTn)		t_{or}		-	-	30	ns
Output Fall Time (OUTn)		t_{of}		-	-	30	
Global Latch Set Up Time		tglc		20	-	-	ns

*1 : Cascade Operation

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TIMING WAVEFORM

CLOCK-DIN-DOUT

CLOCK-STROBE

PWMCK-OUTn

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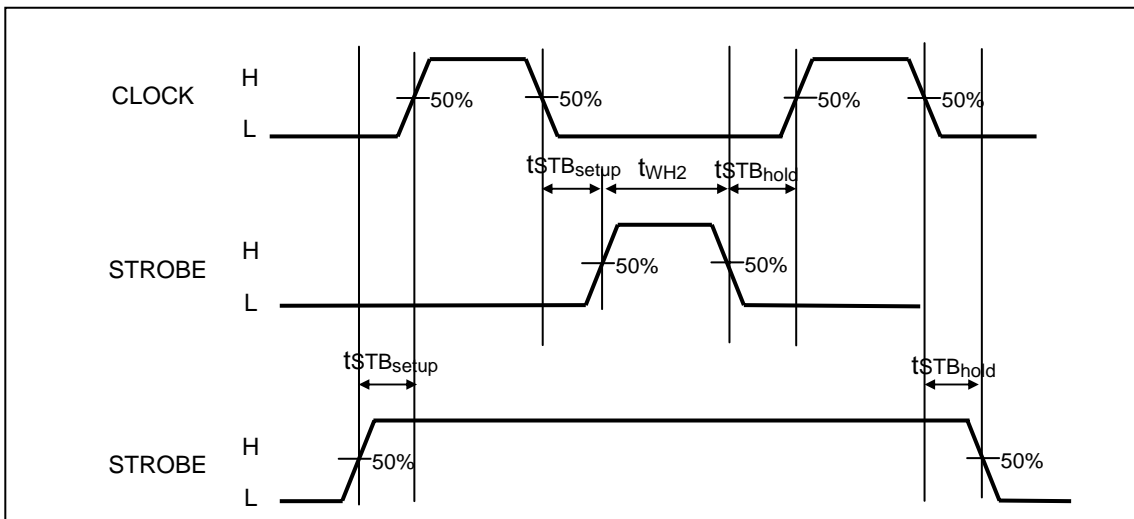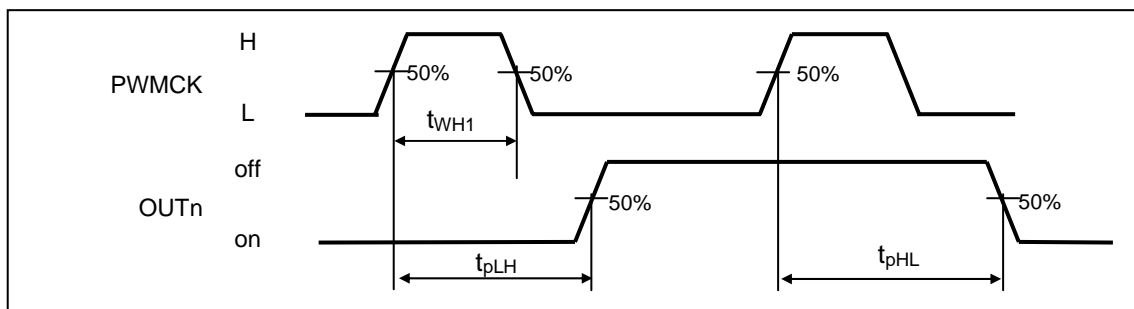
EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

1. PWMCK terminal

VDD

PWMCK

GND

2. STROBE terminal

VDD

STROBE

GND

3. CLOCK, DIN terminal

VDD

CLOCK,
DIN

GND

4. DOUT terminal

VDD

(DATA)

GND

DOUT

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FUNCTIONAL DESCRIPTION

COMMAND TABLE

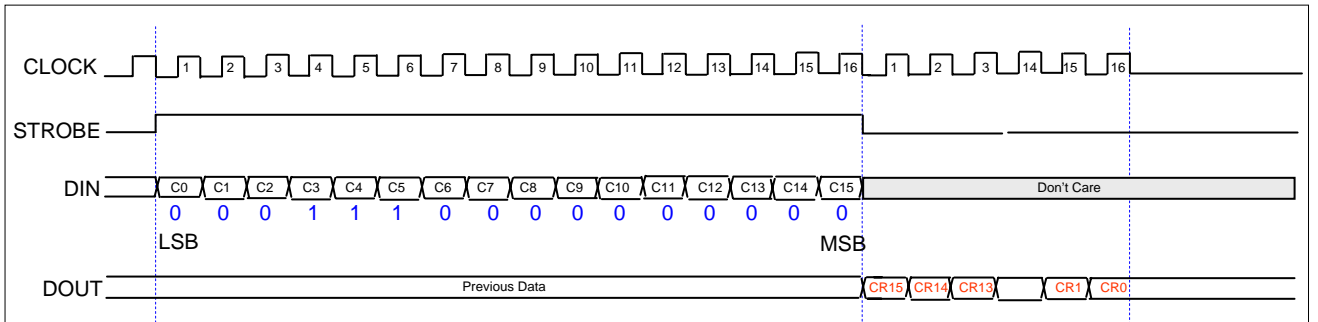| Command Name	Command Value	Description
Software Reset Command	0001h	This command should be issued after power supply input. The Configuration Register, internal shift register, Display Data Register will be cleared with '0' states.
Configuration Register Write Command	0034h	This command is used to update the contents of Configuration Register.
Configuration Register Read Command	0038h	This command is used to read the status of Configuration Register.
Error Status Read Command	003Ch	This command is used to check the 'Open/Short' error status of LED.
Display Data Write Command	0084h	This command is used to write the display image data into LED driver IC for display system.
Global Latch Command	-	This command is used to deliver the internal display data register outputs latched by Display Data Write Command to the internal PWM comparator to make an output current. The Global Latch Command should be transferred after sending the final display data you want. The Global Latch Command has no command value but it needs a special execution sequence.

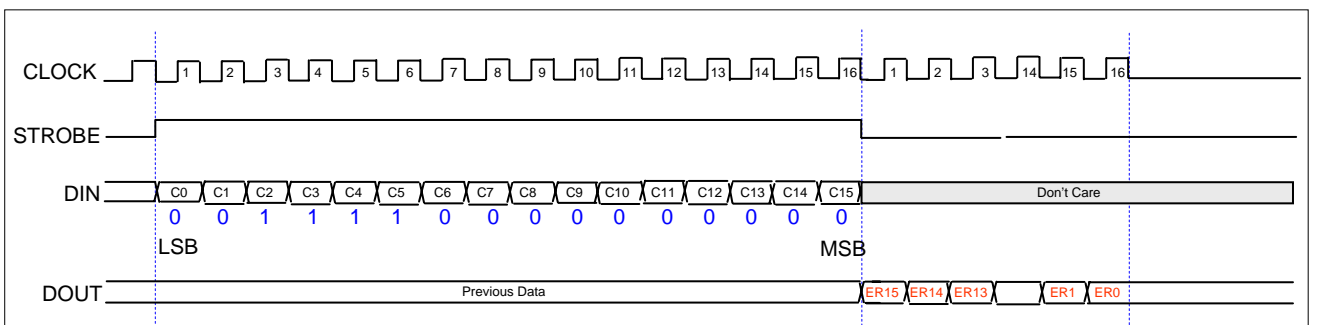## TIMING DIAGRAM OF COMMAND CONTROL

Software Reset Command (0001h)
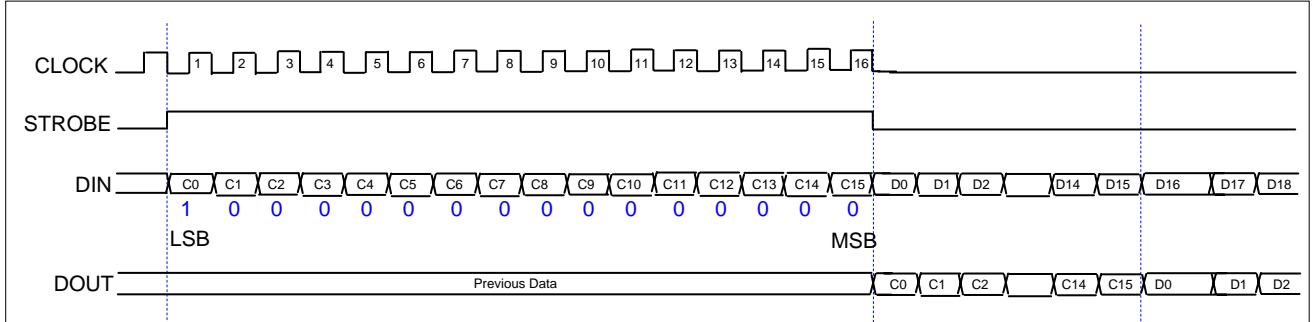
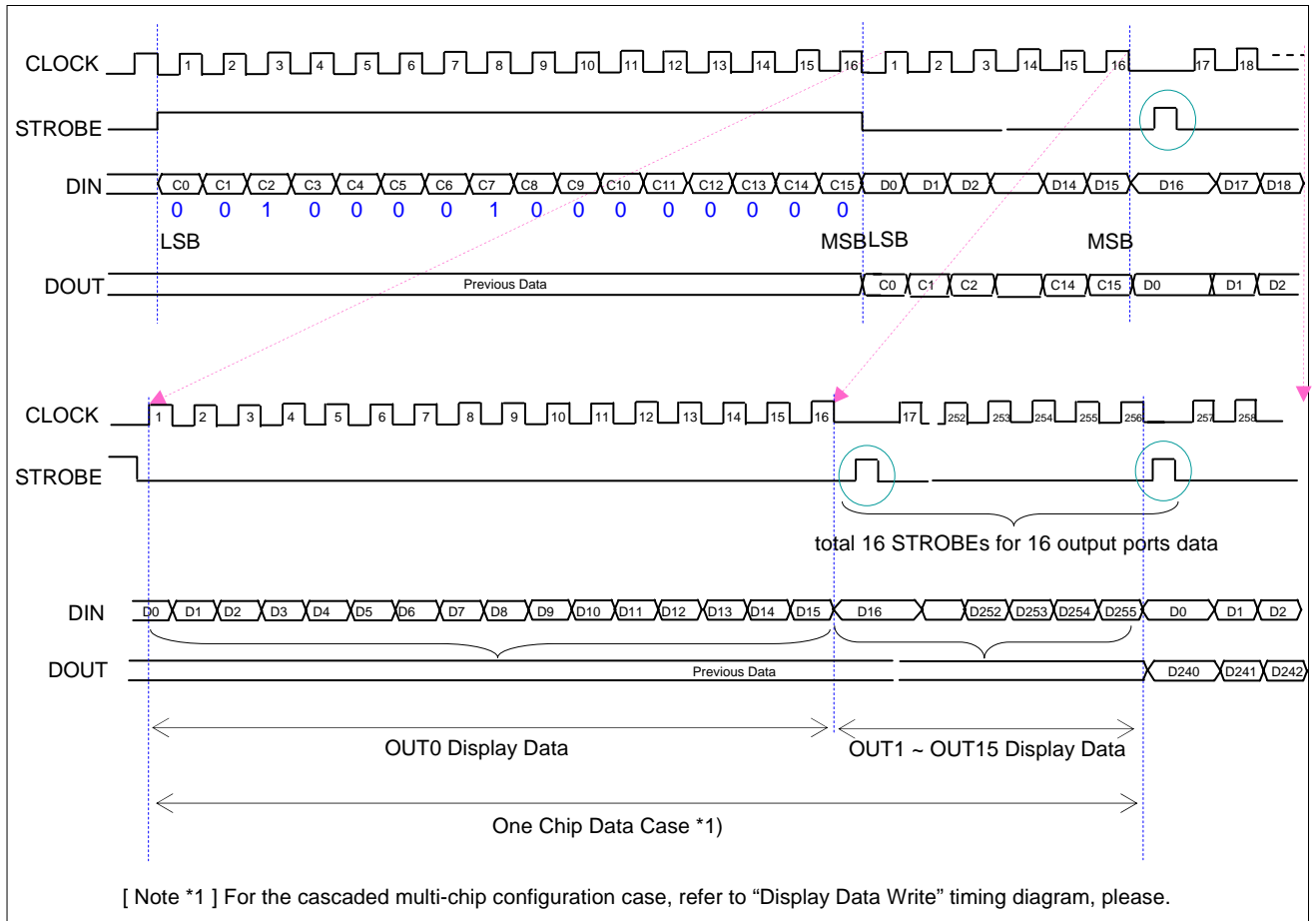### Configuration Register Write Command (0034h)
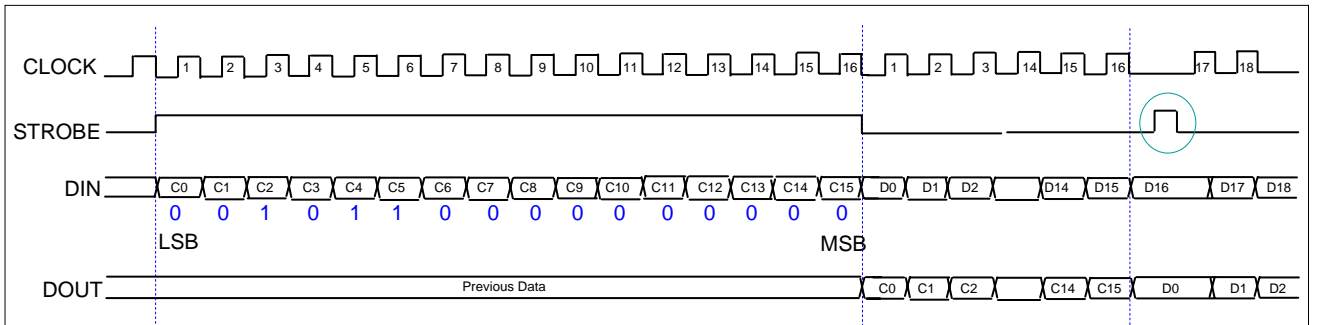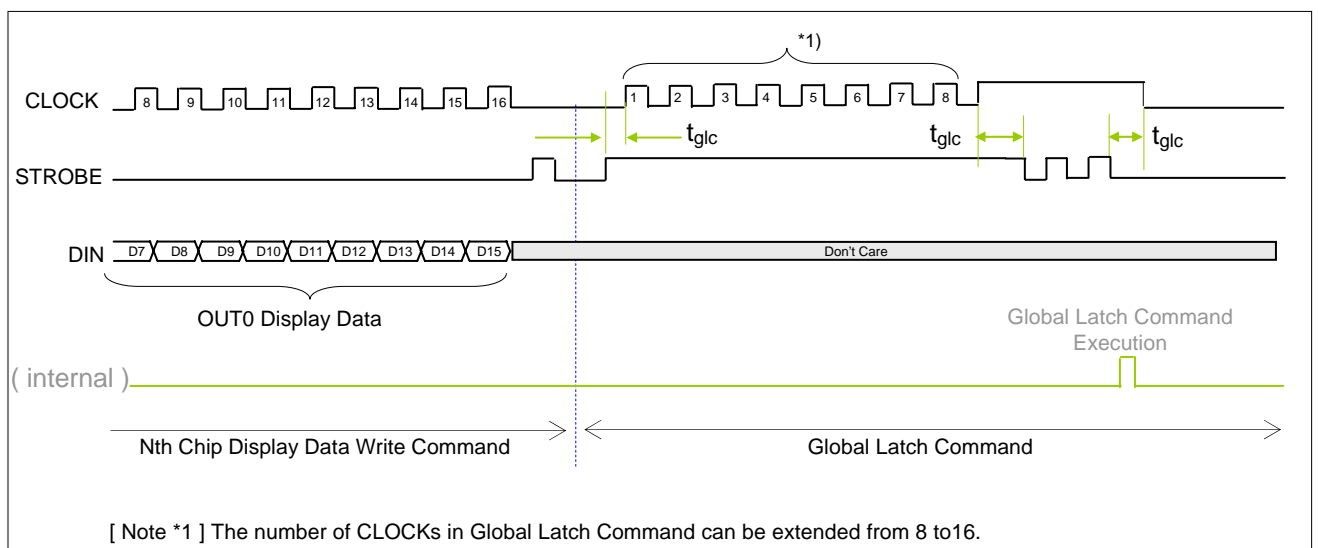

Configuration Register Read Command (0038h)
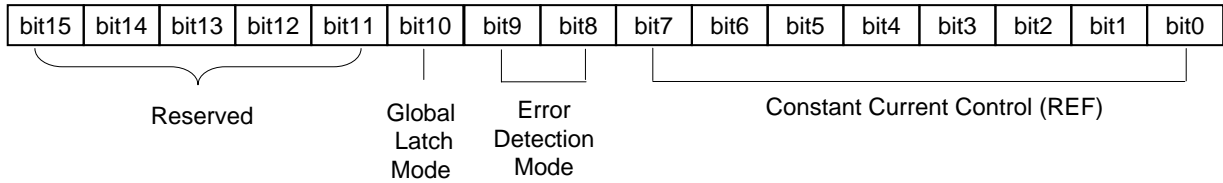

Error Status Read Command (003Ch)

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Display Data Write Command (0084h)

[Note *1] For the cascaded multi-chip configuration case, refer to "Display Data Write" timing diagram, please.

Global Latch Command

[Note *1] The number of CLOCKs in Global Latch Command can be extended from 8 to16.

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CONFIGURTION REGISTER (CR[15:0])

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0

Reserved   Global Latch Mode   Error Detection Mode   Constant Current Control (REF)

Constant Current Control (CR[7:0] Default 00h)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Current Value
0	0	0	0	0	0	0	0	IOUT/256
0	0	0	0	0	0	0	1	IOUT*2/256
-	-	-	-	-	-	-	-	-
0	1	1	1	1	1	1	1	IOUT*128/256
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	1	0	IOUT*255/256
1	1	1	1	1	1	1	1	IOUT

The IOUT is a constant current of OUTn port which is determined by REXT resistor.

Error Detection Mode (CR[9:8] Default 00b)

bit9	bit8	Error Mode
0	0	Check Disable
0	1	Open Check
1	0	Short Check
1	1	Check Disable

Global Latch Mode (CR[10] Default 0b)

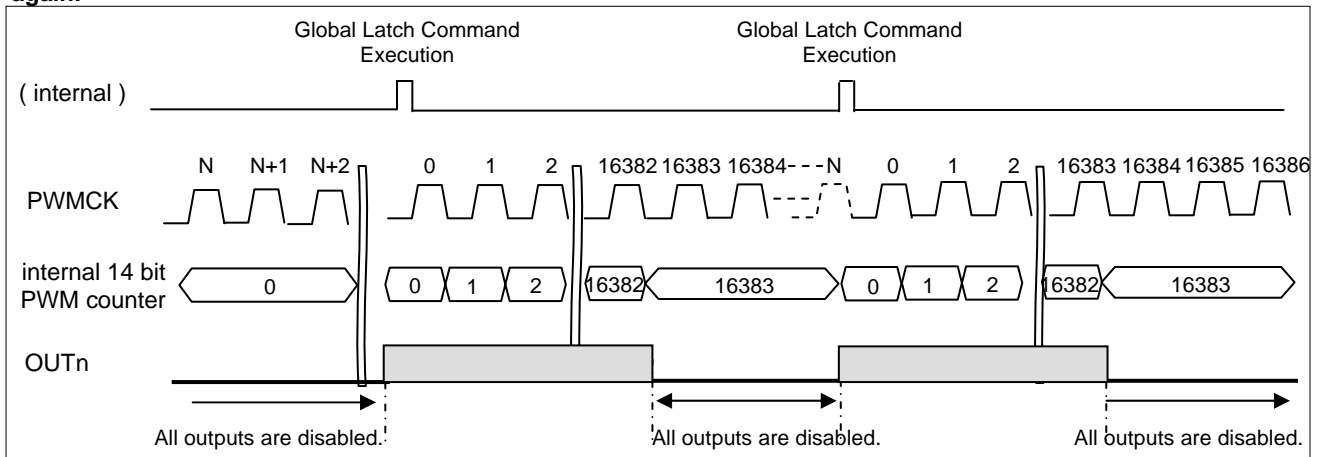| bit10	Global Latch Mode
0	One Shot
1	Automatic Synchronization

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SYNCHRONIZATION FOR PWM COUNTING

The LD1071's Global Latch Command supports two kinds of synchronization mode for PWM counting. The default mode is One Shot Mode(Configuration Register bit10=0) and the other mode is Automatic Synchronization Mode(Configuration Register bit10=1).

One Shot Mode (Default)

When Global Latch Command is executed in this mode, the LD1071 will update the next image data into output ports immediately, no matter what the counting status of previous image data is. The 14 bit internal PWM Counter is initialized with 0000h and the internal PWM counter starts counting with PWMCK clock. When the internal PWM counter value is reached to FFFFh, the internal PWM counter stops the counting even next PWMCK clock is inputting continuously. As a result, all the outputs will be stopped after finishing one internal PWM display cycle (16384 PWMCK clocks). Only the next Global Latch Command can initialize the counting again.

Automatic Synchronization Mode

When Global Latch Command is executed in this mode(Global Latch Mode=1), the LD1071 will update the next image data into output ports immediately, no matter what the counting status of previous image data is. When the internal PWM counter value is reached to FFFFh, if there is no Global Latch Command, the LD1071 automatically loads the previous image data into output ports at next 16384th PWMCK clock again. So in this mode, output ports will be automatically updated at every 16384 PWMCK clocks with previous data.

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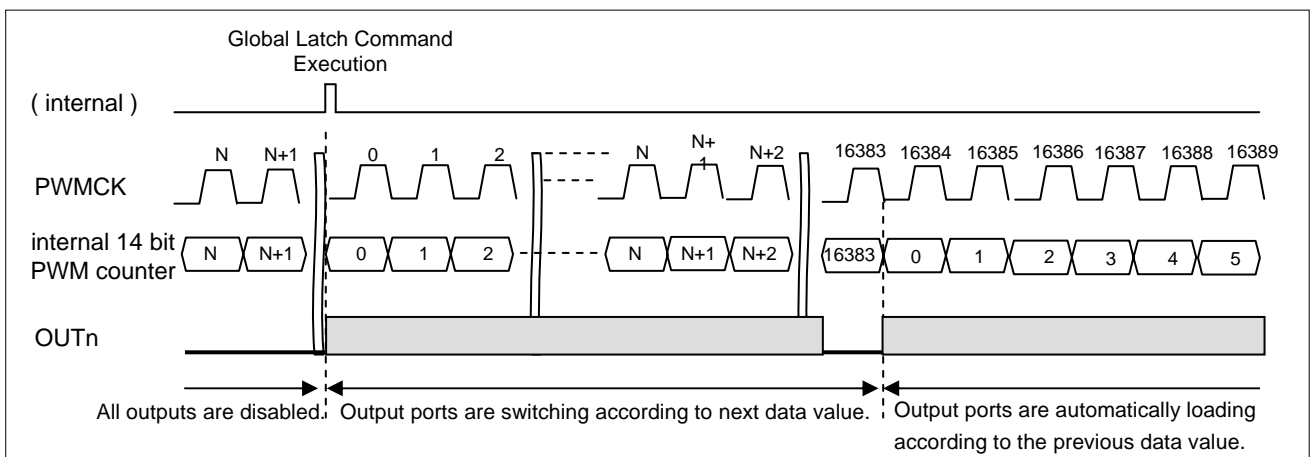
WRITING THE DISPLAY DATA

With the 16 bit data, all output ports can be built with 16,384 gray scales. The 16-bit input shift register latches 16 times of gray scale data into each data buffer with Display Data Write Command sequentially . Finally Global Latch Command will load the 256 bit internal data buffers with LSB first into from output port 15(OUT15) to output port 0(OUT0). Even 16 bit display data for each port should be transferred, only 14 bits data are valid for gray scale image (bit[13:0]) and the high 2bits(bit[15:14]) are reserved. For the detail timing and sequence, refer to "Display Data Write Command" and "Global Latch Command" which is described on page 14, please.
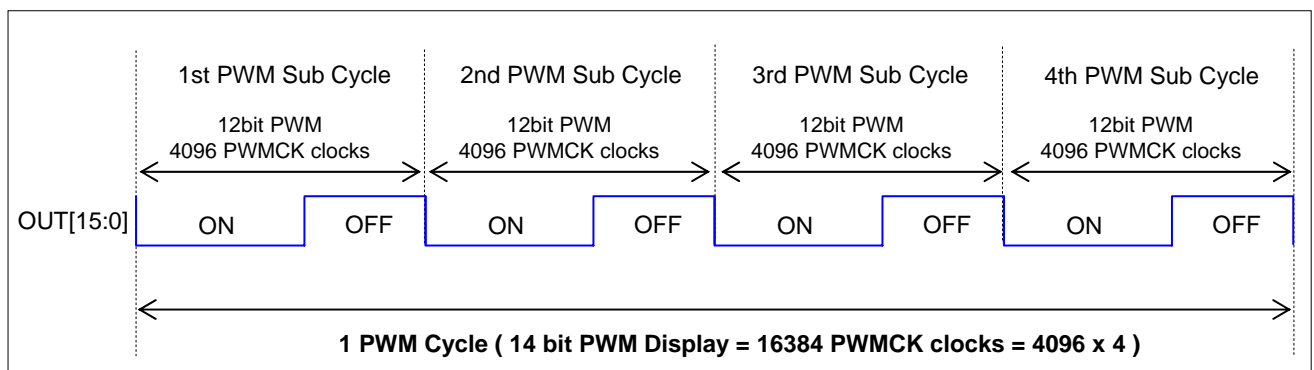
PWM DISPLAY CYCLE

The LD1071 implements the 14 bit gray level of each output port using the 4 PWM sub cycles. Each PWM sub cycle is consisted of 12 bit PWMCK clocks. This enhancement provides a excellent energy distribution in lighting the LED and increases the visual refresh rate and reduces the flickers.

D[15:14]   : Reserved
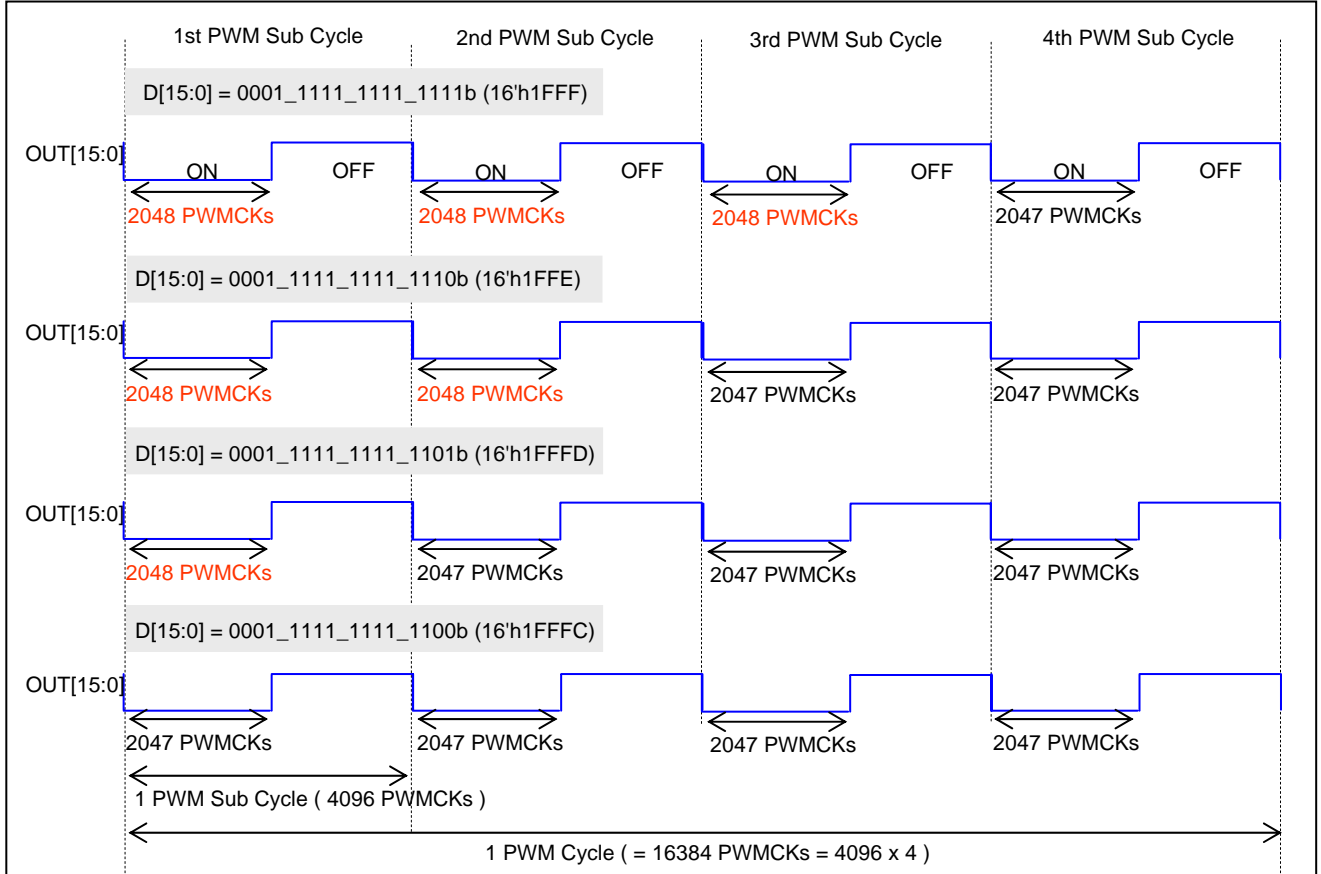D[13:0]   : Display Data(14 bit Gray Scale Data)

        bit[13:2]   : 12bit PWM Comparing Data

        bit[1: 0]   : PWM Insert data
          1 1   : one pulse is inserted in 1st, 2nd and 3rd PWM Sub Cycle
          1 0   : one pulse is inserted in 1st and 2nd PWM Sub Cycle
          0 1   : one pulse is inserted in 1st PWM Sub Cycle
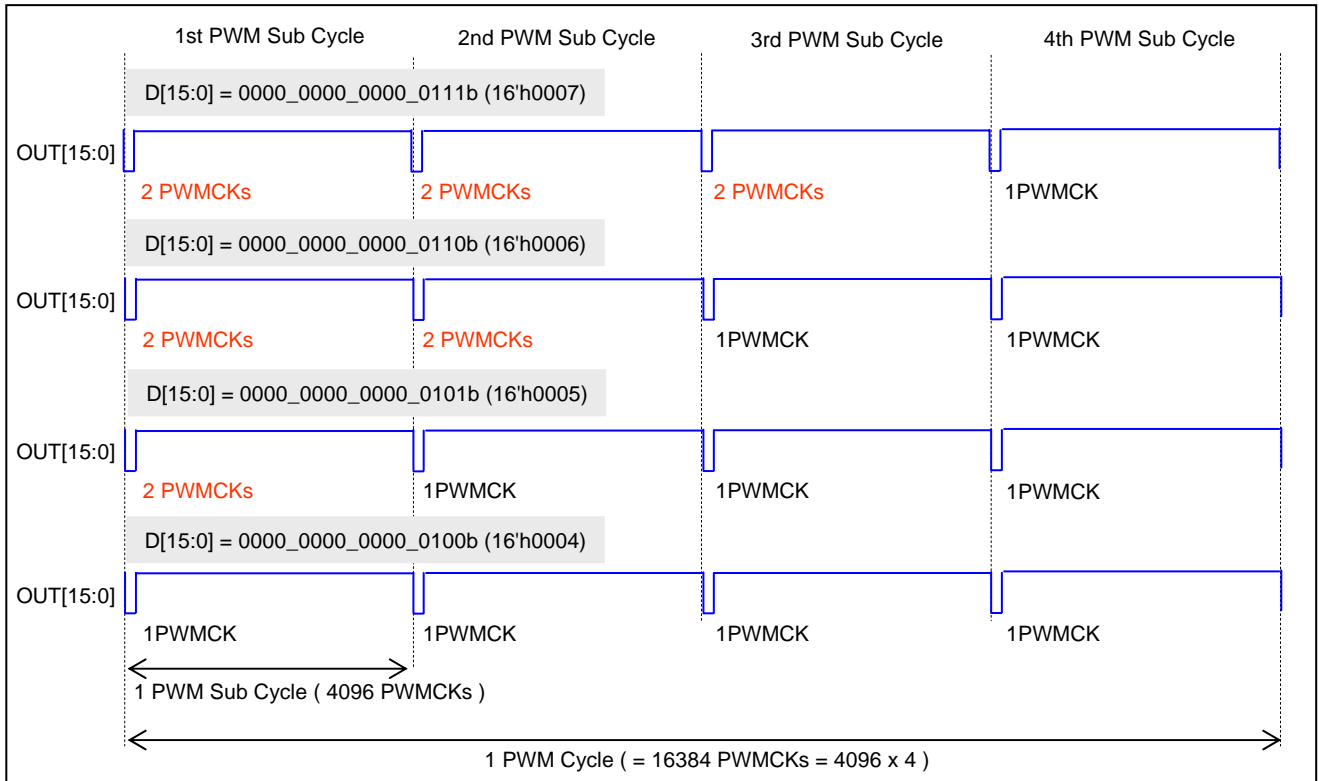   0 0   : Not inserted

1st PWM Sub Cycle	2nd PWM Sub Cycle	3rd PWM Sub Cycle	4th PWM Sub Cycle
12bit PWM 4096 PWMCK clocks	12bit PWM 4096 PWMCK clocks	12bit PWM 4096 PWMCK clocks	12bit PWM 4096 PWMCK clocks

OUT[15:0] ON OFF ON OFF ON OFF ON OFF

1 PWM Cycle (14 bit PWM Display = 16384 PWMCK clocks = 4096 x 4)

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The following examples show the PWM timing diagram for different display data.

(Case 1)

(Case 2)

1st PWM Sub Cycle	2nd PWM Sub Cycle	3rd PWM Sub Cycle	4th PWM Sub Cycle

D[15:0] = 0000_0000_0000_0111b (16'h0007)

OUT[15:0]

2 PWMCKs   2 PWMCKs   2 PWMCKs   1PWMCK

D[15:0] = 0000_0000_0000_0110b (16'h0006)

OUT[15:0]

2 PWMCKs   2 PWMCKs   1PWMCK   1PWMCK

D[15:0] = 0000_0000_0000_0101b (16'h0005)

OUT[15:0]

2 PWMCKs   1PWMCK   1PWMCK   1PWMCK

D[15:0] = 0000_0000_0000_0100b (16'h0004)

OUT[15:0]

1PWMCK   1PWMCK   1PWMCK   1PWMCK

1 PWM Sub Cycle (4096 PWMCKs)

1 PWM Cycle (= 16384 PWMCKs = 4096 x 4)

(Case 3)

1st PWM Sub Cycle	2nd PWM Sub Cycle	3rd PWM Sub Cycle	4th PWM Sub Cycle

D[15:0] = 0000_0000_0000_0011b (16'h0003)

OUT[15:0]

1PWMCK   1PWMCK   1PWMCK

D[15:0] = 0000_0000_0000_0010b (16'h0002)

OUT[15:0]

1PWMCK   1PWMCK

D[15:0] = 0000_0000_0000_0001b (16'h0001)

OUT[15:0]

1PWMCK

D[15:0] = 0000_0000_0000_0000b (16'h0000)

OUT[15:0]

1 PWM Sub Cycle (4096 PWMCKs)

1 PWM Cycle (= 16384 PWMCKs = 4096 x 4)

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(Case 4)

	1st PWM Sub Cycle	2nd PWM Sub Cycle	3rd PWM Sub Cycle	4th PWM Sub Cycle

D[15:0] = 0011_1111_1111_1111b (16'h3FFF)

OUT[15:0] 4096 PWMCKs   4096 PWMCKs   4096 PWMCKs   4095 PWMCKs

D[15:0] = 0011_1111_1111_1110b (16'h3FFE)

OUT[15:0] 4096 PWMCKs   4096 PWMCKs   4095 PWMCKs   4095 PWMCKs

D[15:0] = 0011_1111_1111_1101b (16'h3FFD)

OUT[15:0] 4096 PWMCKs   4095 PWMCKs   4095 PWMCKs   4095 PWMCKs

D[15:0] = 0011_1111_1111_1100b (16'h3FFC)

OUT[15:0] 4095 PWMCKs   4095 PWMCKs   4095 PWMCKs   4095 PWMCKs

1 PWM Sub Cycle (4096 PWMCKs)

1 PWM Cycle (= 16384 PWMCKs = 4096 x 4)

(Case 5)

	1st PWM Sub Cycle	2nd PWM Sub Cycle	3rd PWM Sub Cycle	4th PWM Sub Cycle

D[15:0] = 0011_1111_1111_1011b (16'h3FFB)

OUT[15:0] 4095 PWMCKs   4095 PWMCKs   4095 PWMCKs   4094 PWMCKs

D[15:0] = 0011_1111_1111_1010b (16'h3FFA)

OUT[15:0] 4095 PWMCKs   4095 PWMCKs   4094 PWMCKs   4094 PWMCKs

D[15:0] = 0011_1111_1111_1001b (16'h3FF9)

OUT[15:0] 4095 PWMCKs   4094 PWMCKs   4094 PWMCKs   4094 PWMCKs

D[15:0] = 0011_1111_1111_1000b (16'h3FF8)

OUT[15:0] 4094 PWMCKs   4094 PWMCKs   4094 PWMCKs   4094 PWMCKs

1 PWM Sub Cycle (4096 PWMCKs)

1 PWM Cycle (= 16384 PWMCKs = 4096 x 4)

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ERROR DETECTION

The LD1071 will be able to detect the error status of LED such as open/short error. This function can be entered by setting the bits of Error Detection Mode(CR[9:8]) as 01b(Open Detection) or 10b(Short Detection). The correct meaning of error is defined as follows;

- Open Error : Output port(OUTn) is not connected to LED.

- Short Error : Output port(OUTn) is shorted to GND.

	Error Detection Code		
	Output Port status	Error Detection Voltage	Meaning
Open Check	OFF	OUT Voltage > 0.8V	Normal
		OUT Voltage < 0.8V	Open Error
Short Check	OFF	OUT Voltage > 0.8V	Normal
		OUT Voltage < 0.8V	Short Error

Error Status Register (ER[15:0])
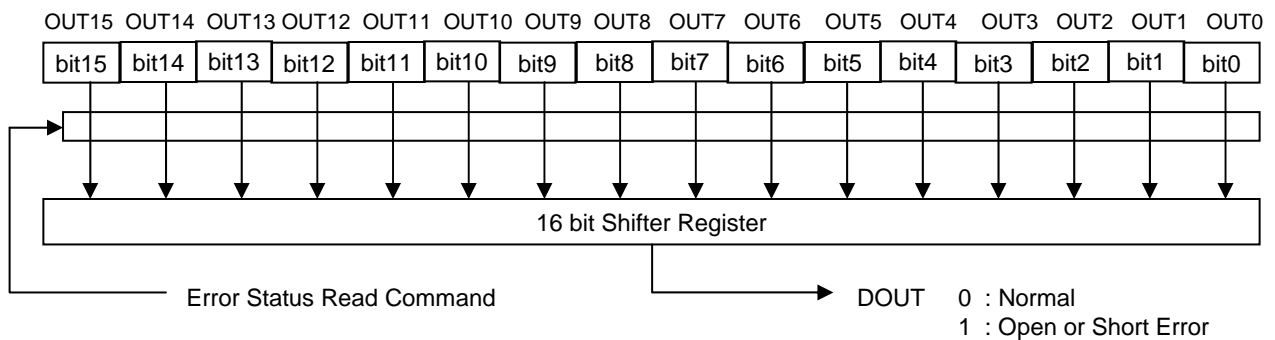
Timing Diagram of Error Status Check

The next timing diagram shows the sequence of error status read operation. The actual error status is read with MSB first after execution of Error Status Read Command. First of all, in order to read the error status, all the output ports (OUT15~OUT0) should be off. So you need some pre-processing for error status read. The flow chart will be provided on next page.
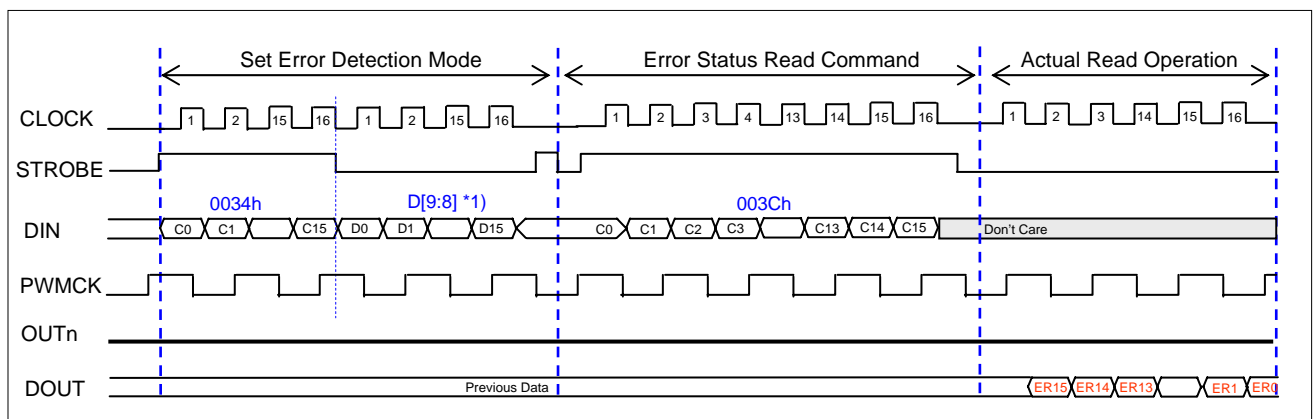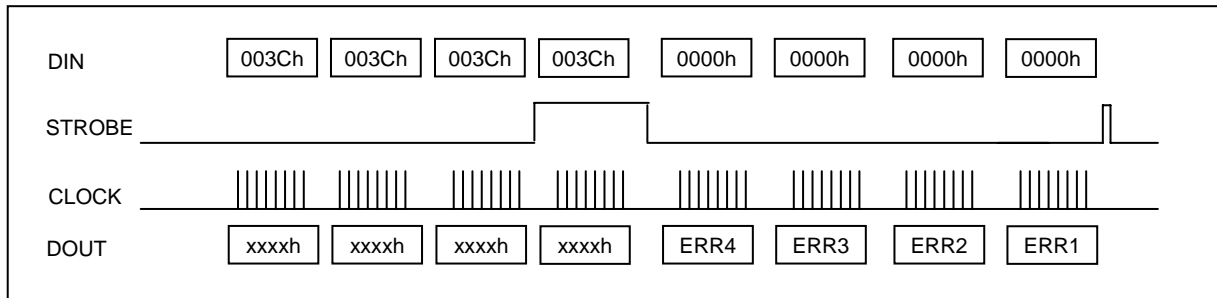

Note *1) In order to keep the Constant Current Value(CR[7:0]) and Global Latch Mode(CR[10]) correctly, maybe you need to read the Configuration Register through the Configuration Register Read Command(0038h) prior to set Error Detection Mode.
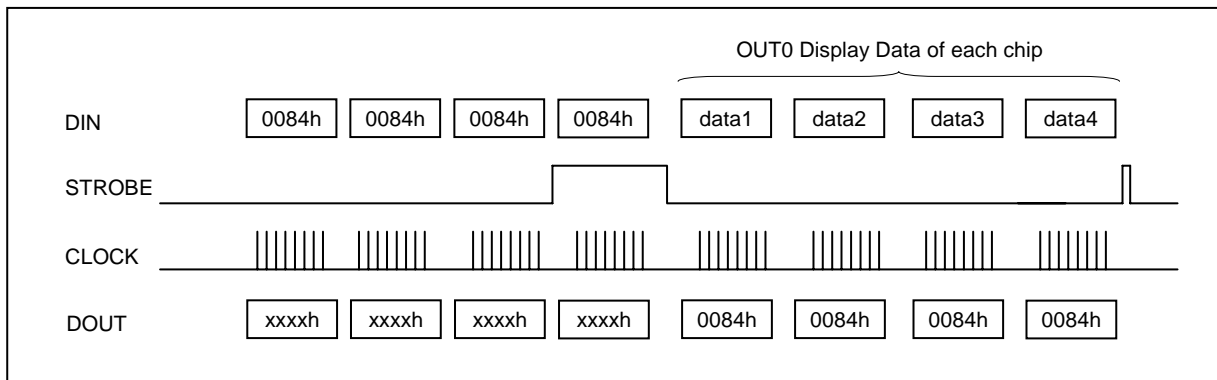
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Start

Set All Output Ports OFF

1) Set Display Data Write Command(0084h) with 0000h Data
2) Run totally 16 times for all the 16 output ports OFF (1 Chip)
3) If N-chips are cascaded, repeat 1) and 2)'s operations N times

Run Global Latch Command

Set Error Detection Mode

1) Set Configuration Register Write Command(0034h)
   - CR[9:8] = 01 : Open Detection,   10 : Short Detection
2) If N-chips are cascaded, repeat 1)'s operations N times

Run Error Status Read Command

1) Set Error Status Read Command(003Ch)
2) If N-chips are cascaded, repeat 1)'s operations N times

Input CLOCKs

1) Input 16 CLOCKs to read the error status of chip1.
   The error status of port15 will be outputted at fall edge first.
2) If N-chips are cascaded, input N x 16 CLOCKs to read error
   status of all ports(N x 16 ports). The data of last chip(Nth
   chip) will be outputted first.

End

Flow Chart of Error Status Check

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COMMAND SETTING GUIDE FOR MULTI-CHIP CASCADE CONFIGURATION
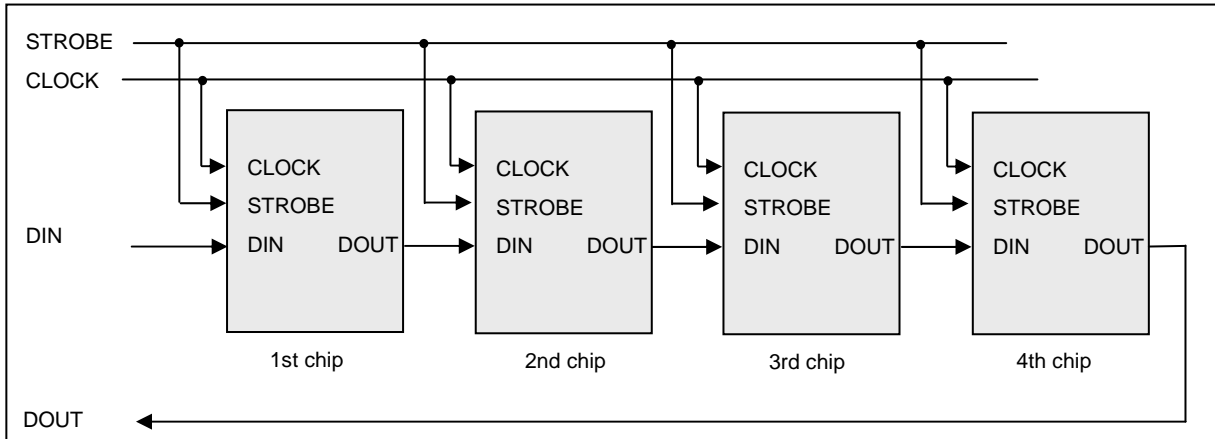
Configuration Register Write(Current Control)
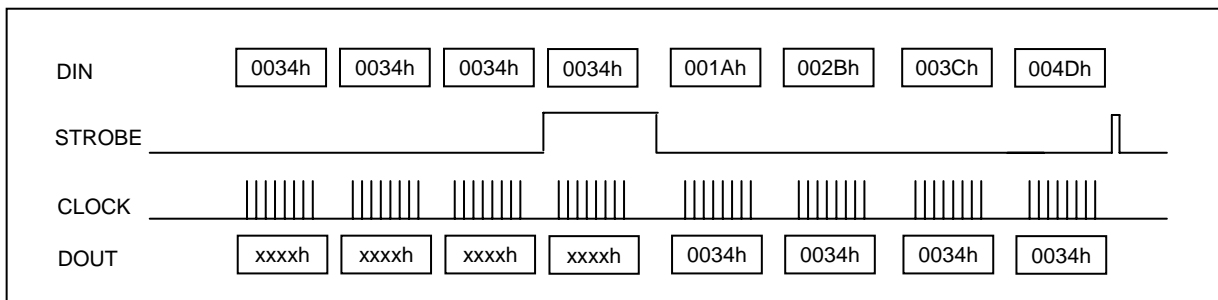
Configuration Register Read
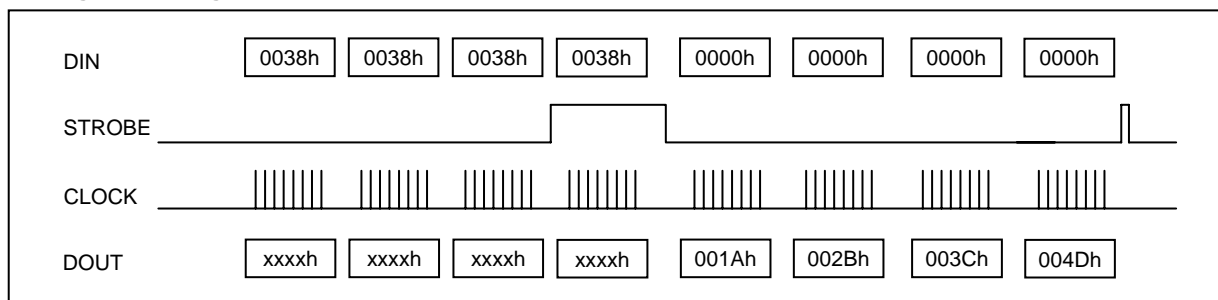
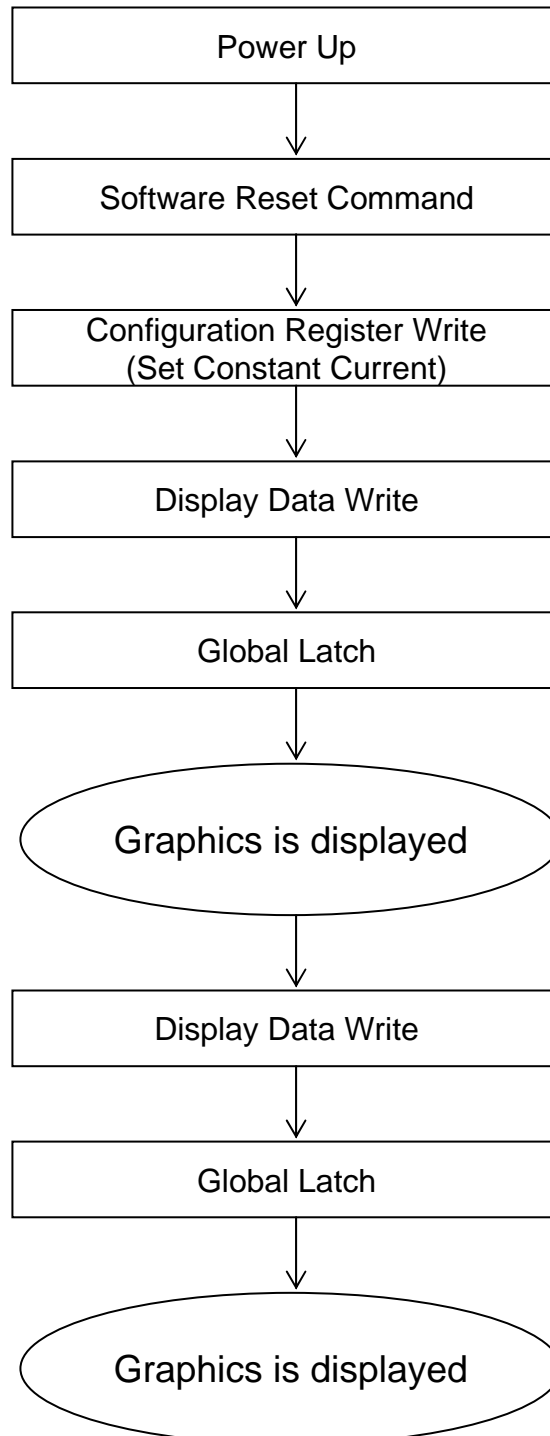**Configuration Register Write (Error Detection Enable)**

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Error Status Read

DIN	003Ch	003Ch	003Ch	003Ch	0000h	0000h	0000h	0000h
STROBE								
CLOCK								
DOUT	xxxxh	xxxxh	xxxxh	xxxxh	ERR4	ERR3	ERR2	ERR1

Display Data Write

OUT0 Display Data of each chip

DIN	0084h	0084h	0084h	0084h	data1	data2	data3	data4
STROBE								
CLOCK								
DOUT	xxxxh	xxxxh	xxxxh	xxxxh	0084h	0084h	0084h	0084h

Software Reset & NOP Operation

	Software Reset				NOP Operation			
DIN	0001h	0001h	0001h	0001h	0000h	0000h	0000h	0000h
STROBE								
CLOCK								
DOUT	xxxxh	xxxxh	xxxxh	xxxxh	xxxxh	xxxxh	xxxxh	xxxxh
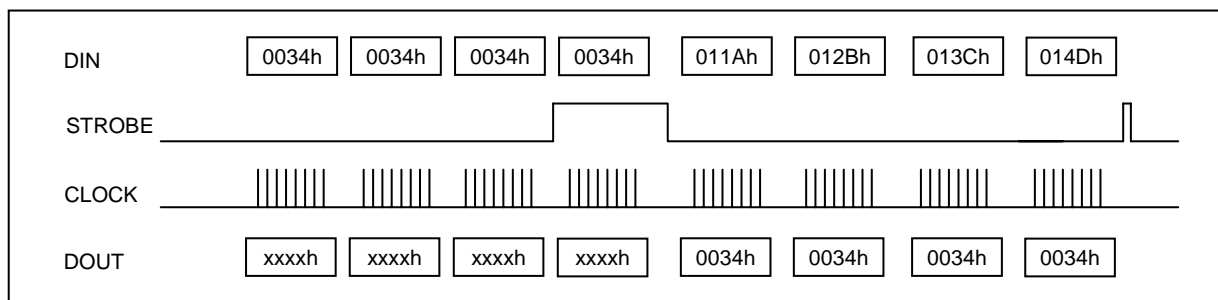
RECOMMENDATION OF GLOBAL SEQUENCE

```
┌─────────────────────────────────┐
│           Power Up              │
└─────────────────────────────────┘
                │
                ▼
┌─────────────────────────────────┐
│      Software Reset Command     │
└─────────────────────────────────┘
                │
                ▼
┌─────────────────────────────────┐
│   Configuration Register Write  │
│     (Set Constant Current)      │
└─────────────────────────────────┘
                │
                ▼
┌─────────────────────────────────┐
│        Display Data Write       │
└─────────────────────────────────┘
                │
                ▼
┌─────────────────────────────────┐
│          Global Latch           │
└─────────────────────────────────┘
                │
                ▼
      ⬭ Graphics is displayed ⬭
                │
                ▼
┌─────────────────────────────────┐
│        Display Data Write       │
└─────────────────────────────────┘
                │
                ▼
┌─────────────────────────────────┐
│          Global Latch           │
└─────────────────────────────────┘
                │
                ▼
      ⬭ Graphics is displayed ⬭
```

The first command should be issued after 0.1ms from Power-Up.

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SETTING OUTPUT CURRENT

The output current is determined by an external resistor. The relationship between I_{OUT} and R_{EXT} is as follows;

When VDD = 5V	When VDD = 3.3V
$I_{OUT}[A] = \{1.06/(120+R_{EXT})\} * S * 61.4$ where $S = (REF+1)/512$	$I_{OUT}[A] = \{1.06/(150+R_{EXT})\} * S * 57.6$ where $S = (REF+1)/512$

- R_{EXT} : External Resistor[ ]
- REF : Constant Current Control (0 ~ 255, CR[7:0] of Configuration Register)

Because the default REF value(CR[7:0]) of Configuration Register(0034h) for current control is 00h, if you want to set the output current through changing the REXT value with following graph, do not forget to write the CR[7:0] of Configuration Register with 'FFh', please.
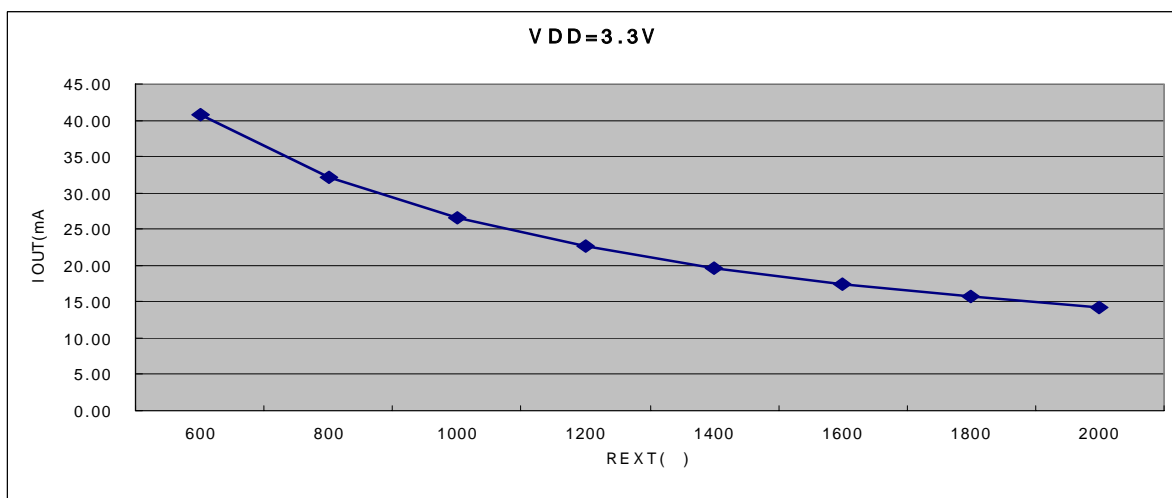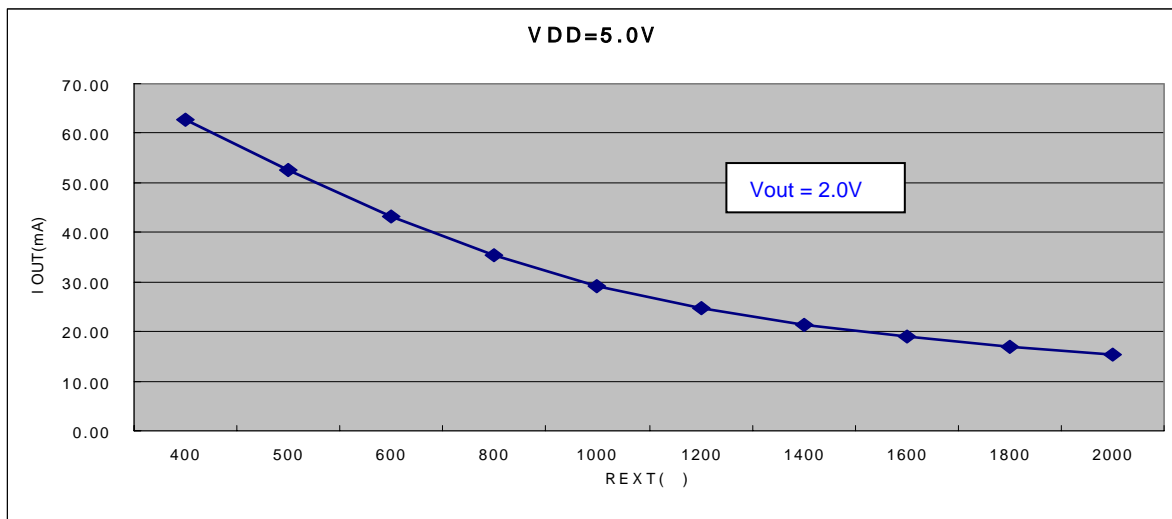
[Note] When VDD is 3.3V, in order to guarantee the accurate output current, do not set the Iout to over 40mA,

please.

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CONSTANT OUTPUT CURRENT

The LD1071 provides a constant current output characteristics for LED display application. The pin to pin deviation is max +/- 3% and chip to chip deviation is max +/- 6%.
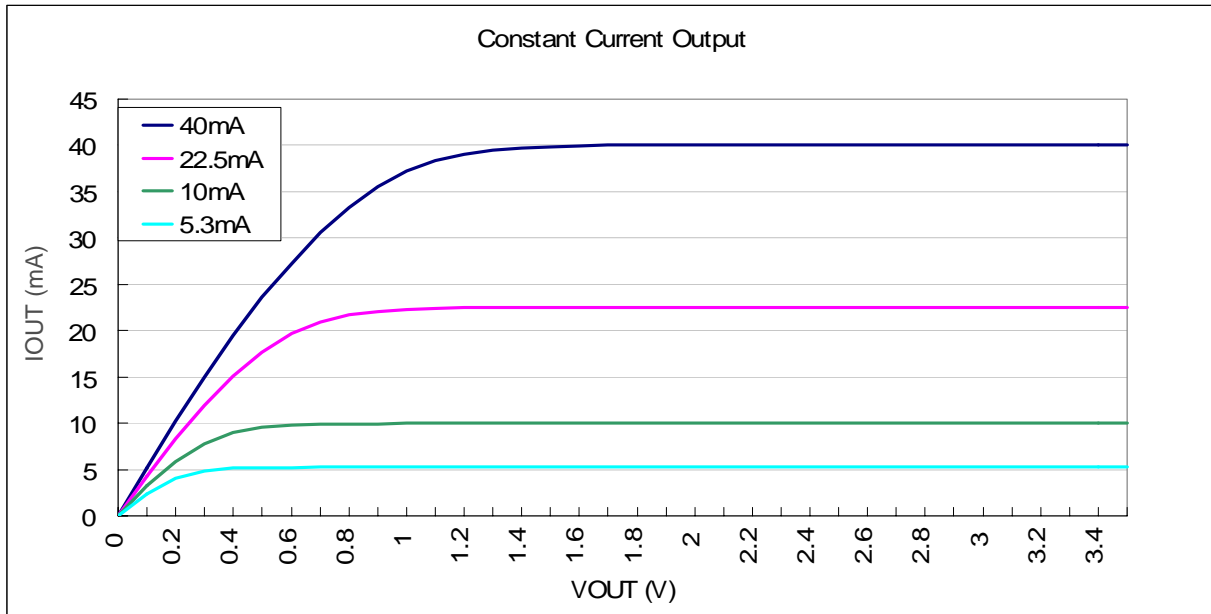
CONSTANT CURRENT CONTROL

The LD1071 provides a excellent Iout linearity by setting the Configuration Register for global brightness control. The following graph shows the linearity example under the condition at VDD=5V, REXT=400 ohms and Vout = 2.0V.

Ver1.0
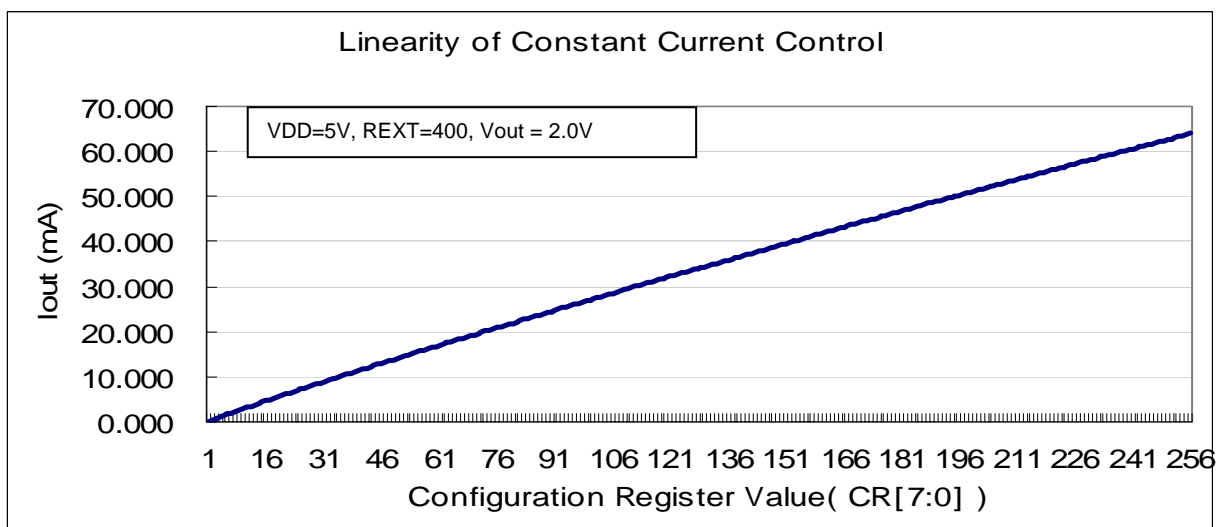
LED SUPPLY VOLTAGE(VLED)
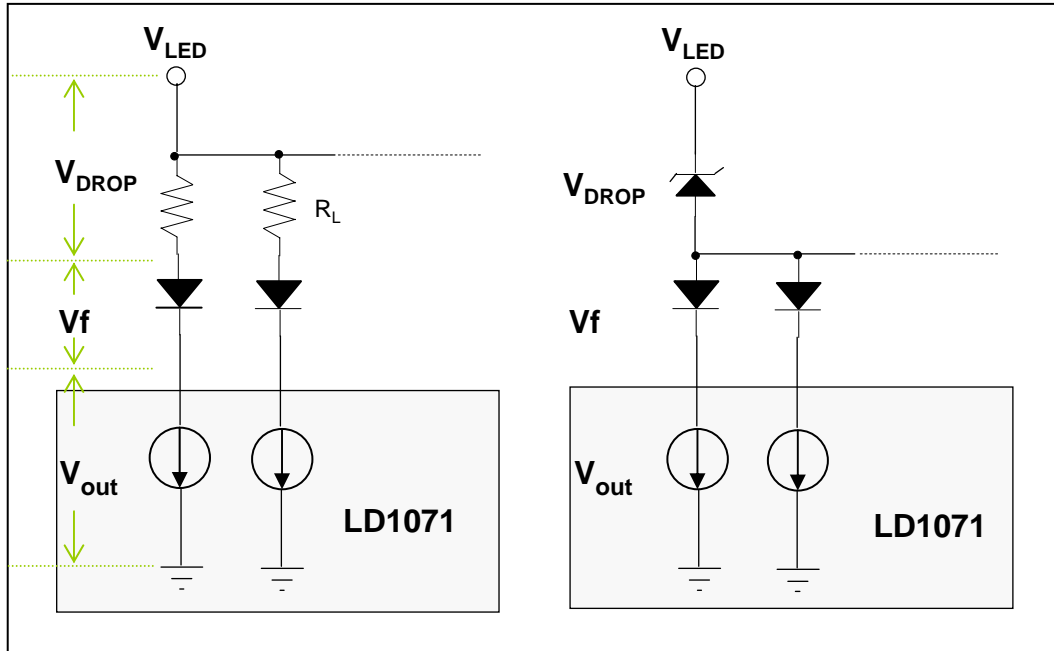
It is very important to select the proper value of Load Resistor(RL). Because the optimal VOUT value guarantees the constant output current and long life time of LED driver IC without over power consumption.

For example, let's calculate the Load Resistor value at VLED=5V, Iout=20mA, LED Forward Voltage(Vf)=3V.

1)   The full current of LD1018 = 20mA x 16 (channels) = 320mA
2)   The power consumption is 320mA x VOUT voltage.
    - when VOUT = 1V, the power consumption is 320mW.
    - when VOUT= 2V, the power consumption is 640mW.

Therefore, the Load Resistor (RL) = (VLED – VOUT– Vf) / Iout
$$= (5V – VOUT – 3V) / 20mA$$
$$= \underline{40}\ \ (When\ VOUT = 1.2V)$$

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PACKAGE POWER DISSIPATION(PD)

The LD1071 provides many package options such as 24-SOP package and 24-SSOP package. The maximum allowable package power dissipation is determined as PD(max) = (Tj – Ta) / R_Theta_JA. When 16 output ports are turned on simultaneously, the actual power package dissipation is PD(act) = (IDD x VDD) + (IOUT x Duty x VOUT x 16). Therefore, to keep that PD(act) is less equal than PD(max). The maximum allowable output current as a function of duty cycle is:

$$IOUT = \{[(Tj - Ta) / R\_Theta\_JA] - (IDD \times VDD)\} / VOUT / Duty / 16 \quad \text{where } Tj = 150C$$

Iout vs Duty (24-SOP)

(R_Theta_JA = 75C/W)

Iout vs Duty (24-SSOP)

(R_Theta_JA = 85C/W)

Package Power Dissipation
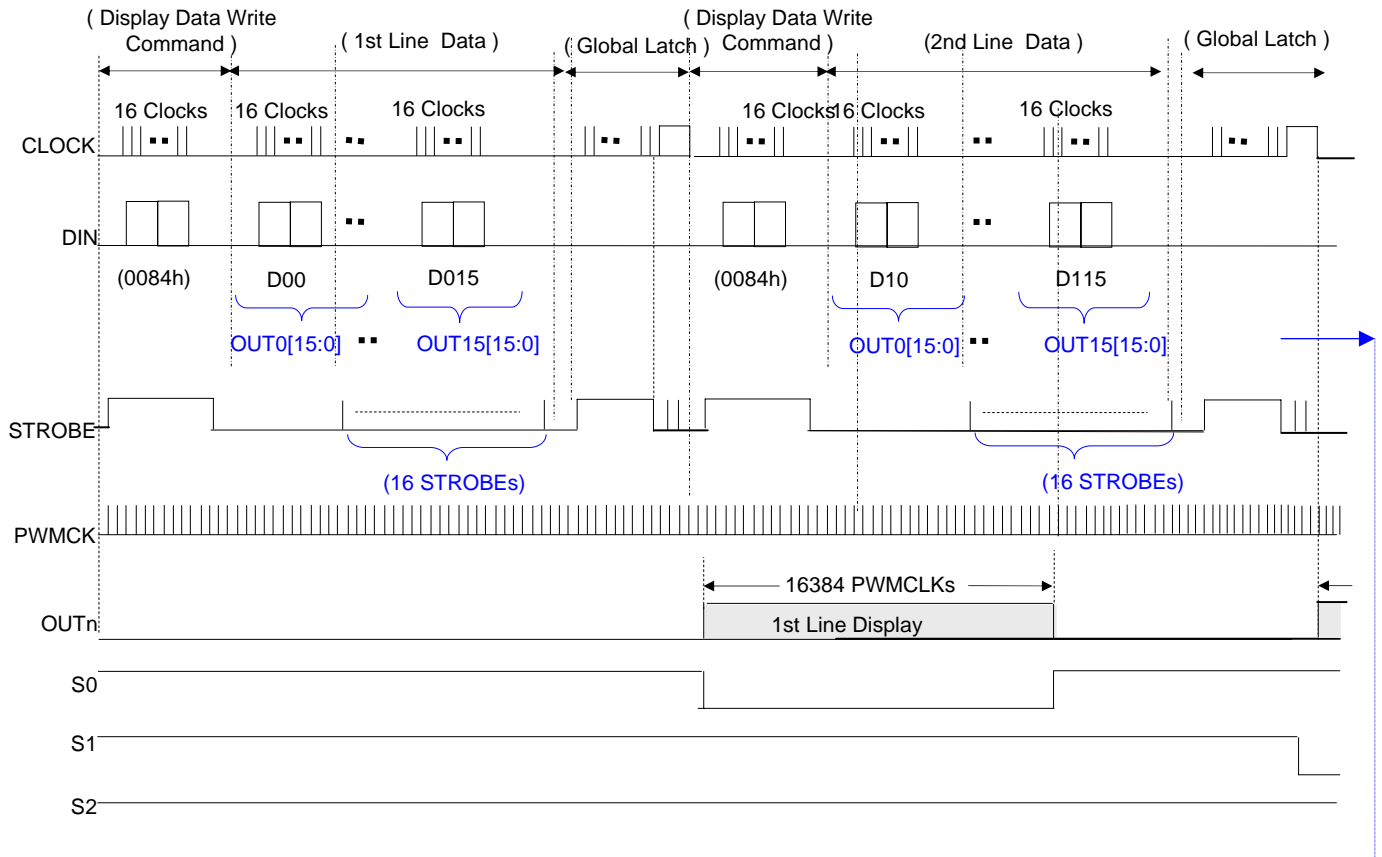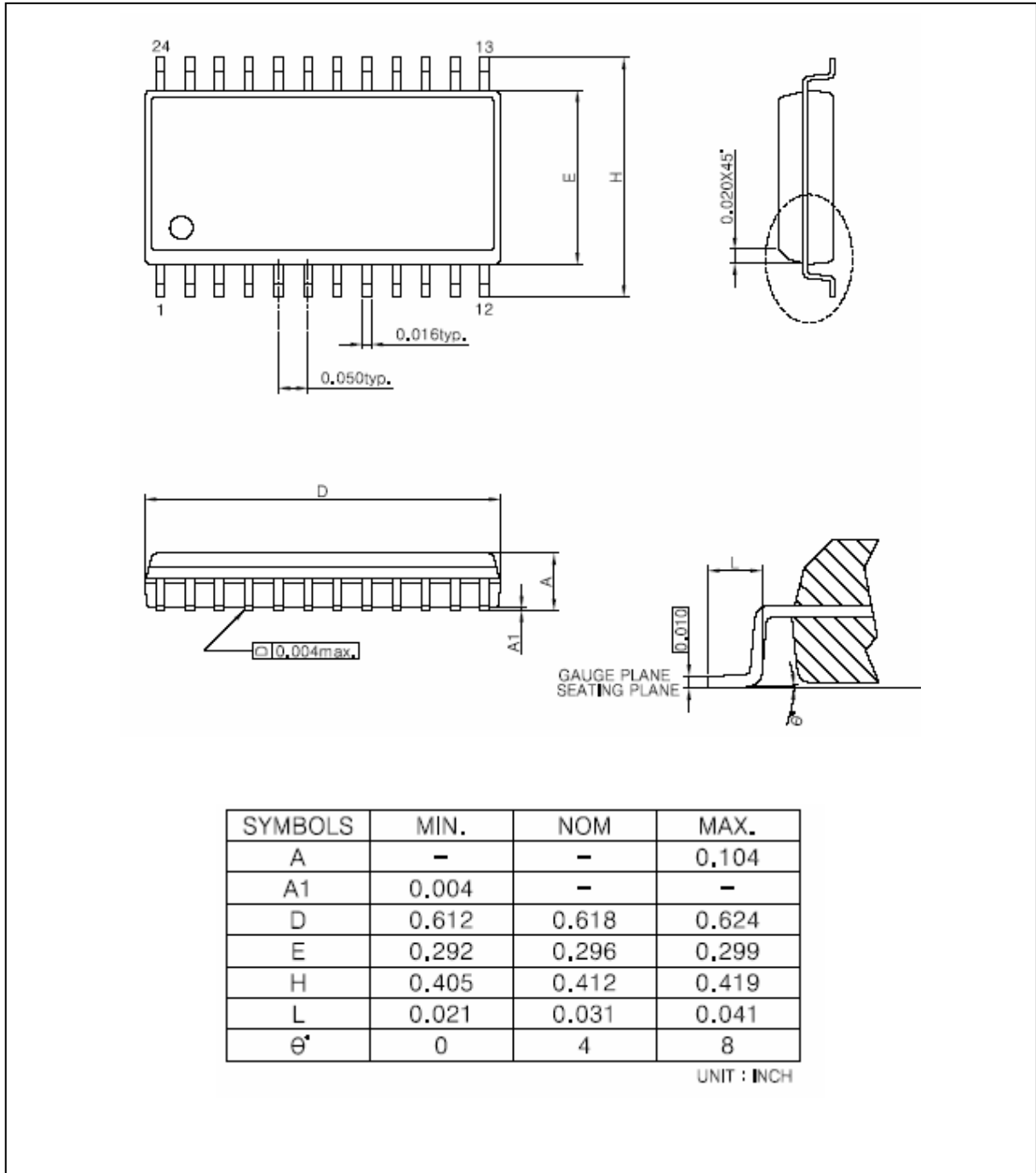
Ver1.0
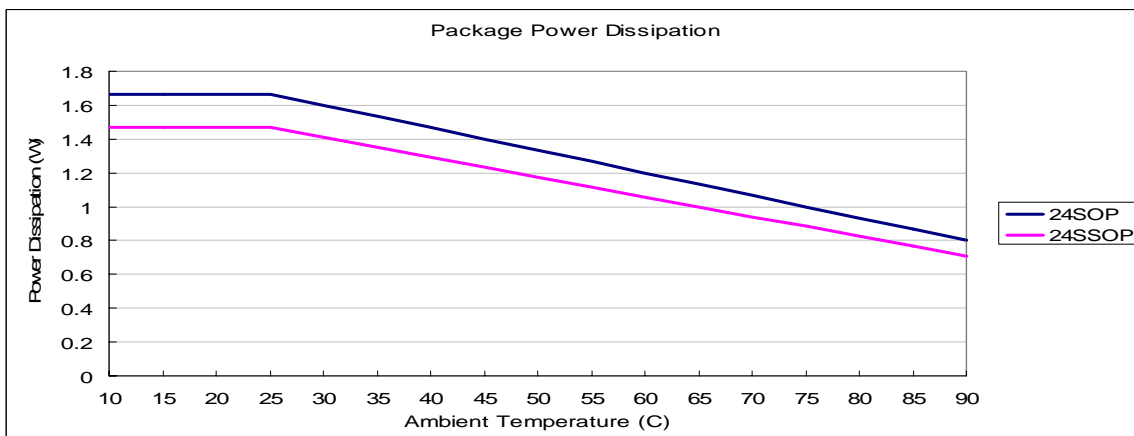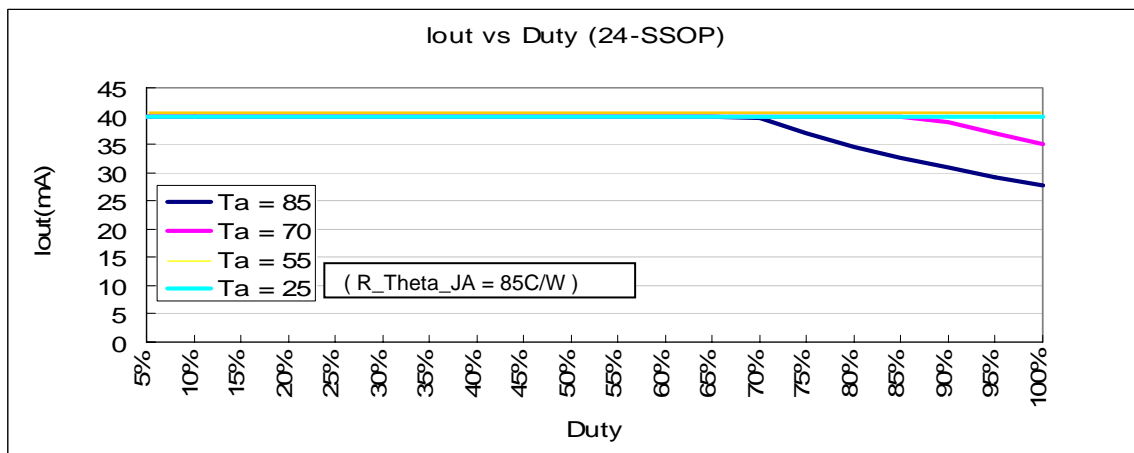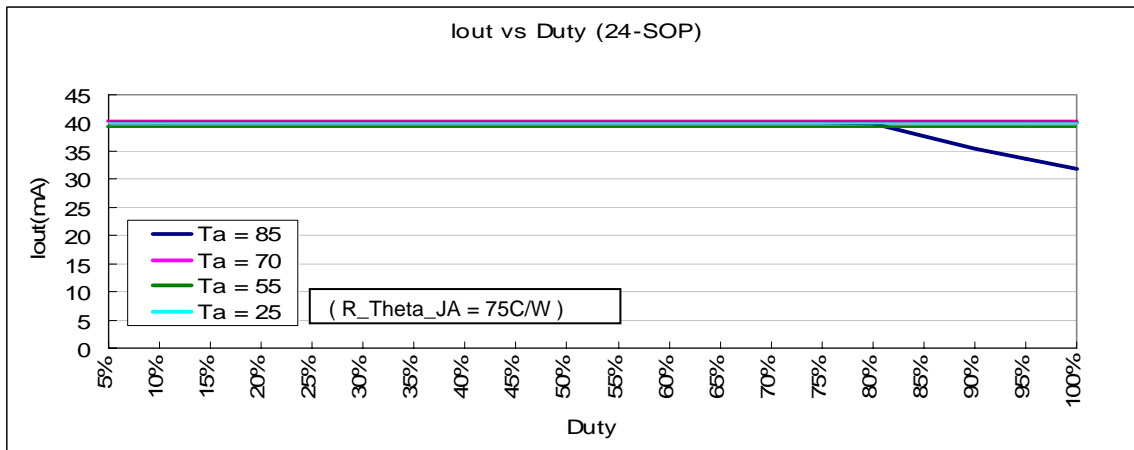
APPLICATION CIRCUIT 1 (16x2 Static Type)
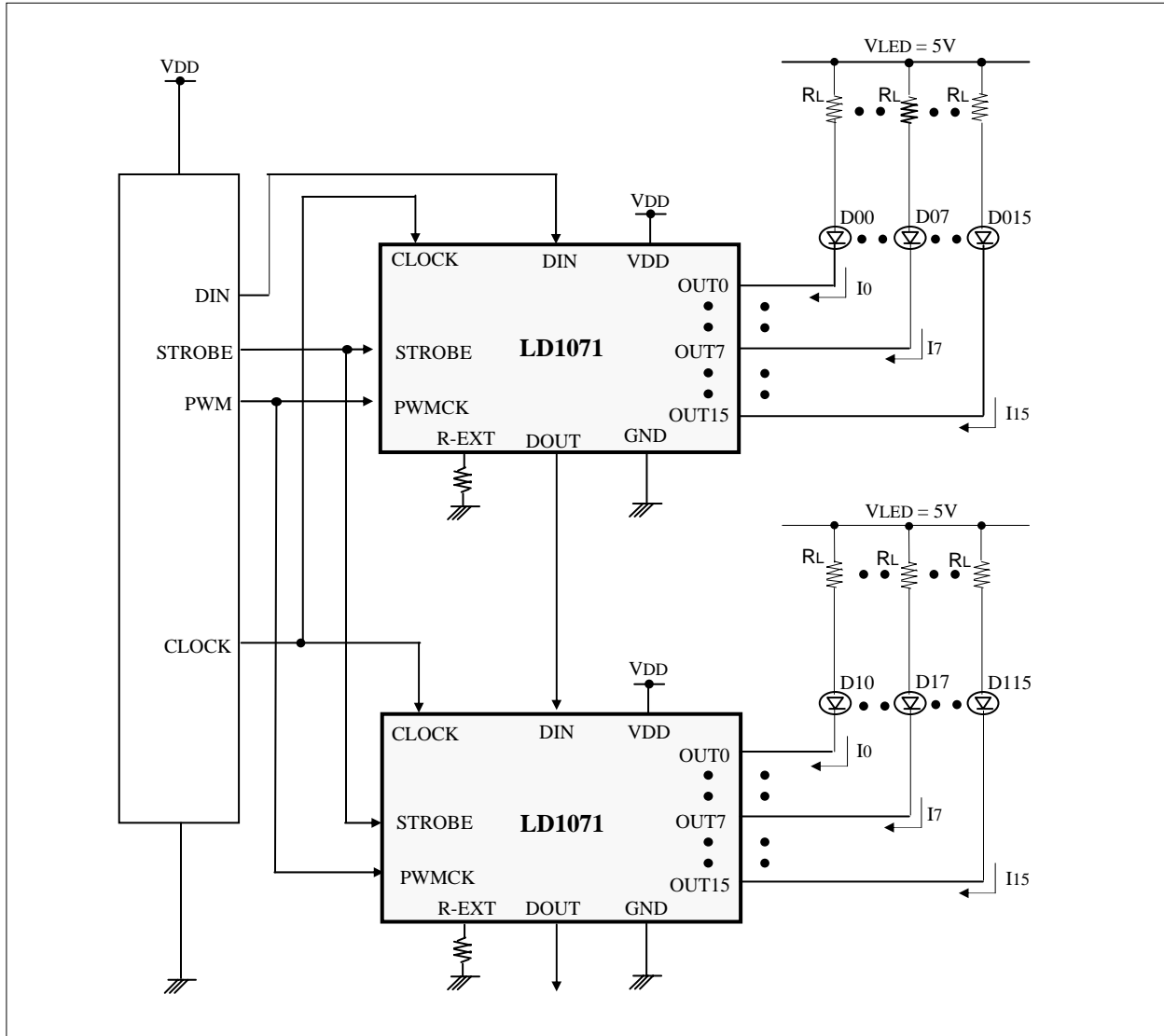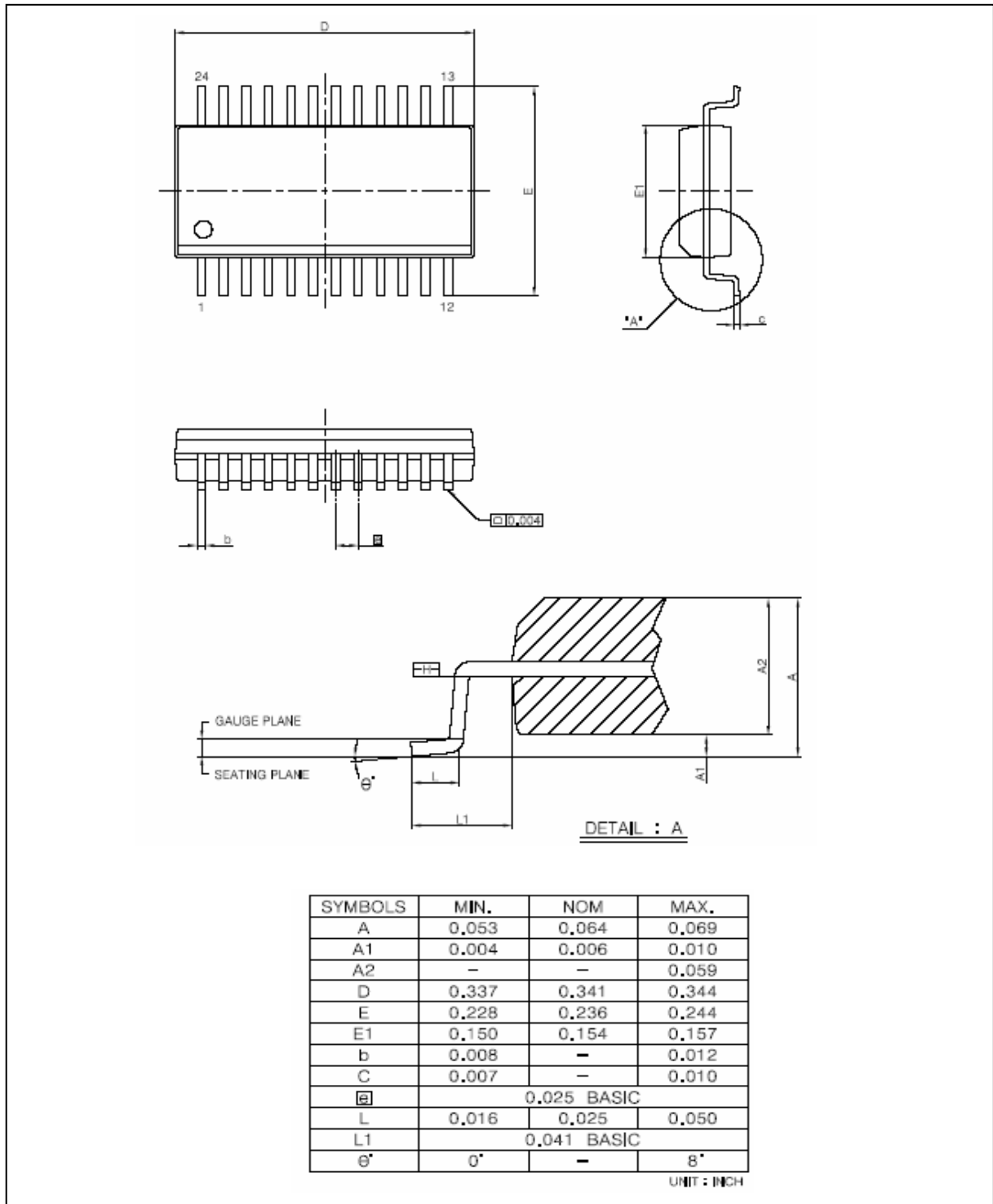

Data & Control Signal Connection for 16x2 Static Type Application

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TIMING DIAGRAM FOR APPLICATION CIRCUIT 1 (Default One Shot Mode)

Ver1.0

APPLICATION CIRCUIT 2 (16x16 Dynamic Type)

Data & Control Signal Connection for 16x16 Dynamic Type Application

Ver1.0
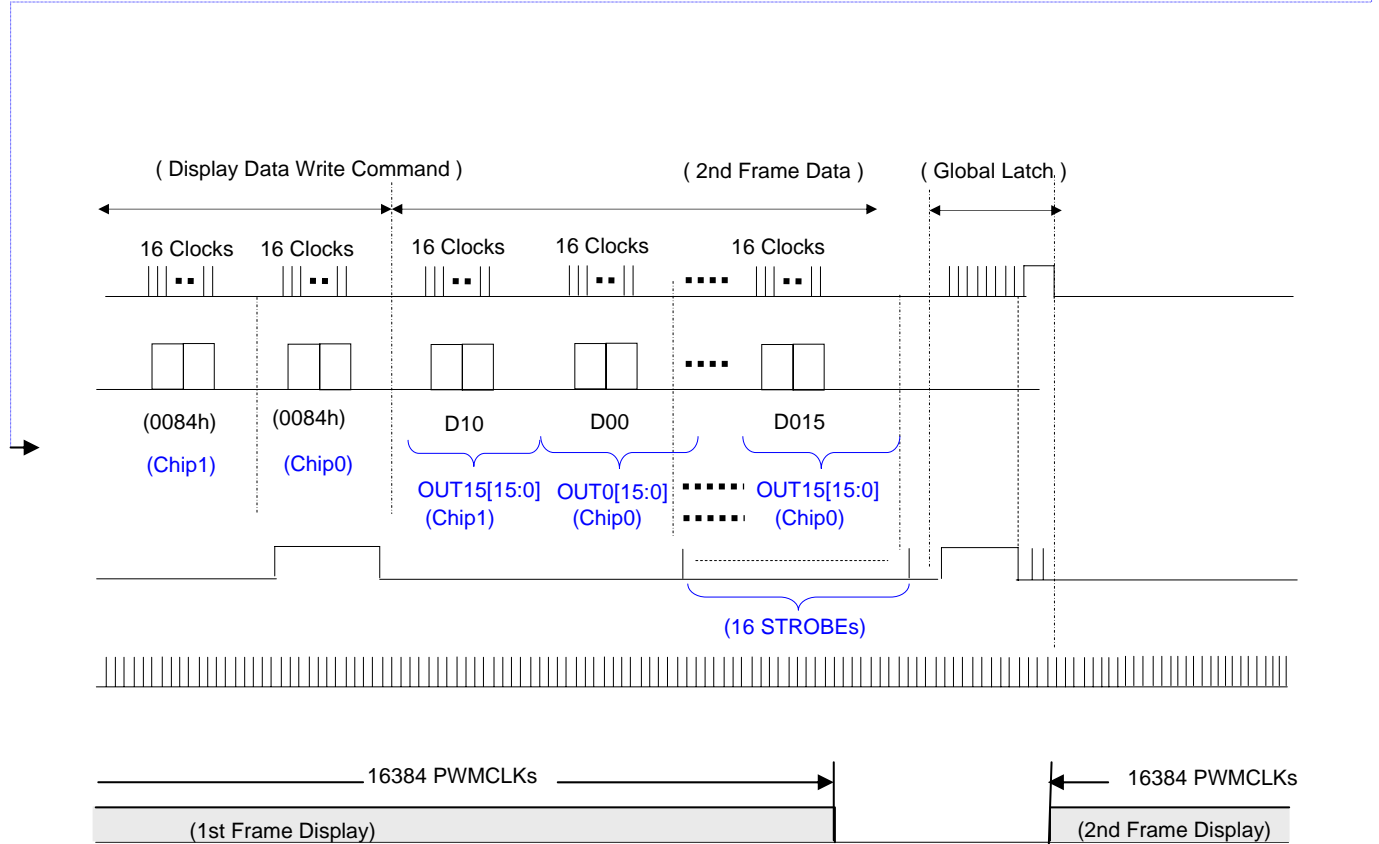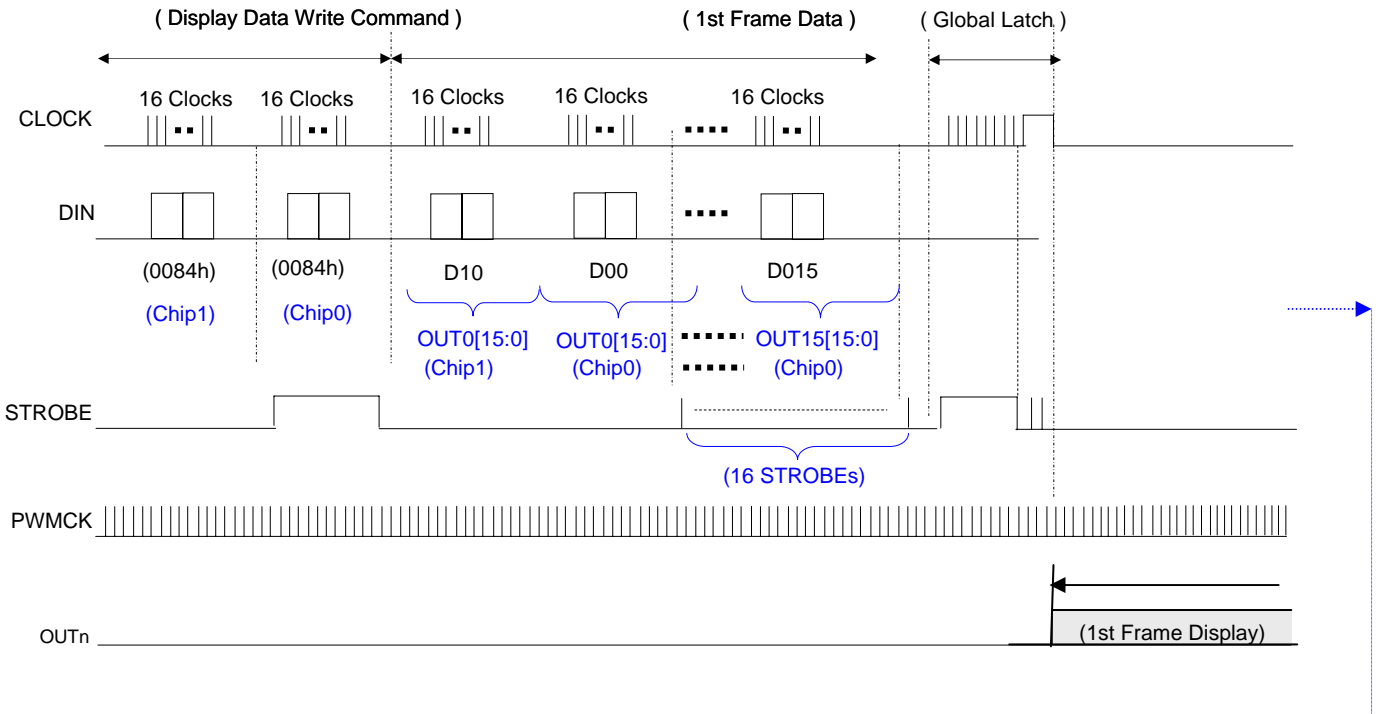
TIMING DIAGRAM FOR APPLICATION CIRCUIT 2 (Default One Shot Mode)

Ver1.0
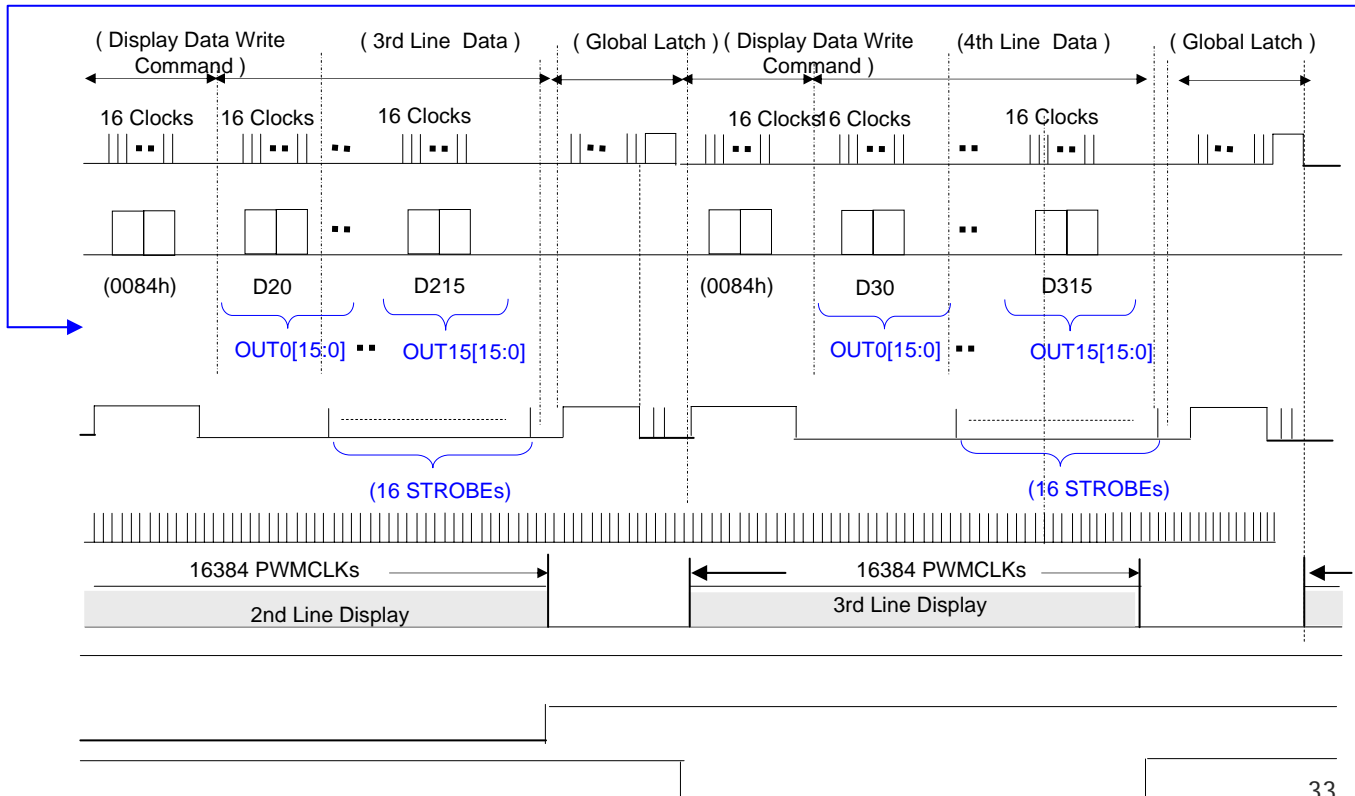
PACKAGE INFORMATION

LD1071-SP (SOP 24)

SYMBOLS	MIN.	NOM	MAX.
A	–	–	0.104
A1	0.004	–	–
D	0.612	0.618	0.624
E	0.292	0.296	0.299
H	0.405	0.412	0.419
L	0.021	0.031	0.041
θ˙	0	4	8

UNIT : INCH

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LD1071-SS (SSOP 24 – 150)

SYMBOLS	MIN.	NOM	MAX.
A	0.053	0.064	0.069
A1	0.004	0.006	0.010
A2	–	–	0.059
D	0.337	0.341	0.344
E	0.228	0.236	0.244
E1	0.150	0.154	0.157
b	0.008	–	0.012
C	0.007	–	0.010
e	0.025 BASIC		
L	0.016	0.025	0.050
L1	0.041 BASIC		
θ°	0°	–	8°

UNIT : INCH

Ver1.0