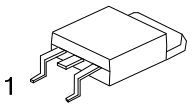
12A, 300V N-CHANNEL POWER MOSFET



TO-252

■ DESCRIPTION

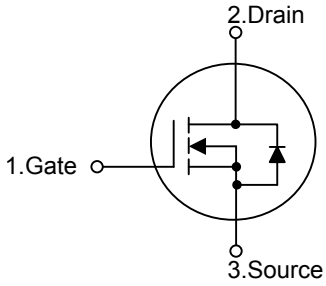
The UTC **12N30** is an N-channel mode power MOSFET using UTC' s advanced technology to provide customers with planar stripe and DMOS technology. This technology specializes in allowing a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **12N30** is universally applied in electronic lamp ballast based on half bridge topology and high efficient switched mode power supply.

■ FEATURES

* $R_{DS(ON)}$=0.34Ω @ V_{GS}=10V
* High switching speed

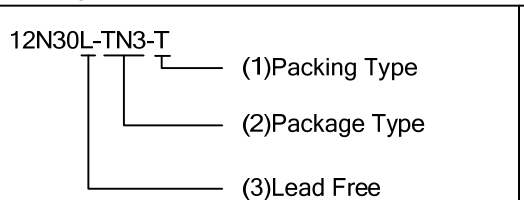
■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
12N30L-TN3-R	12N30G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source



(1) T: Tube

(2) TN3: TO-252

(3) G: Halogen Free, L: Lead Free

■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	300	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	Continuous (T_C=25°C)	I_D	12	A
	Pulsed (Note 2)	I_{DM}	48	A
Single Pulsed Avalanche Energy		E_{AS}	474	mJ
Power Dissipation		P_D	83	W
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55~+150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. Starting T_J=25°C, I_{AS}=12A, V_{DD}=50V, L=6.58mH.

■ THERMAL DATA

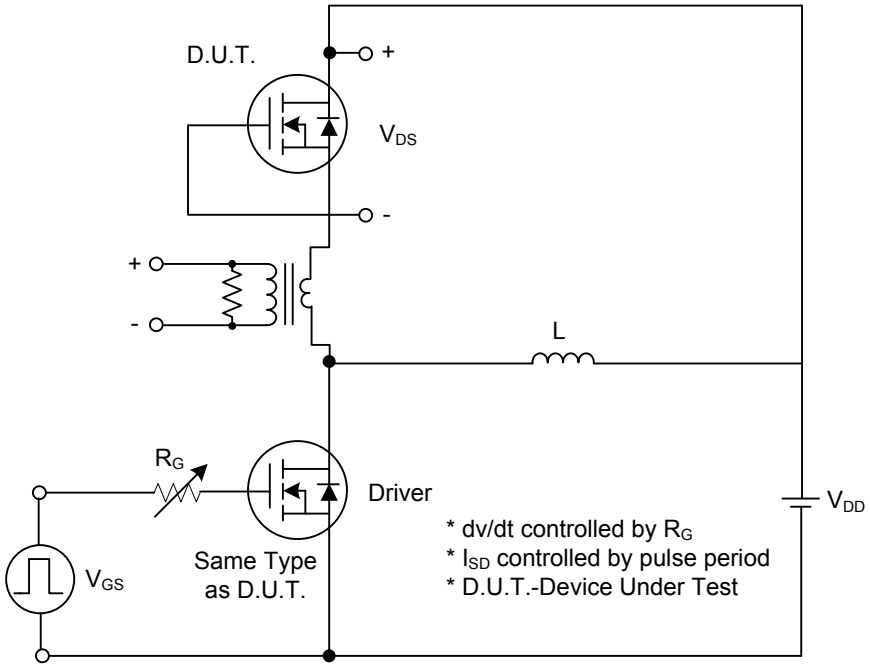
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	°C/W
Junction to Case	θ_{JC}	1.5	°C/W

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise noted)

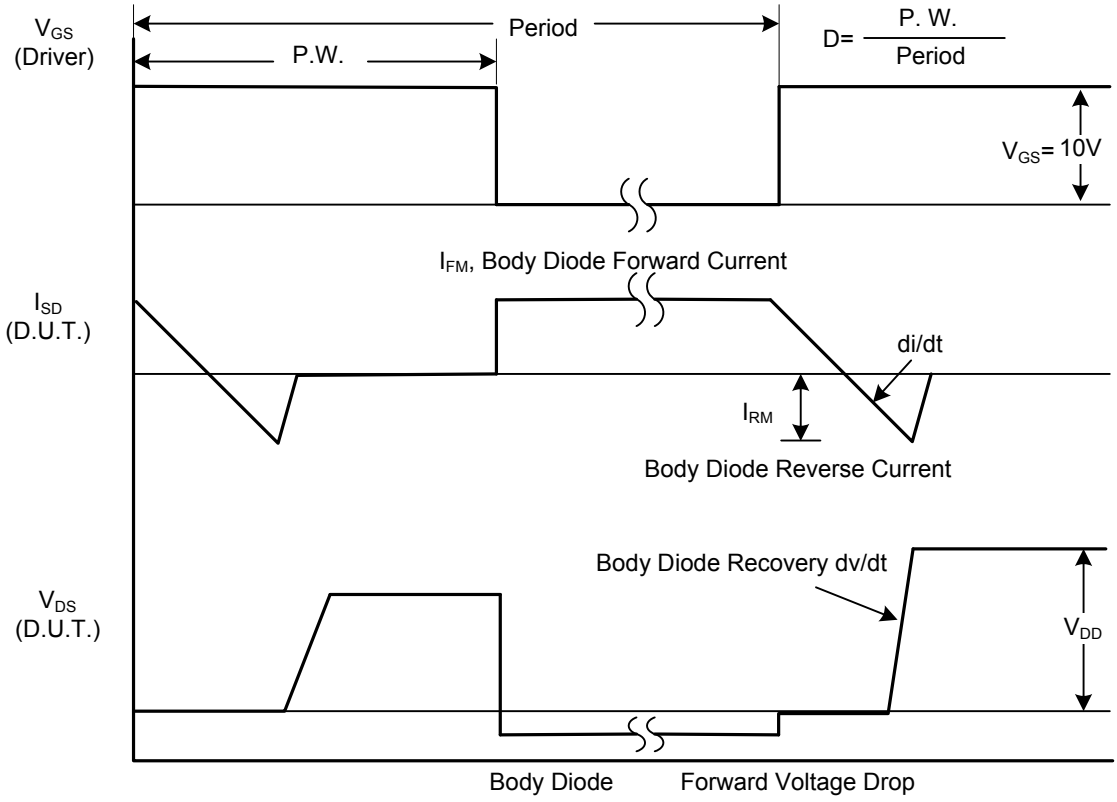
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	300			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=300V, V_{GS}=0V			1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=+20V, V_{DS}=0V			+100	nA
	Reverse		V_{GS}=-20V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=12A		0.34	0.47	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1.0MHz			3000	pF
Output Capacitance		C_{OSS}				900	pF
Reverse Transfer Capacitance		C_{RSS}				400	pF
SWITCHING PARAMETERS							
Total Gate Charge		Q_G	V_{DD}=150V, V_{GS}=10V, I_D=12A (Note 1, 2)		24		nC
Gate-Source Charge		Q_{GS}			5		nC
Gate-Drain Charge		Q_{GD}			5.6		nC
Turn-ON Delay Time		$t_{D(ON)}$	V_{DD}=30V, I_D=12A, R_G=25Ω (Note 1, 2)		30	50	ns
Rise Time		t_R			105	150	ns
Turn-OFF Delay Time		$t_{D(OFF)}$			480	750	ns
Fall-Time		t_F			140	200	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Drain-Source Diode Forward Voltage		V_{SD}	I_S=12A, V_{GS}=0V			1.4	V
Maximum Body-Diode Continuous Current		I_S				12	A
Maximum Body-Diode Pulsed Current		I_{SM}				48	A

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

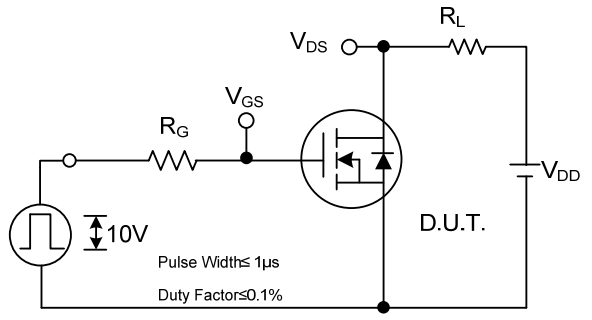


Peak Diode Recovery dv/dt Test Circuit

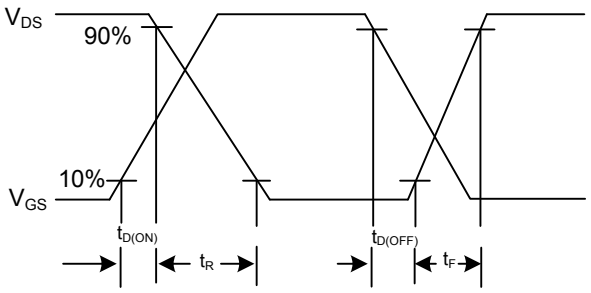


Peak Diode Recovery dv/dt Waveforms

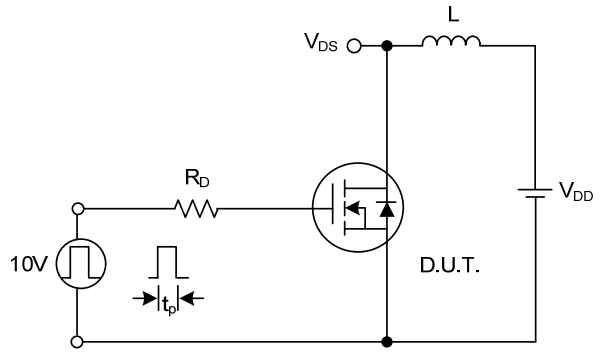
■ TEST CIRCUITS AND WAVEFORMS



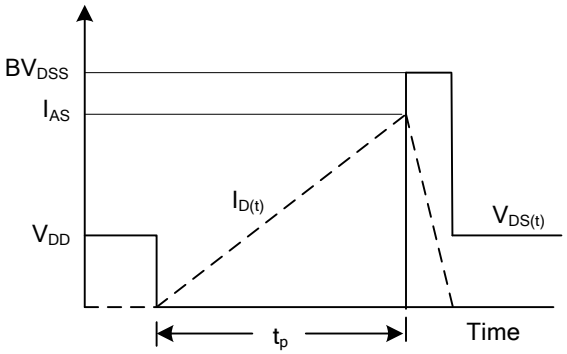
Switching Test Circuit



Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms