SGS-THOMSON MICROELECTRONICS

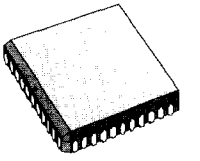
ST9020
ST9027, ST9028

12/16K ROM HCMOS MCUs

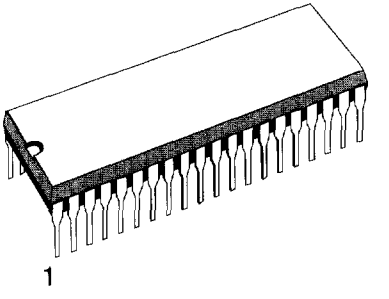
- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time : 500ns (12MHz internal)
- Internal Memory :

	ROM	RAM
ST9020	12K	
ST9027	16K	256
ST9028	16K	256

  224 general purpose registers available as RAM, accumulators or index registers (register file)
- 40-pin Plastic Dual in line Package for ST9020, ST9027
- 44-lead Plastic Leaded Chip Carrier package for ST9028
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- Up to 36 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with an 8-bit Prescaler, able to be used as a Watchdog Timer
- 16 bit Multifunction Timer, with an 8-bit Prescaler and 12 operating modes
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Windowed and One Time Programmable EPROM parts available for prototyping and pre-production development phases



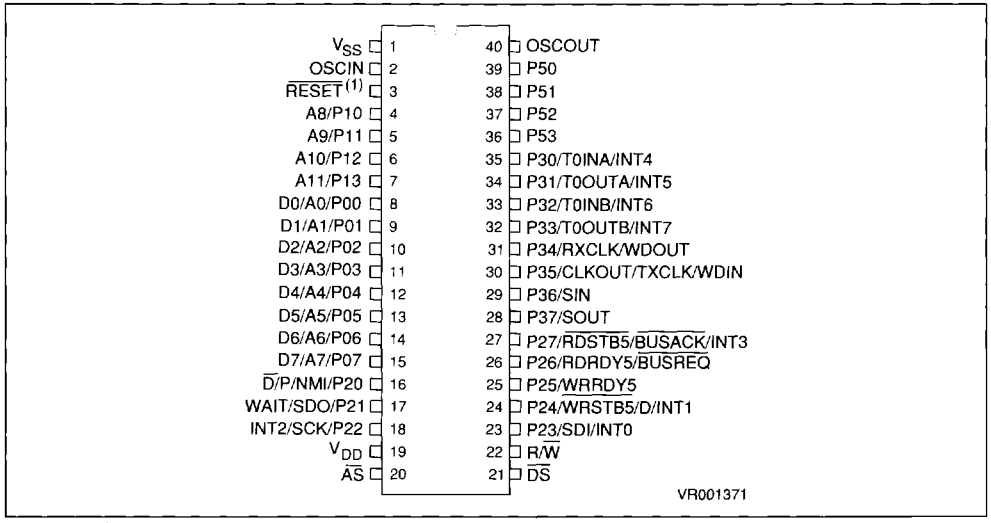
PLCC44



PDIP40

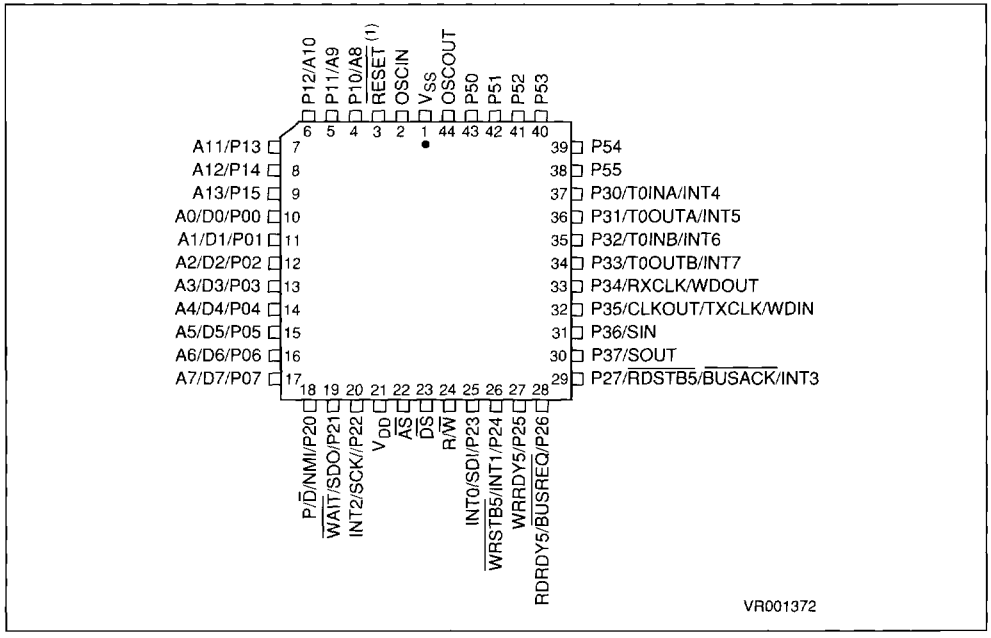
(Ordering Information at the end of the Datasheet)

Figure 1-1. 40 Pin DIP Package



Note 1. This pin is also the V PP input for the EPROM based devices

Figure 1-2. 44 Pin PLCC Package



Note 1. This pin is also the V PP input for the EPROM based devices

1.1 GENERAL DESCRIPTION

The ST9020, ST9027 and ST9028 (following mentioned as ST902X) are ROM members of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM parts are fully compatible with their EPROM versions, which may be used for the prototyping and pre-production phases of development, and can be configured as : stand-alone microcontrollers with 16K bytes of on-chip ROM, (12K for ST9020), microcontrollers able to manage up to 16K bytes of external data memory, or as parallel processing elements in a system with other processors and peripheral controllers.

A key point of the ST902X architecture is its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST902X is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I²C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST902X with up to 36 I/O lines dedicated to digital Input/Output. These lines are grouped into up to three 8 bit I/O Ports plus two 6-bit I/O ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal), Data Memory (internal/external) and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16 bit MultiFunction Timer, with an 8 bit Prescaler and 12 operating modes allows simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

Figure 1-3. ST902X Block Diagram