



N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)			
100	0.025 at V _{GS} = 10 V	9.3			
	0.028 at V _{GS} = 6.0 V	8.8			

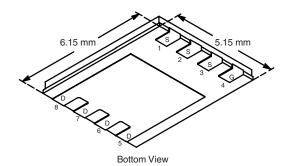
FEATURES

- Halogen-free According to IEC 61249-2-21 **Available**
- TrenchFET® Power MOSFETs
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- PWM Optimized for Fast Switching
- 100 % R_g Tested





PowerPAK SO-8

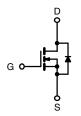


Ordering Information: Si7456DP-T1-E3 (Lead (Pb)-free)

Si7456DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- Primary Side Switch for High Density DC/DC
- Telecom/Server 48 V, Full-/Half-Bridge DC/DC
- Industrial and 42 V Automotive



N-Channel MOSEET

ABSOLUTE MAXIMUM RATINGS T	$_{\lambda}$ = 25 °C, unle	ss otherwise r	noted		
Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V _{DS}	100		V
Gate-Source Voltage		V_{GS}	± 20		V
Continuous Drain Current (T,I = 150°C) ^a	T _A = 25 °C	- I _D	9.3	5.7	А
Continuous Diain Current (1 j = 150 C)	T _A = 85 °C		6.7	4.1	
Pulsed Drain Current		I _{DM}	40		1
Avalanche Current	L = 0.1 mH	I _{AS}	30		
Single Avalanche Energy (Duty Cycle ≤ 1 %)	(Duty Cycle ≤ 1 %)		45		mJ
Continuous Source Current (Diode Conduction) ^a		I _S	4.3	1.6	Α
	T _A = 25 °C	P _D	5.2	1.9	W
Maximum Power Dissipation ^a	T _A = 85 °C		2.7	1.0	VV
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b,c}			2	160	O

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Manianum lungtion to Austranti	t ≤ 10 s	R _{thJA}	19	24	°C/W	
Maximum Junction-to-Ambient ^a	Steady State	' 'thJA	52	65		
Maximum Junction-to-Case	Steady State	R_{thJC}	1.5	1.8		

- a. Surface Mounted on 1" x 1" FR4 board.
- b. See Solder Profile (<u>www.vishay.com/ppg?73257</u>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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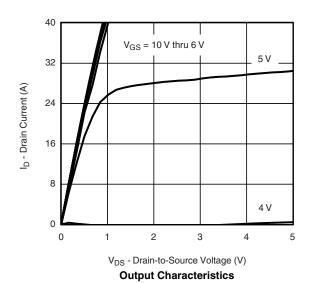
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static			1			
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2		4	V
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zava Cata Valtaga Dvain Current	1	V _{DS} = 100 V, V _{GS} = 0 V	V _{DS} = 100 V, V _{GS} = 0 V		1	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$			20	μΑ
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	40			Α
	В	$V_{GS} = 10 \text{ V}, I_D = 9.3 \text{ A}$		0.021	0.025	0
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 6.0 V, I _D = 8.8 A 0.023			0.028	Ω
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 15 \text{ V}, I_D = 9.3 \text{ A}$		35		S
Diode Forward Voltage ^a	V_{SD}	I _S = 4.3 A, V _{GS} = 0 V		0.8	1.2	V
Dynamic ^b			•			
Total Gate Charge	Qg			36	44	
Gate-Source Charge	Q_{gs}	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 9.3 \text{ A}$		10		nC
Gate-Drain Charge	Q_{gd}			8.6		
Gate Resistance	R_{g}		0.5	1.27	2.1	Ω
Turn-On Delay Time	t _{d(on)}			20	40	
Rise Time	t _r	V_{DD} = 50 V, R_L = 50 Ω		10	20	
Turn-Off Delay Time	t _{d(off)}	$\text{I}_\text{D}\cong\text{1.0 A},\text{V}_\text{GEN}=\text{10 V},\text{R}_\text{g}=\text{6}~\Omega$		46	90	ns
Fall Time	t _f			26	50]
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 4.3 A, dI/dt = 100 A/μs		50	80	

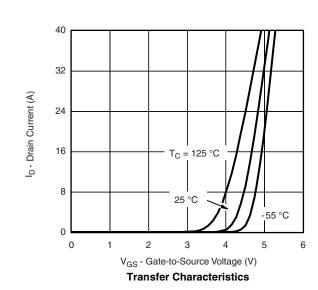
Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

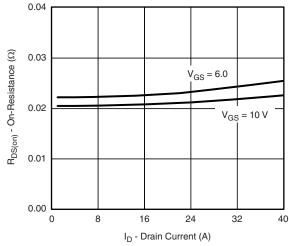
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



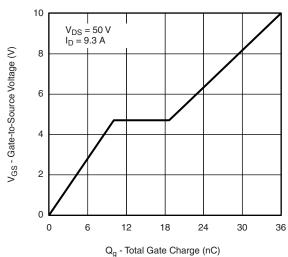




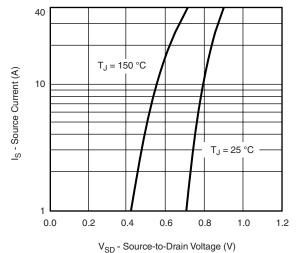
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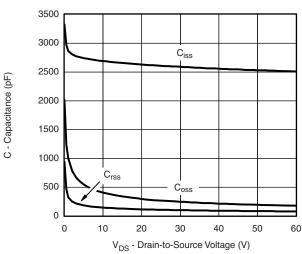
On-Resistance vs. Drain Current



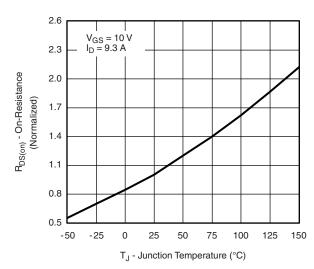
Gate Charge



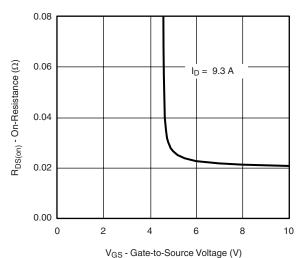
Source-Drain Diode Forward Voltage



Capacitance



On-Resistance vs. Junction Temperature



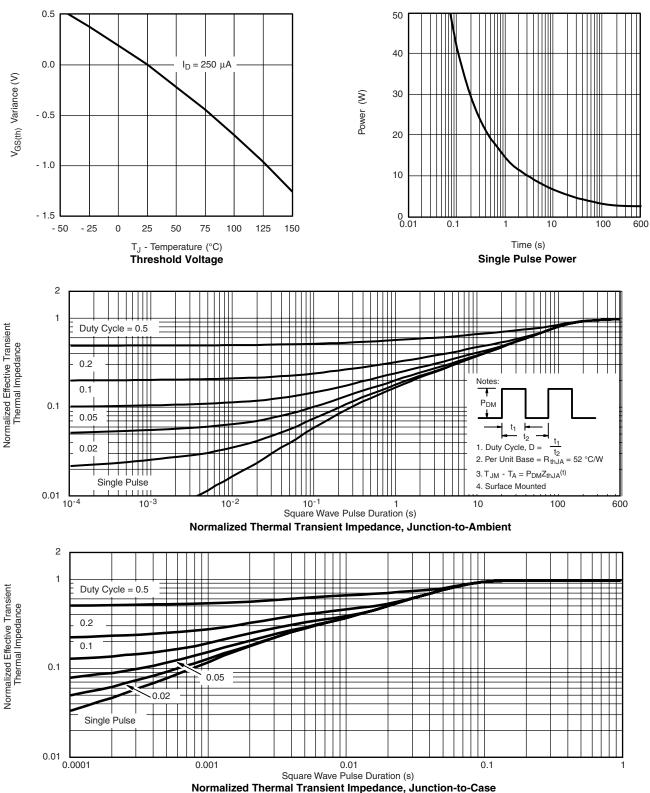
VGS - Gate-to-Source Voltage (V)

On-Resistance vs. Gate-to-Source Voltage

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

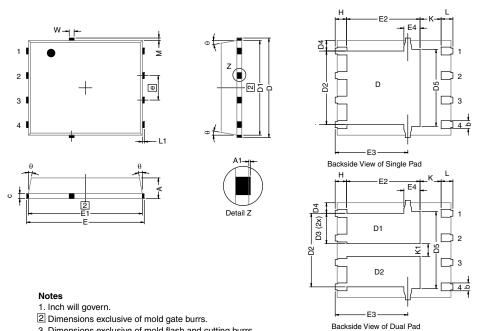


Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71603.



DWG: 5881

PowerPAK® SO-8, (Single/Dual)



3. Dimensions exclusive of mold flash and cutting burrs.							
DIM.		MILLIMETERS		INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.97	1.04	1.12	0.038	0.041	0.044	
A1		-	0.05	0	-	0.002	
b	0.33	0.41	0.51	0.013	0.016	0.020	
С	0.23	0.28	0.33	0.009	0.011	0.013	
D	5.05	5.15	5.26	0.199	0.203	0.207	
	4.00	4.00	F 00	0.400	0.400	0.407	

Α	0.97	1.04	1.12	0.038	0.041	0.044	
A1		-	0.05	0	-	0.002	
b	0.33	0.41	0.51	0.013	0.016	0.020	
С	0.23	0.28	0.33	0.009	0.011	0.013	
D	5.05	5.15	5.26	0.199	0.203	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.56	3.76	3.91	0.140	0.148	0.154	
D3	1.32	1.50	1.68	0.052	0.059	0.066	
D4		0.57 typ.			0.0225 typ.		
D5		3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246	
E1	5.79	5.89	5.99	0.228	0.232	0.236	
E2 (for AL product)	3.30	3.48	3.66	0.130	0.137	0.144	
E2 (for other product)	3.48	3.66	3.84	0.137	0.144	0.151	
E3	3.68	3.78	3.91	0.145	0.149	0.154	
E4 (for AL product)		0.58 typ.			0.023 typ.		
E4 (for other product)		0.75 typ.		0.030 typ.			
е		1.27 BSC		0.050 BSC			
K (for AL product)		1.45 typ.		0.057 typ.			
K (for other product)		1.27 typ.		0.050 typ.			
K1	0.56	-	=	0.022	-	=	
Н	0.51	0.61	0.71	0.020	0.024	0.028	
L	0.51	0.61	0.71	0.020	0.024	0.028	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
θ	0°	-	12°	0°	-	12°	
W	0.15	0.25	0.36	0.006	0.010	0.014	
M	0.125 typ.			0.005 typ.			
ECN: C13-0702-Rev. K, 20)-May-13			•			

Revison: 20-May-13 Document Number: 71655



RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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