High Voltage Synchronous Rectified Dual-Channel Buck MOSFET Driver for Notebook Computer

General Description

The RT9627A is a high frequency, dual-channel driver specifically designed to drive two power N-MOSFETs in each channel of a synchronous-rectified Buck converter topology. It is especially suited for mobile computing applications that require high efficiency and excellent thermal performance. This driver, combined with Richtek's series of multi-phase Buck PWM controllers, provides a complete core voltage regulator solution for advanced microprocessors.

The drivers are capable of driving a 3nF load with fast rising/falling time and fast propagation delay. This device implements bootstrapping on the upper gates with only a single external capacitor. This reduces implementation complexity and allows the use of higher performance, cost effective, N-MOSFETs. Adaptive shoot through protection is integrated to prevent both MOSFETs from conducting simultaneously.

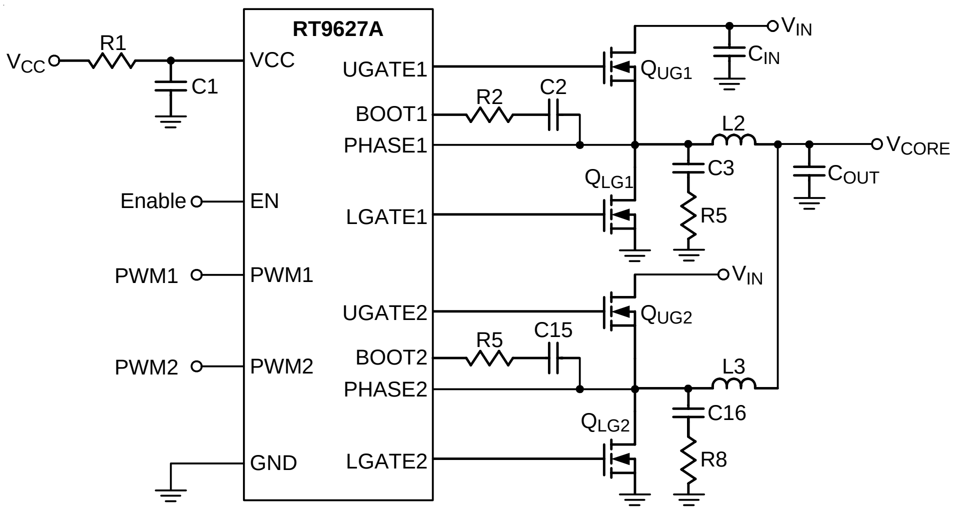
Features

- **Dual-Channel Driver**
- **Each Channel Drives Two N-MOSFETs**
- **Adaptive Shoot-Through Protection**
- **0.5Ω On-Resistance, 4A Sink Current Capability**
- **Supports High Switching Frequency**
- **Tri-State PWM Input for Power Stage Shutdown**
- **Output Disable Function**
- **Integrated Boost Switch**
- **Low Bias Supply Current**
- **VCC POR Feature Integrated**
- **RoHS Compliant and Halogen Free**

Applications

- Core Voltage Supplies for Intel® / AMD® Mobile Microprocessors
- High Frequency Low Profile DC/DC Converters
- High Current Low Output Voltage DC/DC Converters
- High Input Voltage DC/DC Converters

Simplified Application Circuit



Ordering Information

RT9627A □□

- Package Type
  QW : WDFN-12L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

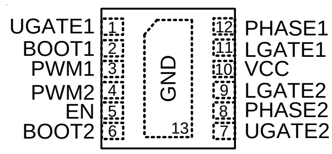
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

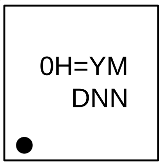
Pin Configurations

(TOP VIEW)



WDFN-12L 3x3

Marking Information



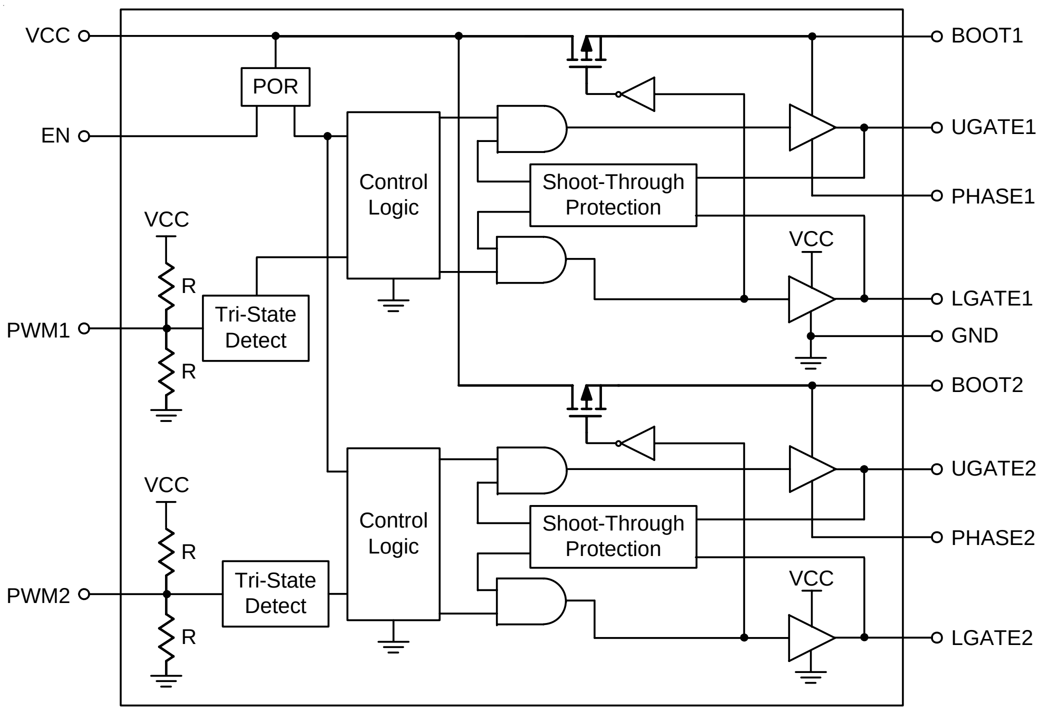
0H= : Product Code

YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 7	UGATE1, UGATE2	High Side Gate Drive Outputs. Connect to the Gates of high side power N-MOSFETs.
2, 6	BOOT1, BOOT2	Bootstrap Supply for High Side Gate Drives. Connect the bootstrap capacitors between these pins and the PHASEx pins. The bootstrap capacitors provide the charge to turn on the high side MOSFETs.
3, 4	PWM1, PWM2	Control Inputs for Drivers. The PWM signal can enter three distinct states during operation. Connect these pins to the PWM outputs of the controller.
5	EN	Enable Control Input. When pulling low, both UGATEx and LGATEx are driven low and the normal operation is disabled.
8, 12	PHASE2, PHASE1	Switch Nodes. Connect these pins to the Sources of the high side MOSFETs and the Drains of the low side MOSFETs. These pins provide return paths for the high side gate drivers.
9, 11	LGATE2, LGATE1	Low Side Gate Drive Outputs. Connect to the Gates of the low side power N-MOSFETs.
10	VCC	Supply Voltage Input. Connect this pin to a 5V bias supply. Place a high quality bypass capacitor from this pin to GND.
13 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Operation

POR (Power On Reset)

POR block detects the voltage at the VCC pin. When the VCC pin voltage is higher than POR rising threshold, the POR pin output voltage (POR output) is high. POR output is low when VCC is not higher than POR rising threshold. When the POR pin voltage is high, UGATEx and LGATEx can be controlled by PWMx input voltage. If the POR pin voltage is low, both UGATEx and LGATEx will be pulled to low.

Tri-State Detect

When both POR output and ENx pin voltages are high, UGATEx and LGATEx can be controlled by PWMx input. There are three PWMx input modes which are high, low, and shutdown state. If PWMx input is within the shutdown window, both UGATEx and LGATEx outputs are low. When PWMx input is higher than its rising threshold, UGATEx is high and LGATEx is low. When PWMx input is lower than its falling threshold, UGATEx is low and LGATEx is high.

Control Logic

Control logic block detects whether high side MOSFET is turned off by monitoring (UGATEx – PHASEx) voltages below 1.1V or phase voltage below 2V. To prevent the overlap of the gate drives during the UGATEx pull low and the LGATEx pull high, low side MOSFET can be turned on only after high side MOSFET is effectively turned off.

Shoot-Through Protection

Shoot-through protection block implements the dead-time when both high side and low side MOSFETs are turned off. With shoot-through protection block, high side and low side MOSFETs are never turned on simultaneously. Thus, shoot-through between high side and low side MOSFETs is prevented.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VCC ---------- –0.3V to 6V
- BOOTx to PHASEx ---------- –0.3V to 6V
- PHASEx to GND
  DC ---------- –0.3V to 32V
  < 20ns ---------- –8V to 38V
- UGATEx to PHASEx
  DC ---------- –0.3V to 6V
  < 20ns ---------- –5V to 7.5V
- LGATEx to GND
  DC ---------- –0.3V to 6V
  < 20ns ---------- –2.5V to 7.5V
- PWMx, EN to GND ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-12L 3x3 ---------- 3.28W
- Package Thermal Resistance (Note 2)
  WDFN-12L 3x3, θ_{JA} ---------- 30.5°C/W
  WDFN-12L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage, VIN ---------- 4.5V to 26V
- Supply Voltage, VCC ---------- 4.5V to 5.5V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC Supply Current						
Quiescent Current	I_Q	PWM Pin Floating, V_{EN} = 3.3V	--	120	--	μA
Shutdown Current	I_{SHDN}	V_{EN} = 0V, PWM = 0V	--	0	5	μA
VCC Power On Reset (POR)	V_{PORH}	VCC POR Rising	--	3.85	4.1	V
	V_{PORL}	VCC POR Falling	3.4	3.65	--	V
	V_{PORHYS}	Hysteresis	--	200	--	mV
Internal BOOT Switch						
Internal Boot Switch On Resistance	R_{BOOT}	VCC to BOOT, 10mA	--	--	80	Ω

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
PWMx Input							
Input Current		I_{PWM}	V_{PWM} = 5V	--	174	--	μA
			V_{PWM} = 0V	--	–174	--	
PWMx Tri-State Rising Threshold		V_{PWMH}		3.5	3.8	4.1	V
PWMx Tri-State Falling Threshold		V_{PWML}		0.7	1	1.3	V
Tri-State Shutdown Hold-off Time		t_{SHD_Tri}		100	175	250	ns
EN Input							
EN Input Voltage	Logic-High	V_{ENH}		2	--	--	V
	Logic-Low	V_{ENL}		--	--	0.5	
Switching Time							
UGATEx Rise Time		t_{UGATEr}	3nF load	--	8	--	ns
UGATEx Fall Time		t_{UGATEf}	3nF load	--	8	--	ns
LGATEx Rise Time		t_{LGATEr}	3nF load	--	8	--	ns
LGATEx Fall Time		t_{LGATEf}	3nF load	--	4	--	ns
UGATEx Turn-Off Propagation Delay		t_{PDLU}	Outputs Unloaded	--	35	--	ns
LGATEx Turn-Off Propagation Delay		t_{PDLL}	Outputs Unloaded	--	35	--	ns
UGATEx Turn-On Propagation Delay		t_{PDHU}	Outputs Unloaded	--	20	--	ns
LGATEx Turn-On Propagation Delay		t_{PDHL}	Outputs Unloaded	--	20	--	ns
UGATEx/LGATEx Tri-State Propagation Delay		t_{PTS}	Outputs Unloaded	--	35	--	ns
Output							
UGATEx Driver Source Resistance		$R_{UGATEsr}$	100mA Source Current	--	1	--	Ω
UGATEx Driver Source Current		$I_{UGATEsr}$	$V_{UGATE} - V_{PHASE}$ = 2.5V	--	2	--	A
UGATEx Driver Sink Resistance		$R_{UGATEsk}$	100mA Sink Current	--	1	--	Ω
UGATEx Driver Sink Current		$I_{UGATEsk}$	$V_{UGATE} - V_{PHASE}$ = 2.5V	--	2	--	A
LGATEx Driver Source Resistance		$R_{LGATEsr}$	100mA Source Current	--	1	--	Ω
LGATEx Driver Source Current		$I_{LGATEsr}$	V_{LGATE} = 2.5V	--	2	--	A
LGATEx Driver Sink Resistance		$R_{LGATEsk}$	100mA Sink Current	--	0.5	--	Ω
LGATEx Driver Sink Current		$I_{LGATEsk}$	V_{LGATE} = 2.5V	--	4	--	A

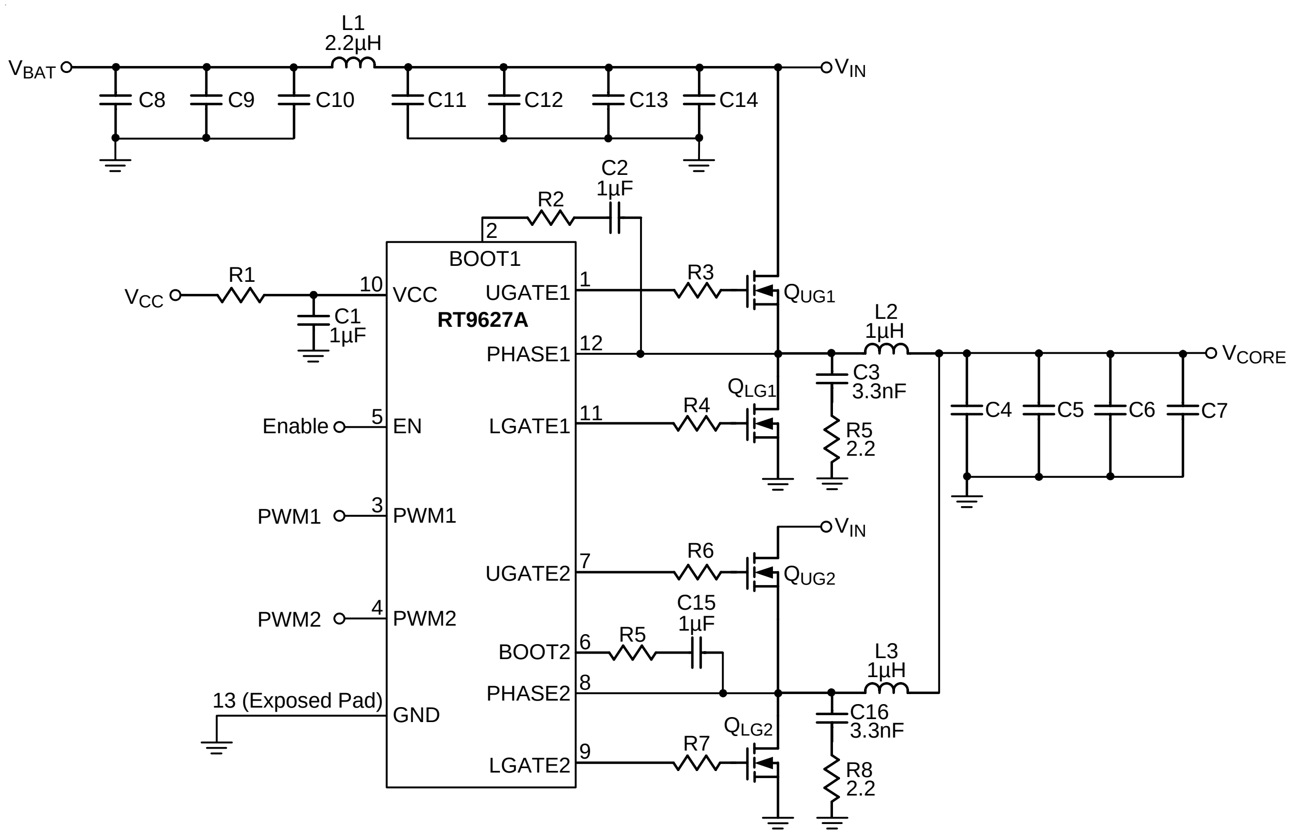
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended. The human body mode is a 100pF capacitor is charged through a 1.5kΩ resistor into each pin.

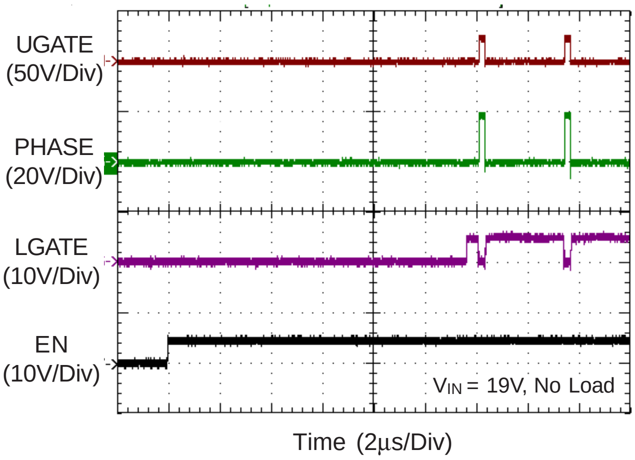
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

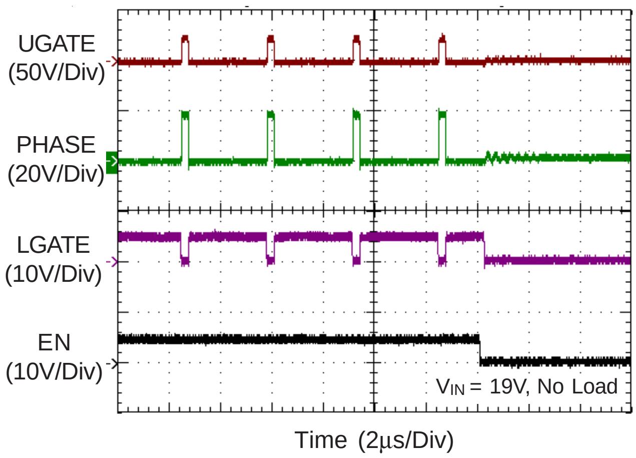


Typical Operating Characteristics

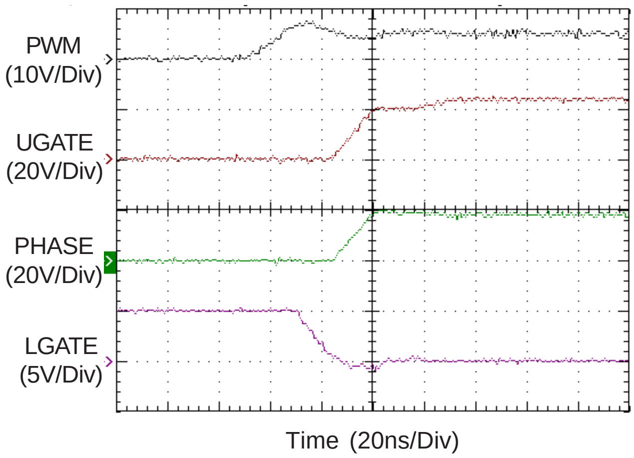
Driver Enable



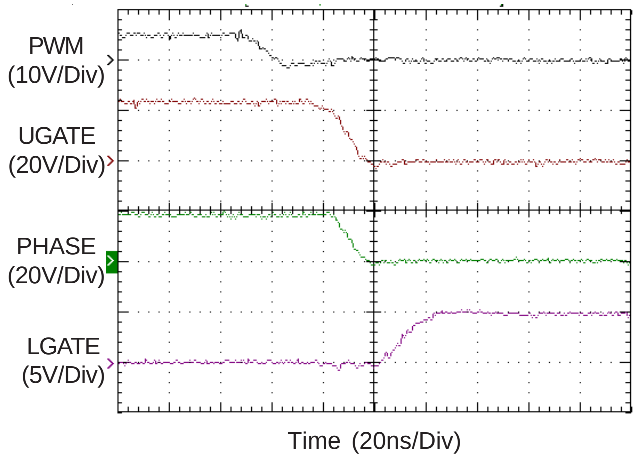
Driver Disable



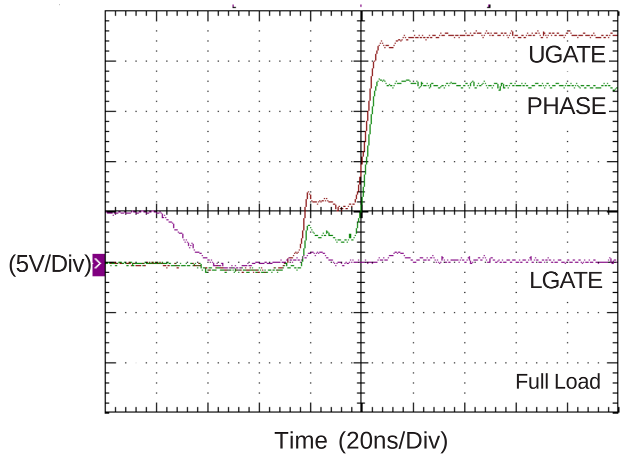
PWM Rising Edge



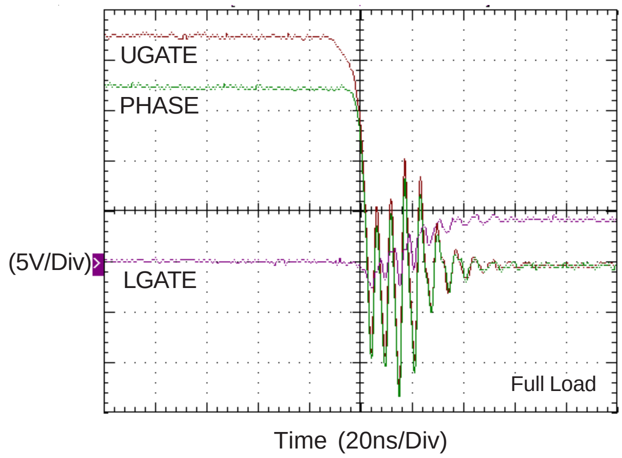
PWM Falling Edge

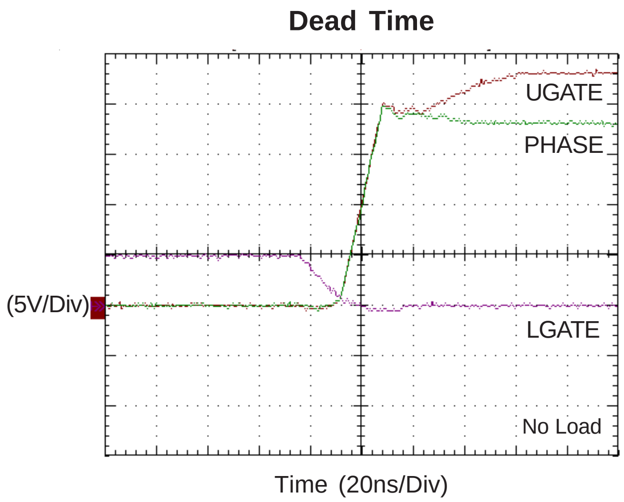


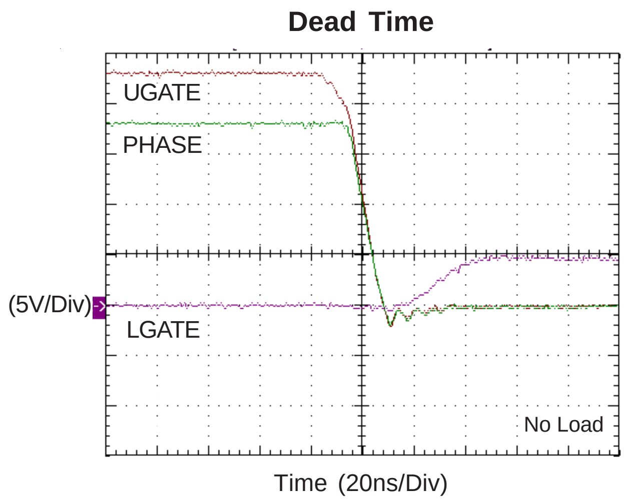
Dead Time

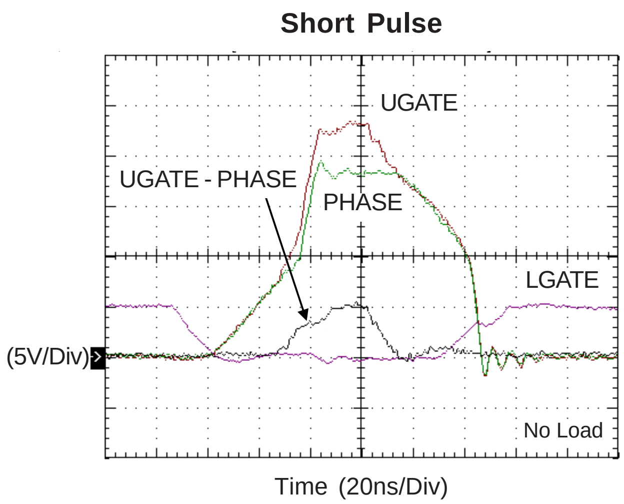


Dead Time




Dead Time
UGATE
PHASE
(5V/Div)
LGATE
No Load
Time (20ns/Div)


Dead Time
UGATE
PHASE
(5V/Div)
LGATE
No Load
Time (20ns/Div)


Short Pulse
UGATE
UGATE - PHASE
PHASE
LGATE
(5V/Div)
No Load
Time (20ns/Div)

Application Information

Supply Voltage and Power On Reset

The RT9627A is designed to drive two sets of both high side and low side N-MOSFETs through two externally input PWMx control signals. Connect 5V to VCC to power on the RT9627A. A minimum 1μF ceramic capacitor is recommended to bypass the supply voltage. Place the bypassing capacitor physically near the IC. The Power On Reset (POR) circuit monitors the supply voltage at the VCC pin. If VCC exceeds the POR rising threshold voltage, the controller resets and prepares for operation. UGATEx and LGATEx are held low before VCC is above the POR rising threshold.

Enable and Disable

The RT9627A includes an EN pin for sequence control. When the EN pin rises above the V_{ENH} trip point, the RT9627A begins a new initialization and follows the PWMx command to control the UGATEx and LGATEx. When the EN pin falls below the V_{ENL} trip point, the RT9627A shuts down and keeps UGATEx and LGATEx low.

Three State PWM Input

After initialization, the PWMx signal takes over the control. The rising PWMx signal first forces the LGATEx signal low and then allows the UGATEx signal to go high right after a non-overlapping time to avoid shoot-through current. In contrast, the falling PWMx signal first forces UGATEx to go low. When the UGATEx or PHASEx signal reach a predetermined low level, LGATEx signal is then allowed to go high.

Non-overlap Control

To prevent the overlap of the gate drives during the UGATEx pull low and the LGATEx pull high, the non-overlap circuit monitors the voltages at the PHASEx node and high side gate drive (UGATEx – PHASEx). When the PWMx input signal goes low, UGATEx begins to pull low (after propagation delay). Before LGATEx can pull high, the non-overlap protection circuit ensures that the monitored (UGATEx – PHASEx) voltages have gone below 1.1V or phase voltage is below 2V. Once the monitored voltages fall below the threshold, LGATEx begins to turn high. By waiting for the voltages of the PHASEx pin and high side gate drive to fall below their threshold, the non-overlap protection circuit ensures that UGATEx is low before LGATEx pulls high.

Also to prevent the overlap of the gate drives during LGATEx pull low and UGATEx pull high, the non-overlap circuit monitors the LGATEx voltage. When LGATEx go below 1.1V, UGATEx is allowed to go high.

Driving Power MOSFETs

The DC input impedance of the power MOSFET is extremely high. The gate draws the current only for few nano-amperes. Thus, once the gate has been driven up to "ON" level, the current could be negligible.

However, the capacitance at the Gate to Source terminal should be considered. It requires relatively large currents to drive the Gate up and down rapidly. It is also required to switch Drain current on and off with the required speed. The required gate drive currents are calculated as follows.

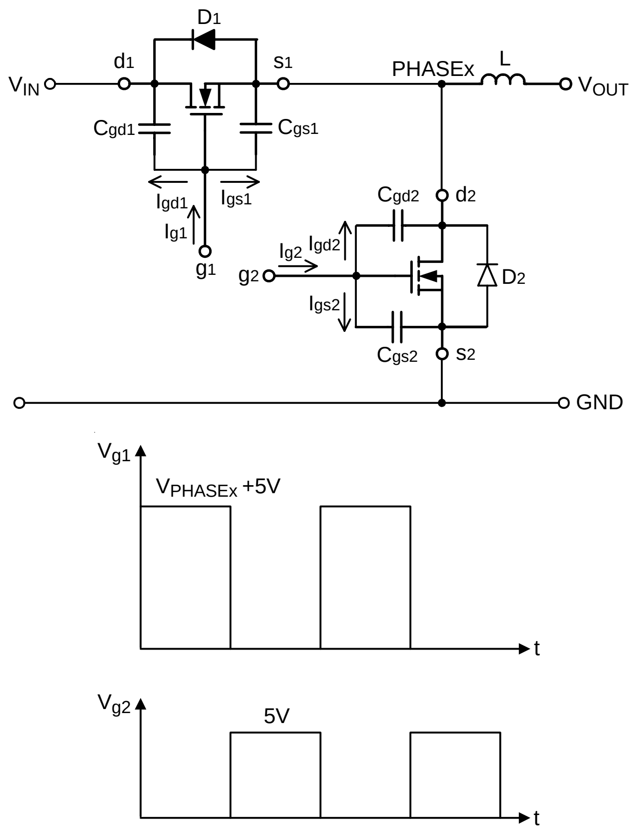


Figure1. Equivalent Circuit and Associated Waveforms

In Figure 1, the current I_{g1} and I_{g2} are required to move the gate up to 5V. The operation consists of charging C_{gd1}, C_{gd2}, C_{gs1} and C_{gs2}. C_{gs1} and C_{gs2} are the capacitors from Gate to Source of the high side and the low side power MOSFETs, respectively. In general data sheets, the C_{gs1} and C_{gs2} are referred as "C_{iss}" which are the input capacitors. C_{gd1} and C_{gd2} are the capacitors from Gate to Drain of the high side and the low side power MOSFETs, respectively and referred to the data sheets as "C_{rss}" the reverse transfer capacitance. For example, t_{r1} and t_{r2} are the rising time of the high side and the low side power MOSFETs respectively, the required current I_{gs1} and I_{gs2}, are shown as below :

$$I_{gs1} = C_{gs1}\frac{dV_{g1}}{dt} = \frac{C_{gs1} \times 5}{t_{r1}} \quad (1)$$

$$I_{gs2} = C_{gs1}\frac{dV_{g2}}{dt} = \frac{C_{gs1} \times 5}{t_{r2}} \quad (2)$$

Before driving the Gate of the high side MOSFET up to 5V, the low side MOSFET has to be off; the high side MOSFET is turned off before the low side is turned on. From Figure 1, the body diode "D_2" had been turned on before high side MOSFETs turned on.

$$I_{gd1} = C_{gd1}\frac{dV}{dt} = C_{gd1}\frac{5}{t_{r1}} \quad (3)$$

Before the low side MOSFET is turned on, the C_{gd2} have been charged to V_{IN}. Thus, as C_{gd2} reverses its polarity and g_2 is charged up to 5V, the required current is :

$$I_{gd2} = C_{gd2}\frac{dV}{dt} = C_{gd2}\frac{Vi+5}{t_{r2}} \quad (4)$$

It is helpful to calculate these currents in a typical case. Assume a synchronous rectified Buck converter, input voltage V_{IN} = 12V, $V_{g1} = V_{g2}$ = 5V. The high side MOSFET is PHB83N03LT whose C_{iss} = 1660pF, C_{rss} = 380pF, and t_r = 14ns. The low side MOSFET is PHB95N03LT whose C_{iss} = 2200pF, C_{rss} = 500pF and t_r = 30ns, from the equation (1) and (2) we can obtain :

$$I_{gs1} = \frac{1660 \times 10^{-12} \times 5}{14 \times 10^{-9}} = 0.593 \quad (A) \quad (5)$$

$$I_{gs2} = \frac{2200 \times 10^{-12} \times 5}{30 \times 10^{-9}} = 0.367 \quad (A) \quad (6)$$

from equation. (3) and (4)

$$I_{gd1} = \frac{380 \times 10^{-12} \times 5}{14 \times 10^{-9}} = 0.136 \quad (A) \quad (7)$$

$$I_{gd2} = \frac{500 \times 10^{-12} \times (12+5)}{30 \times 10^{-9}} = 0.283 \quad (A) \quad (8)$$

the total current required from the gate driving source can be calculated as following equations :

$$I_{g1} = I_{gs1} + I_{gd1} = (0.593 + 0.136) = 0.729 \quad (A) \quad (9)$$

$$I_{g2} = I_{gs2} + I_{gd2} = (0.367 + 0.283) = 0.65 \quad (A) \quad (10)$$

By a similar calculation, we can also get the sink current required from the turned off MOSFET.

Select the Bootstrap Capacitor

Figure 2 shows part of the bootstrap circuit of the RT9627A. The V_{CB} (the voltage difference between BOOTx and PHASEx on RT9627A) provides a voltage to the Gate of the high side power MOSFET. This supply needs to be ensured that the MOSFET can be driven. For this, the capacitance C_B has to be selected properly. It is determined by following constraints.

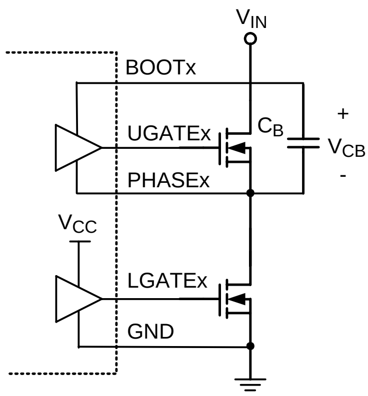


Figure 2. Part of Bootstrap Circuit of RT9627A

In practice, a low value capacitor C_B will lead to the over charging that could damage the IC. Therefore, to minimize the risk of overcharging and to reduce the ripple on V_{CB}, the bootstrap capacitor should not be smaller than 0.1μF, and the larger the better. In general design, using 1μF can provide better performance. At least one low ESR capacitor should be used to provide good local de-coupling. It is recommended to adopt a ceramic or tantalum capacitor.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-12L 3x3 package, the thermal resistance, θ_{JA}, is 30.5°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (30.5°C/W) = 3.28W for WDFN-12L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

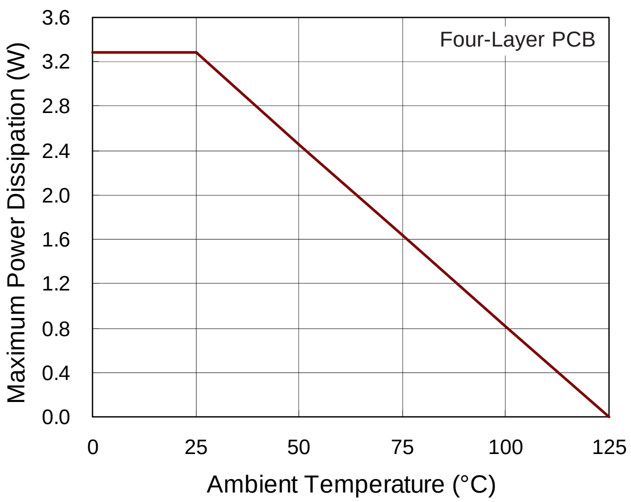


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

Figure 4 shows the schematic circuit of a synchronous Buck converter to implement the RT9627A.

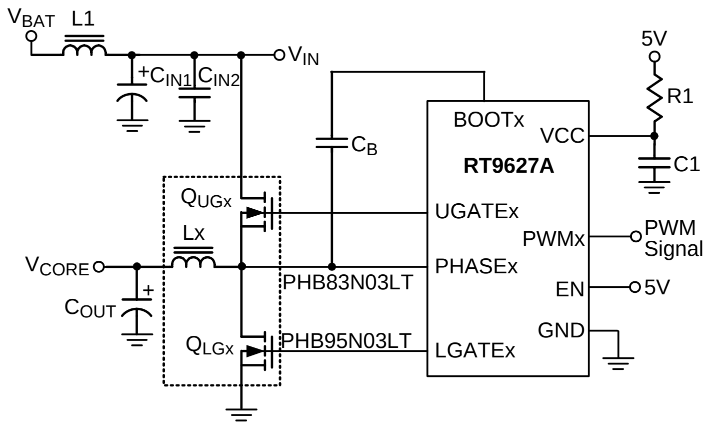
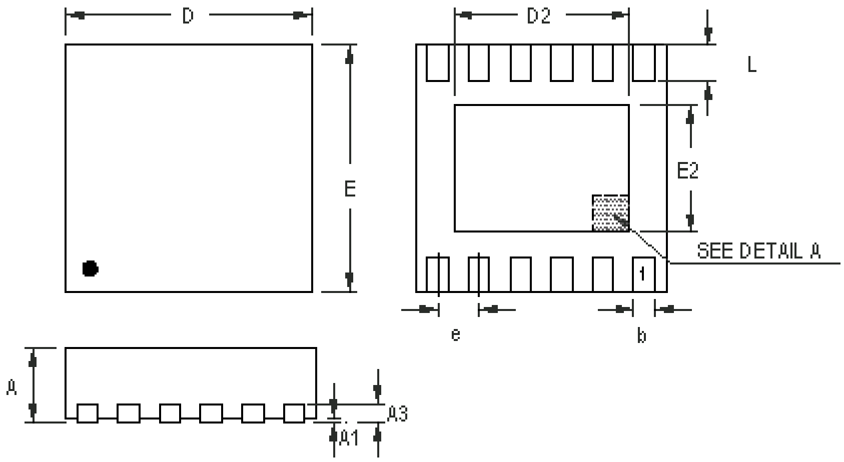


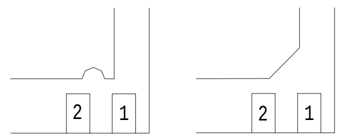
Figure 4. Synchronous Buck Converter Circuit

When layout the PCB, it should be very careful. The power circuit section is the most critical one. If not configured properly, it will generate a large amount of EMI. The junction of Q_{UGx}, Q_{LGx}, Lx should be very close.

Next, the trace from UGATEx, and LGATEx should also be short to decrease the noise of the driver output signals. PHASEx signals from the junction of the power MOSFET, carrying the large gate drive current pulses, should be as heavy as the gate drive trace. The bypass capacitor C1 should be connected to GND directly. Furthermore, the bootstrap capacitors (C_B) should always be placed as close to the pins of the IC as possible.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.400	1.750	0.055	0.069
e	0.450		0.018	
L	0.350	0.450	0.014	0.018

W-Type 12L DFN 3x3 Package

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