PAM2303

3A Low Noise Step-Down DC-DC Converter

Features

- Output Current: Up to 3A
- Output Voltage: 0.6V to V_{IN}
- Input Voltage: 2.7 to 5.5V
- Efficiency up to 95%
- 42μA (Typ) No Load Quiescent Current
- Shutdown Current: <1μA
- 100% Duty Cycle Operation
- 1.5MHz Switching Frequency
- Analog Soft Start
- No external Compensation Required
- Current Limit Protection
- Thermal Shutdown
- SOP-8(EP), DFN3X3-10 and QFN3X3-16 Package

Applications

- 5V or 3.3V Point of Load Conversion
- Telecom/Networking Equipment
- Set Top Boxes
- Storage Equipment
- Video Cards
- DDR Power Supply

Description

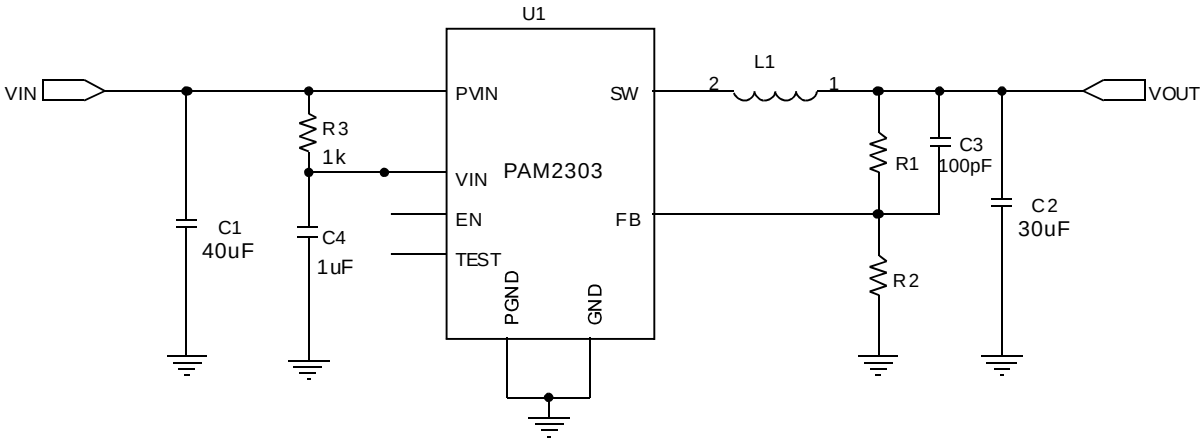
The PAM2303 is a 3A step-down DC-DC converter. It operates in two different modes: PSM and PWM modes. At light load, it automactically enters into the PSM mode to improve efficiency. At heavy load, the constant-frequency PWM control performs excellent stability and transient response. No external compensation components are required.

The PAM2303 supports a range of input voltages from 2.7V to 5.5V. The output voltage is adjustable from 0.6V to the input voltage. The PAM2303 employs internal power switch and synchronous rectifier to minimize external part count and realize high efficiency. During shutdown, the input is disconnected from the output and the shutdown current is less than 1μA. Other key features include over-temperature and short circuit protection, and under-voltage lockout to prevent deep battery discharge.

The PAM2303 delivers 3A maximum output current while consuming only 42μA of no-load quiescent current. Ultra-low RDS(ON) integrated MOSFETs and 100% duty cycle operation make the PAM2303 an ideal choice for high output voltage, high current applications which require a low dropout threshold.

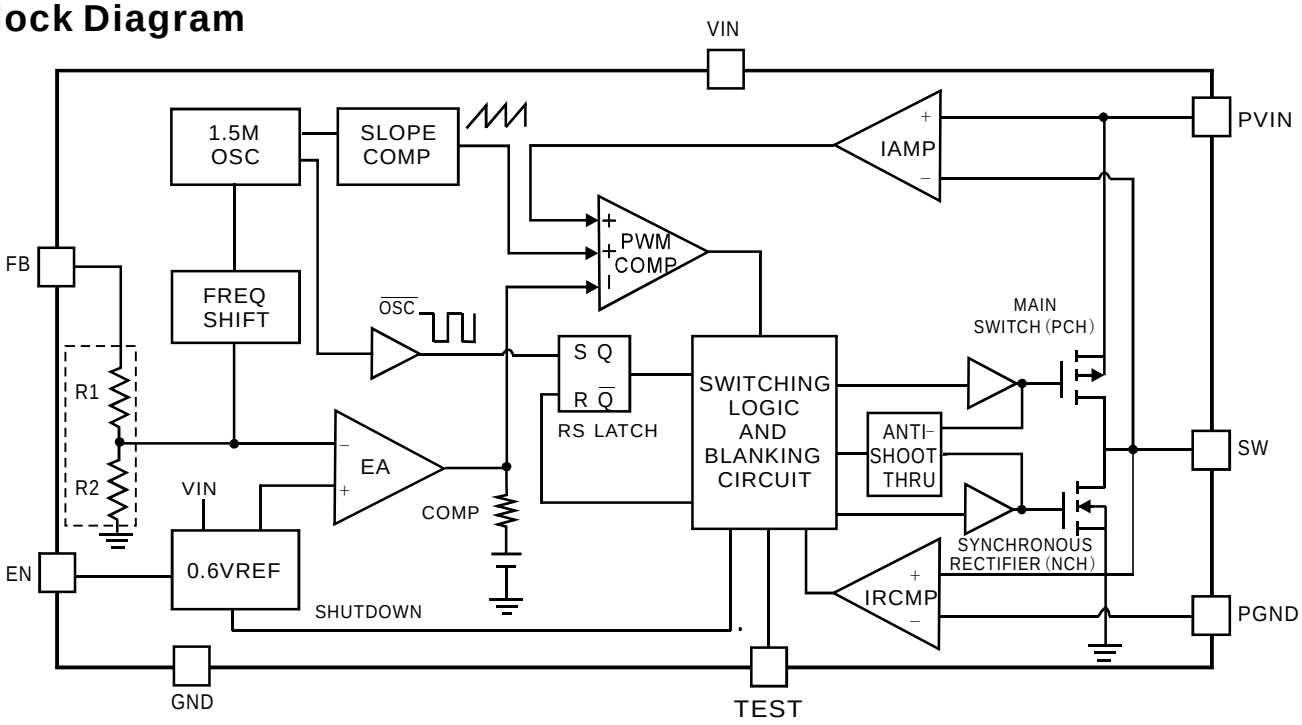
The PAM2303 is available in SOP-8(EP), DFN3X3-10, and QFN3X3-16 package.

Typical Application



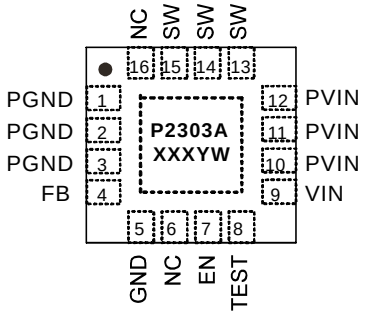
$$V_O = 0.6 \times \left(1 + \frac{R1}{R2}\right)$$

Block Diagram

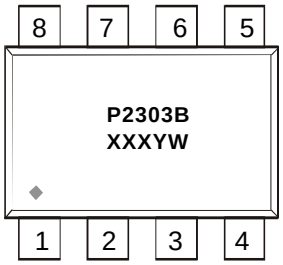


Pin Configuration & Marking Information

Top View
QFN 3X3-16



Top View
SOP-8(EP)

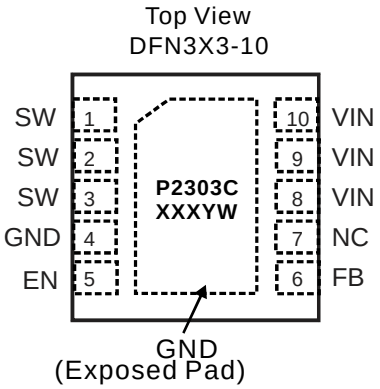


A/B: Pin Configuration
Y: Year
W: Week
X: Internal Code

Pin Description

Name	QFN3X3-16	SOP-8(EP)	Function
PGND	1,2,3	2	Main power ground pin
FB	4	3	Feedback voltage to internal error amplifier, the threshold voltage is 0.6V.
GND	5	4	Signal ground for small signal components.
NC	6,16	-	No connected
EN	7	5	Enable control input. Force this pin voltage above 1.5V, enables the chip, and below 0.3V shuts down the device.
Test	8	6	Test mode. "Low" connection is recommended.
VIN	9	7	Bias supply. Chip main power supply pin
PVIN	10,11,12	8	Input supply for power stage. Must be closely decoupled to PGND
SW	13,14,15	1	The drains of the internal main and synchronous power MOSFET.

Pin Configuration & Marking Information



C: Pin Configuration
Y: Year
W: Week
X: Internal Code

Pin Description

Name	DFN3X3-10	Function
SW	1,2,3	The drains of the internal main and synchronous power MOSFET.
GND	4	GND
EN	5	Enable control input. Force this pin voltage above 1.5V, enables the chip, and below 0.3V shuts down the device.
FB	6	Feedback voltage to internal error amplifier, the threshold voltage is 0.6V.
NC	7	No connected
VIN	8,9,10	Bias supply. Chip main power supply pin

Absolute Maximum Ratings

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Input Voltage PV_{IN}, V_{IN}.....6V
SW Pin Voltage.....-0.3V to (PV_{IN}+0.3V)
FB Pin Voltage.....-0.3V to (V_{IN}+0.3V)
EN Pin Voltage.....-0.3V to -6V

Maximum Junction Temperature.....150°C
Storage Temperature Range.....-65°C to 150°C
Soldering Temperature.....300°C, 5sec

Recommended Operating Conditions

Supply Voltage.....2.7V to 5.5V

Junction Temperature Range.....-40°C to 125°C
Ambient Temperature Range.....-40°C to 85°C

Thermal Information

Parameter	Symbol	Package	Maximum	Unit
Thermal Resistance (Junction to Ambient)	θ_{JA}	SOP-8(EP)	90	°C/W
		DFN3X3-10	60	
		QFN3X3-16	35	
Thermal Resistance (Junction to Case)	θ_{JC}	SOP-8(EP)	11	°C/W
		DFN3X3-10	8.5	
		QFN3X3-16	11	

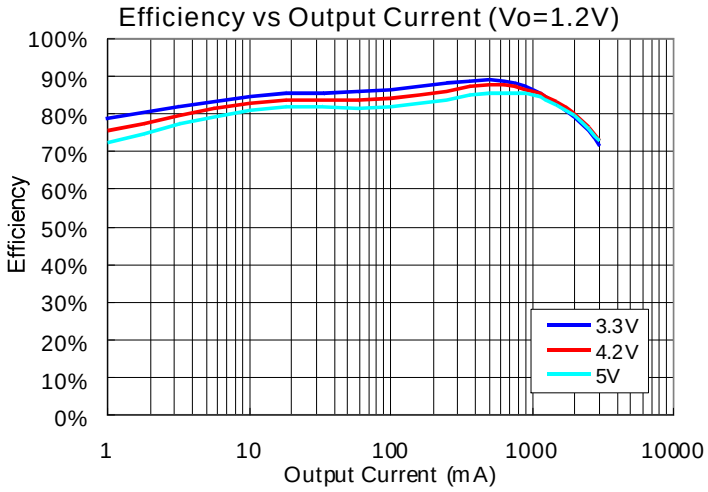
Electrical Characteristic

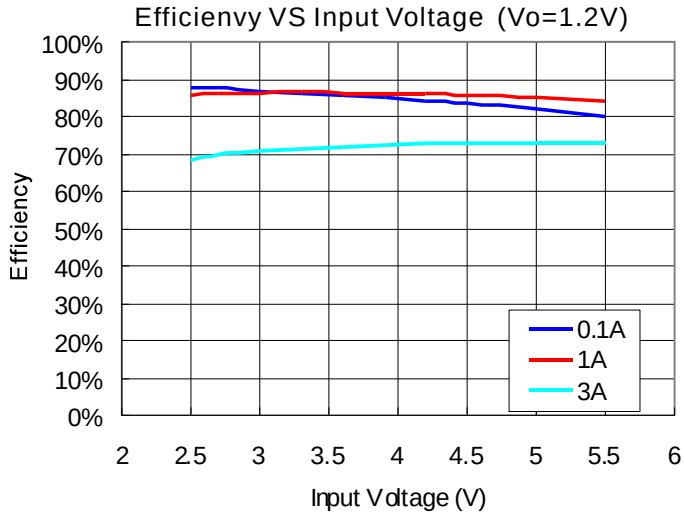
T_A=25°C, Vin=3.6V, Vo=1.8V, Cin=33uF,Co=22uF, L=2.2uH, unless otherwise noted.

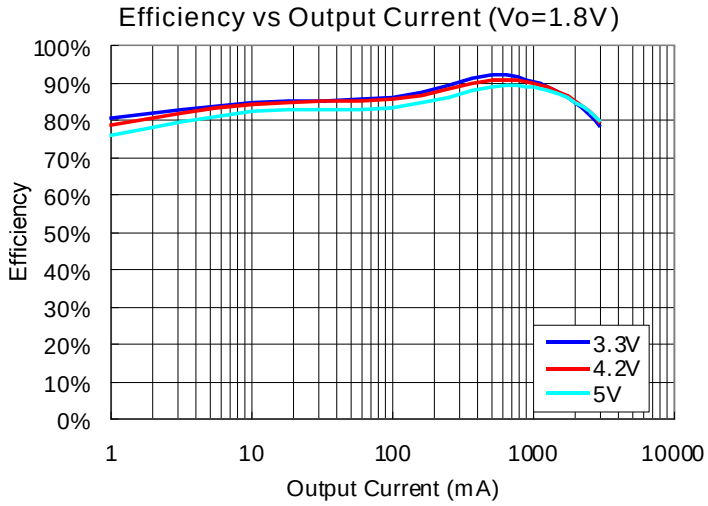
PARAMETER	SYMBOL	Test Conditions		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			2.7		5.5	V
Output Voltage Range	V_O			0.6		V_{IN}	V
UVLO Threshold	V_{UVLO}	V_{IN} Rising			2.4	2.5	V
		Hysteresis			240		mV
		V_{IN} Falling		1.8			V
Regulated Output Voltage Accuary	V_O	I_O = 0 to 3A		-3		+3	%
Regulated Feedback Voltage	V_{FB}			0.591	0.6	0.609	V
FB Leakage Current	I_{FB}	V_O=1V		-50		+50	nA
Output Voltage Line Regulation	LNR	V_{IN} = 2.5V to 5V			0.2		%/V
Output Voltage Load Regulation	LDR	I_O=0A to 3A			0.5		%/A
Quiescent Current	I_Q	No load			42	90	µA
Shutdown Current	I_{SD}	V_{EN} = 0V				1	µA
Current Limit	I_{LIM}				4		A
Oscillator Frequency	f_{OSC}			1.2	1.5	1.8	MHz
Drain-Source On-State Resistance	$R_{DS(ON)}$		High Side		85		mΩ
			Low Side		60		mΩ
High Efficiency	η				95		%
PSM Threshold	I_{TH}	Vin=3.3V,Vo=1.2V,L=1uH				450	mA
Analog Soft Start Time	t_S	From enable to output regulation			0.5		ms
EN Threshold High	V_{EH}			1.5			V
EN Threshold Low	V_{EL}					0.3	V
EN Leakage Current	I_{EN}	V_{IN}=V_{EN} = 0V		-1.0		1.0	µA
Over Temperature Protection	OTP				150		°C
OTP Hysteresis	OTH				30		°C

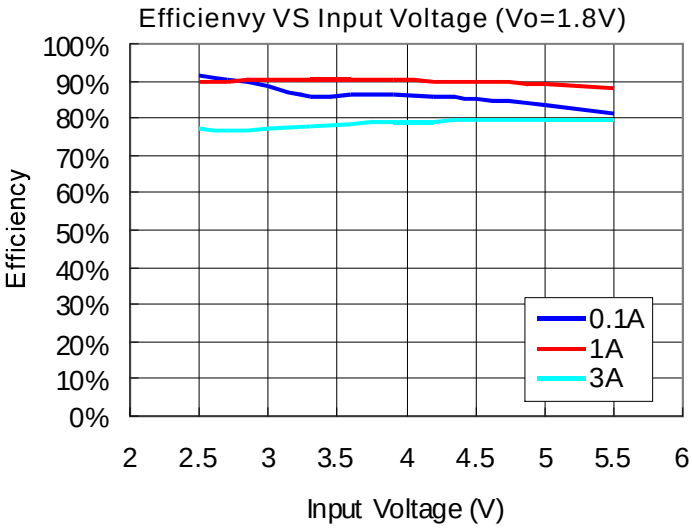
Typical Performance Characteristics

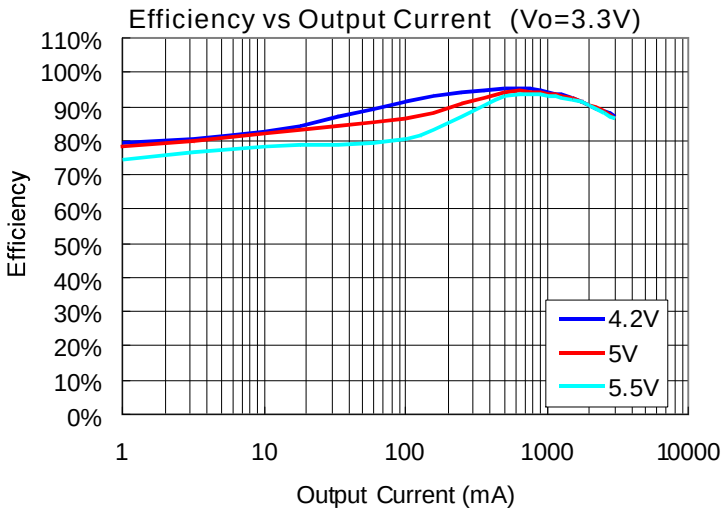
T_A=25°C, C_{IN}=33uF,Co=22µF unless otherwise noted.

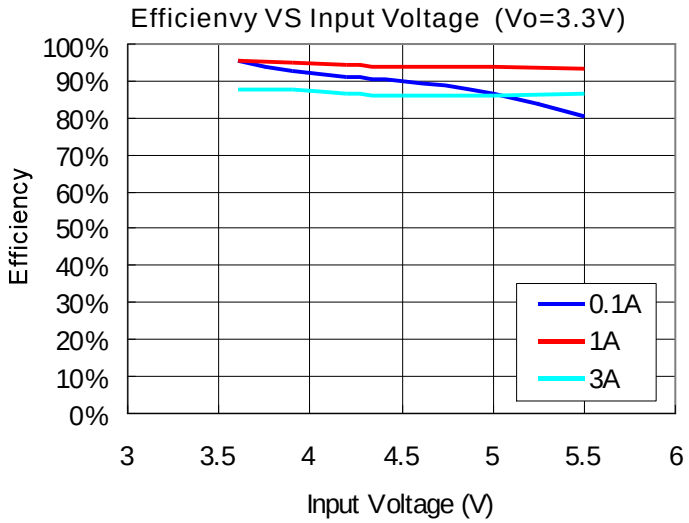












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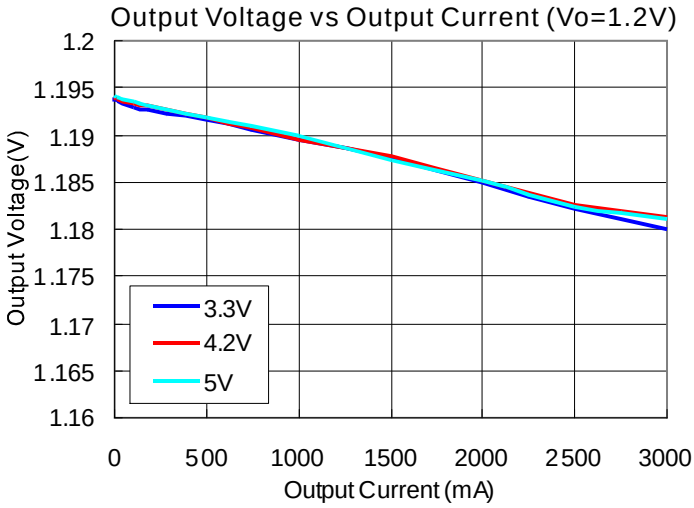
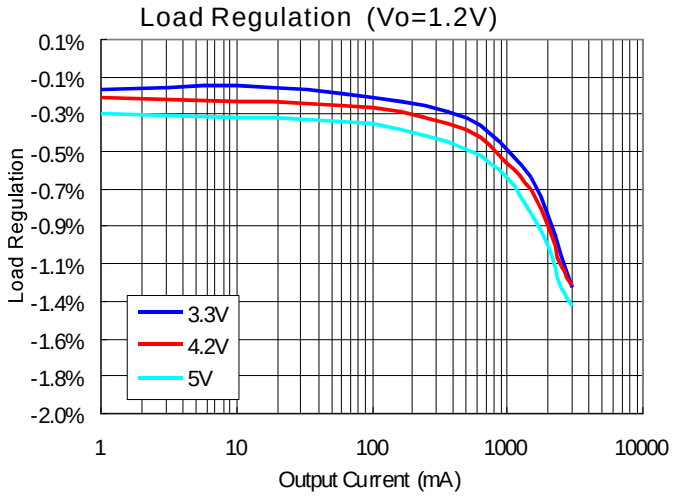
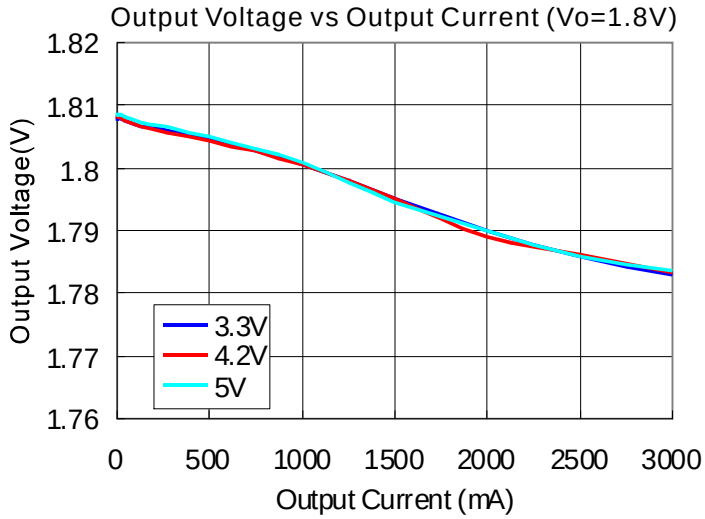
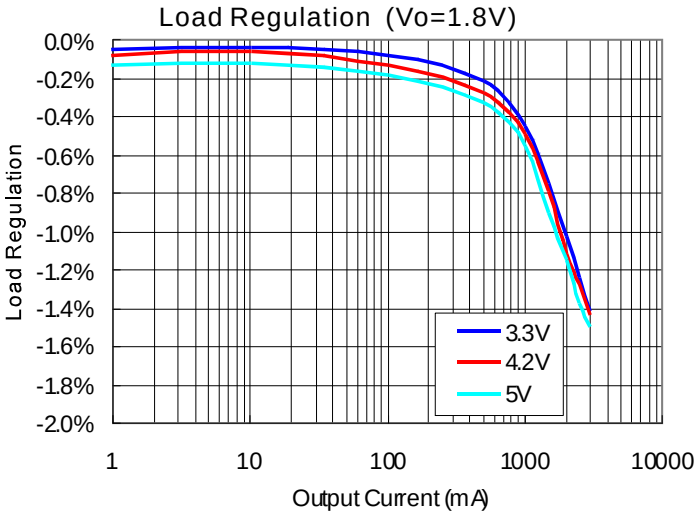
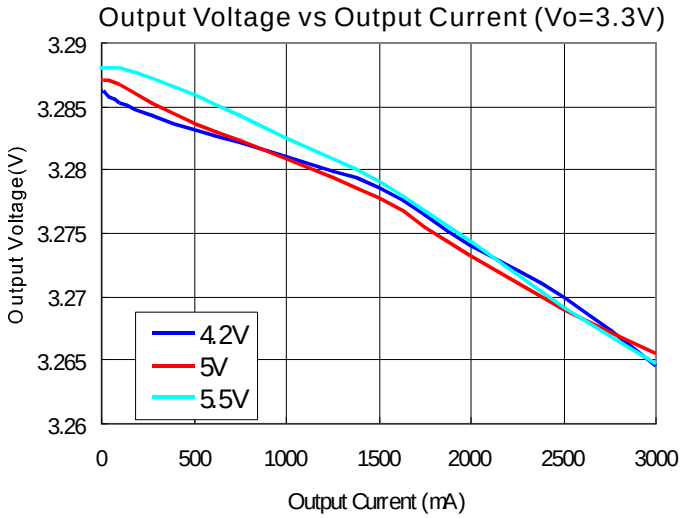
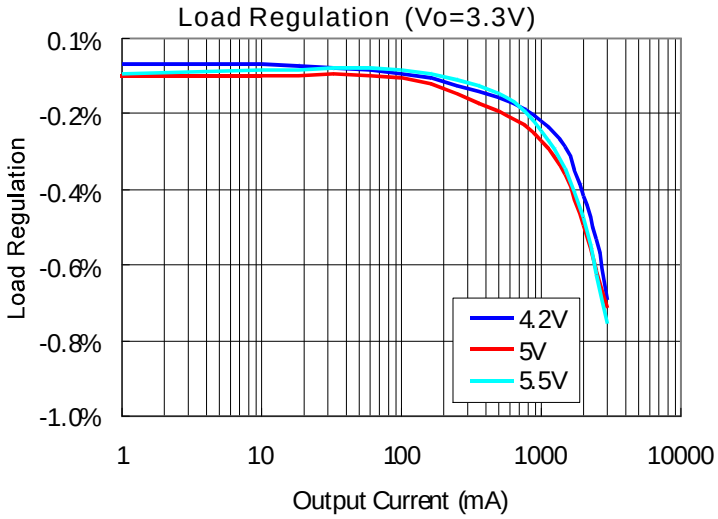








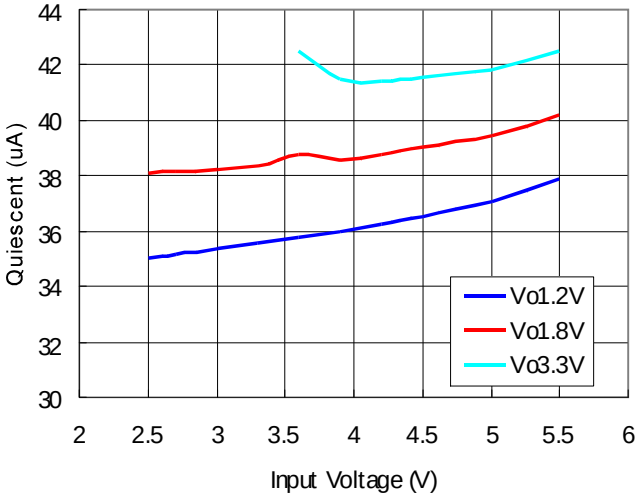




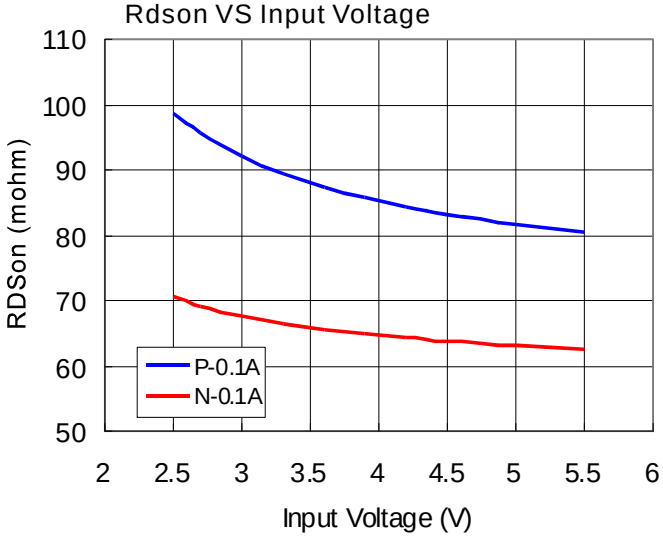
Typical Performance Characteristics

T_A=25°C, C_{IN}=33uF,Co=22µF unless otherwise noted.

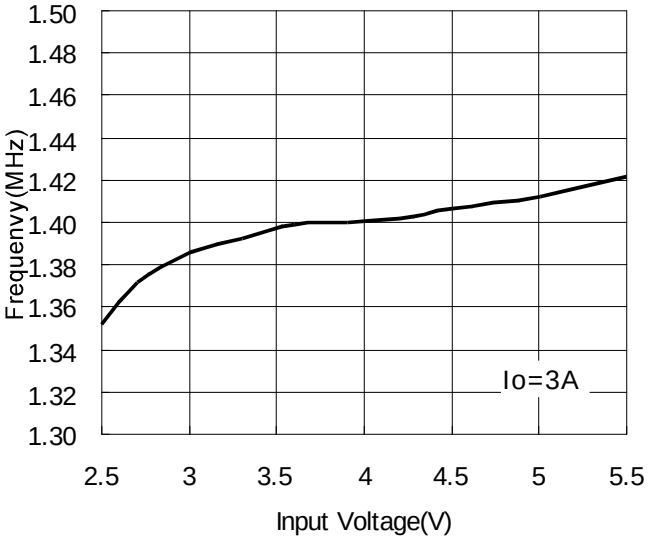
Quiescent Current VS Input Voltage



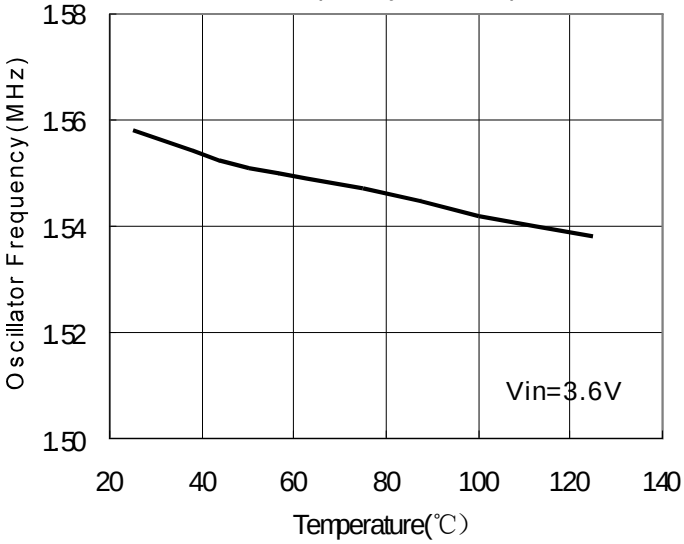
Rdson VS Input Voltage



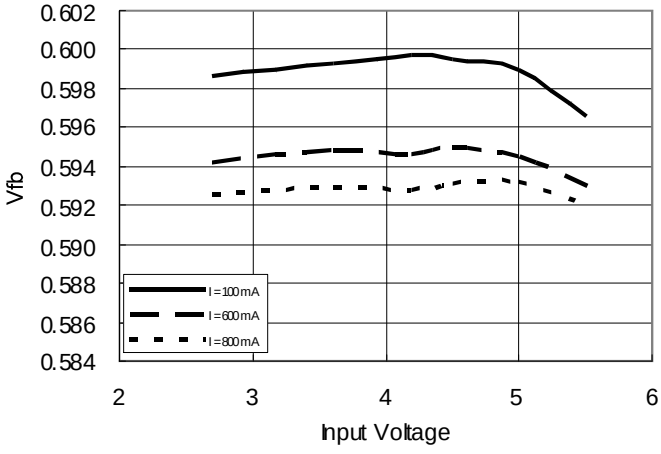
Oscillator Frequency VS Input Voltage



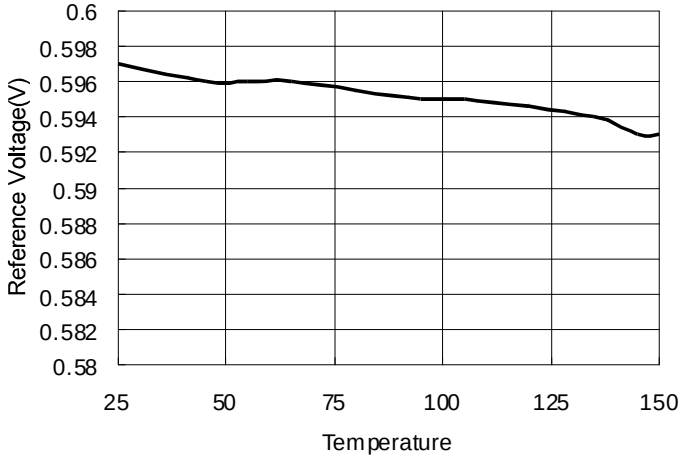
Oscillator Frequency VS Temperature



Reference Voltage VS Input Voltage



Reference Voltage VS Temperature



Application Information

The basic PAM2303 application circuit is shown in Page 1. External component selection is determined by the load requirement, selecting L first and then Cin and Cout.

Inductor Selection

For most applications, the value of the inductor will fall in the range of 1µH to 3.3µH. Its value is chosen based on the desired ripple current and efficiency. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V_{IN} or Vout also increases the ripple current as shown in equation 3A reasonable starting point for setting ripple current is $\triangle I_L$ = 1.2A (40% of 3A).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 4.2A rated inductor should be enough for most applications (3A + 1.2A). For better efficiency, choose a low DC-resistance inductor.

Vo	1.2V	1.5V	1.8V	2.5V	3.3V
L	1µH	1.5µH	2.2µH	2.2µH	3.3µH

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle Vout/Vin. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \cong I_{OMAX} \frac{\left[V_{OUT}(V_{IN}-V_{OUT})\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at V_{IN} =2Vout, where $I_{RMS}=I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Consult the manufacturer if there is any question.

The selection of Cout is driven by the required effective series resistance (ESR).

Typically, once the ESR requirement for Cout has been met, the RMS current rating generally far exceeds the I_{RIPPLE}(P-P) requirement. The output ripple △Vout is determined by:

$$\triangle Vout \approx \triangle I_L (ESR + 1/8fCout)$$

Where f = operating frequency, C_{OUT}=output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Using ceramic capacitors can achieve very low output ripple and small circuit size.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Thermal consideration

Thermal protection limits power dissipation in the PAM2303. When the junction temperature exceeds 150°C, the OTP (Over Temperature Protection) starts the thermal shutdown and turns the pass transistor off. The pass transistor resumes operation after the junction temperature drops below 120°C.

For continuous operation, the junction temperature should be maintained below 125°C. The power dissipation is defined as:

$$P_D = I_O^2 \frac{V_O R_{DSONH} + (V_{IN} - V_O) R_{DSONL}}{V_{IN}} + (t_{SW} F_S I_O + I_Q) V_{IN}$$

I_Q is the step-down converter quiescent current. The term tsw is used to estimate the full load step-down converter switching losses.

For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_D=I_O^2 R_{DSONH}+I_Q V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surrounding airflow and temperature difference between junction and ambient. The maximum power dissipation can be calculated by the following formula:

$$P_D=\frac{T_{J(MAX)}-T_A}{\theta_{JA}}$$

Where TJ(max) is the maximum allowable junction temperature 125°C.T_A is the ambient temperature and θ_{JA} is the thermal resistance from the junction to the ambient. Based on the standard JEDEC for a two layers thermal test board, the thermal resistance θ_{JA} of QFN3X3-16 68°C/W and SOP-8(EP) 90°C/W respectively. The maximum power dissipation at T_A = 25°C can be calculated by following formula:

P_D=(125°C-25°C)/68°C/W=1.47W(QFN3X3-16)
P_D=(125°C-25°C)/90°C/W=1.11W(SOP-8)

Setting the Output Voltage

The internal reference is 0.6V (Typical). The output voltage is calculated as below:
The output voltage is given by Table 1.

$$V_O=0.6\times\left(1+\frac{R1}{R2}\right)$$

Table 1: Resistor recommend for output voltage setting

Vo	R1	R2
1.2V	150k	150k
1.5V	225k	150k
1.8V	300k	150k
2.5V	475k	150k
3.3V	680k	150k

Pulse Skipping Mode (PSM) Description

When load current decreases, the peak switch current in Power-PMOS will be lower than skip current threshold and the device will enter into Pulse Skipping Mode.

In this mode, the device has two states, working state and idle state. First, the device enters into working state controlled by internal error amplifier.When the feedback voltage gets higher than internal reference voltage, the device will enter into low I_Q idle state with most of internal blocks disabled. The output voltage will be reduced by loading or leakage current. When the feedback voltage gets lower than the internal reference voltage, the convertor will start a working state again.

100% Duty Cycle Operation

As the input voltage approaches the output voltage, the converter turns the P-channel transistor continuously on. In this mode the output voltage is equal to the input voltage minus the voltage drop across the P - channel transistor:

$$V_{OUT}=V_{IN}-I_{LOAD}(R_{dson}+R_L)$$

where R_{dson} = P-channel switch ON resistance, I_{LOAD} = Output current, R_L = Inductor DC resistance

UVLO and Soft-Start

The reference and the circuit remain reset until the VIN crosses its UVLO threshold.

The PAM2303 has an internal soft-start circuit that limits the in-rush current during start-up. This prevents possible voltage drops of the input voltage and eliminates the output voltage overshoot. The soft-start make the output voltage rise up smoothly.

Short Circuit Protection

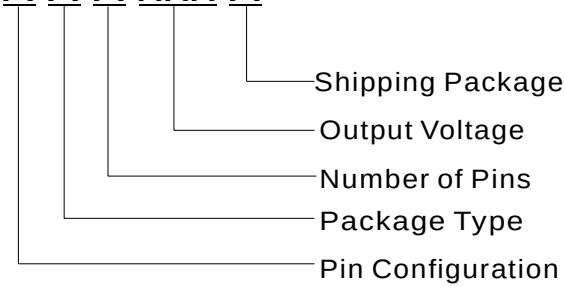
The switch peak current is limited cycle-by-cycle to a typical value of 4A. In the event of an output voltage short circuit, the device operates with a frequency of 500kHz and minimum duty cycle, therefore the average input current is more smaller than current limit.

Thermal Shutdown

When the die temperature exceeds 150°C, a reset occurs and the reset remains until the temperature decrease to 120°C, at which time the circuit can be restarted.

Ordering Information

PAM 2303 X X X xxx X

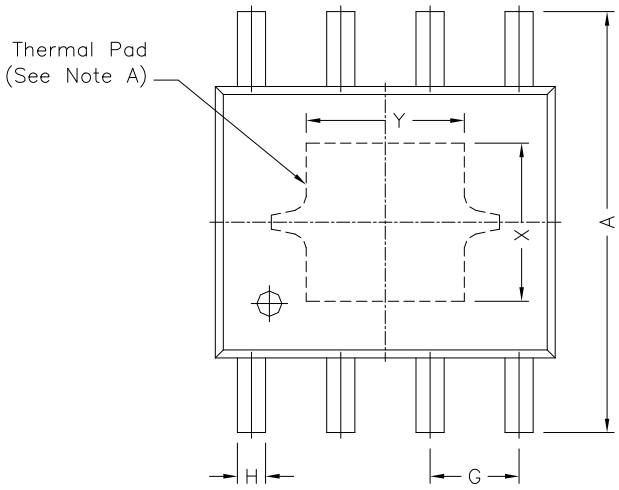


Pin Configuration	Package Type	Number of Pins	Output Voltage
A Type 16 pins	J: QFN3X3-16	E: 16	ADJ: Adj
B Type 8 pins	E: SOP-8(EP)	C: 8	ADJ: Adj
C Type 10 pins	F: DFN3X3-10	G: 10	ADJ: Adj

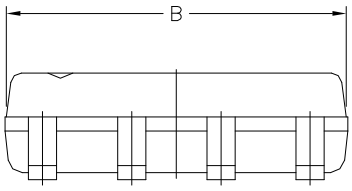
Part Number	Output Voltage	Package Type	Shipping Package
PAM2303AJEADJR	ADJ	QFN3X3-16	3,000 Units/Tape & Reel
PAM2303BECADJR	ADJ	SOP-8(EP)	2,500 Units/Tape & Reel
PAM2303CFGADJR	ADJ	DFN3X3-10	3,000 Units/Tape & Reel

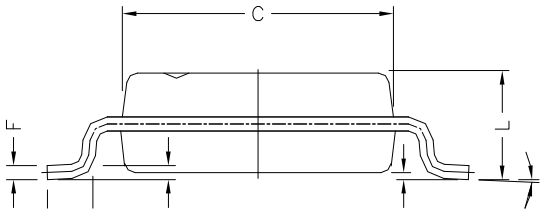
Outline Dimensions

SOP-8(EP)



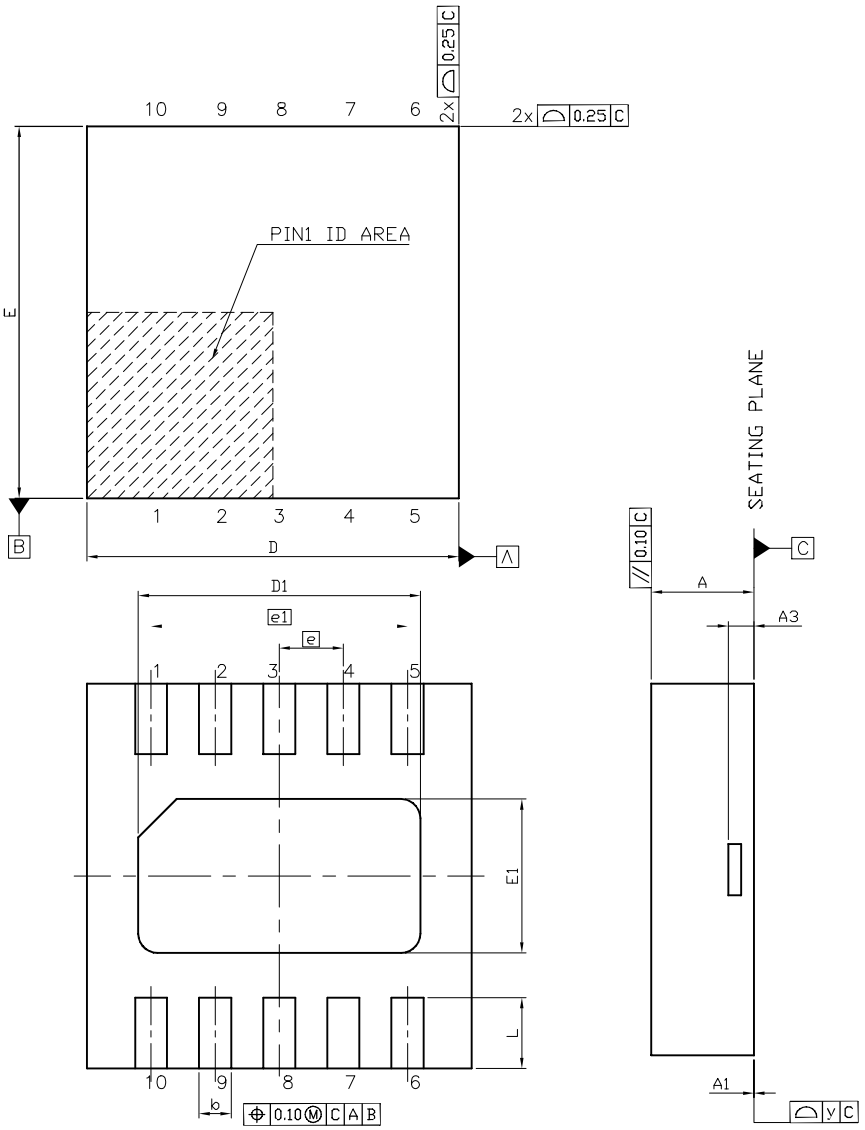
REF.		DIMENSIONS	
		Millimeters	
		Min.	Max.
A		5.80	6.20
B		4.80	5.00
C		3.80	4.00
D		0°	8°
E		0.40	0.90
F		0.19	0.25
M		0	0.15
H		0.35	0.49
L		1.35	1.75
G		1.27 TYP.	
Option1	X	2.28	
	Y	2.28	
Option2	X	2.41	
	Y	3.30	





Outline Dimensions

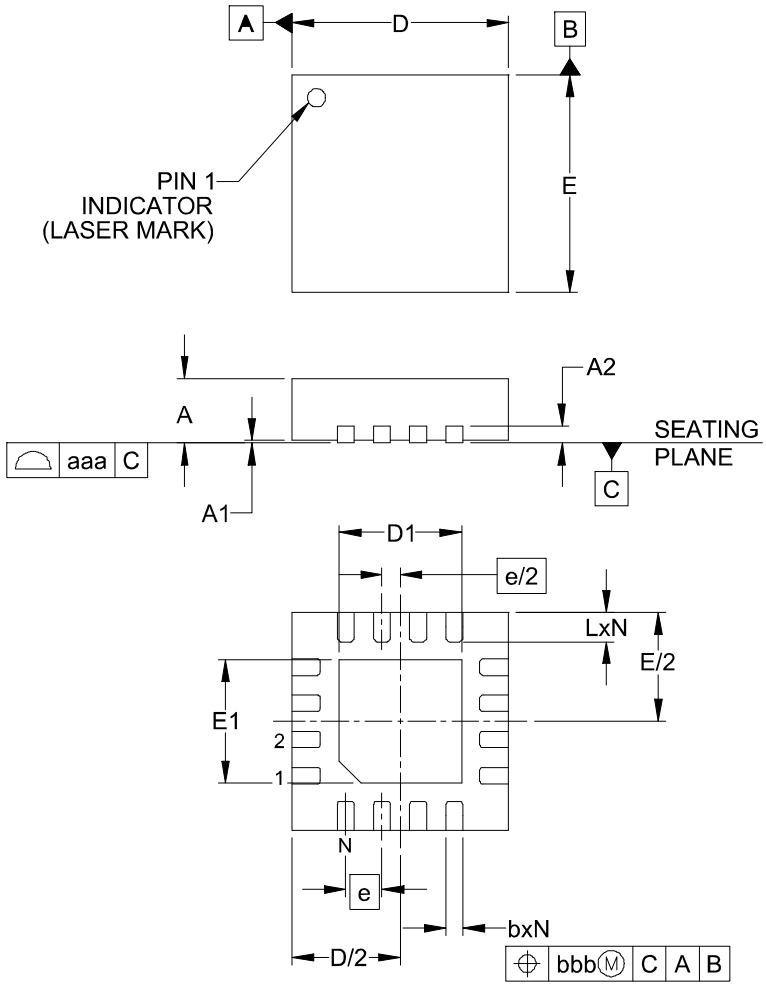
DFN3X3-10



SYMBOL	DIMENSION (MM)		
	MIN	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.18	0.25	0.30
D	2.90	3.00	3.10
D1	2.10	2.20	2.30
E	2.90	3.00	3.10
E1	1.10	1.20	1.30
L	0.45	0.55	0.65
e		0.50 BASIC	
e1		2.00 BASIC	
y	0		0.08

Outline Dimensions

QFN3X3-16



DIMENSIONS (Millieters)			
	MIN	TYP	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A2		0.20	
b	0.18	0.25	0.30
D	2.90	3.00	3.10
D1	1.55	1.70	1.80
E	2.90	3.00	3.10
E1	1.55	1.70	1.80
e		0.50BSC	
L	0.30	0.40	0.50
N		16	
aaa		0.08	
bbb		0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP IS 1.90 x 1.90mm.