NCV8403

Product Preview

Self-Protected Low Side Driver with Temperature and Current Limit

42 V, 14 A, Single N−Channel, SOT−223

NCV8403 is a three terminal protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments. There is a fault feedback feature by monitoring the input current at the gate or voltage if a resistor is utilized.

Features

- Short Circuit Protection
- Thermal Shutdown with Automatic Restart
- Over Voltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- RoHs Compliant
- AEC-Q101 Qualified
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- This is a Pb−Free Device

Typical Applications

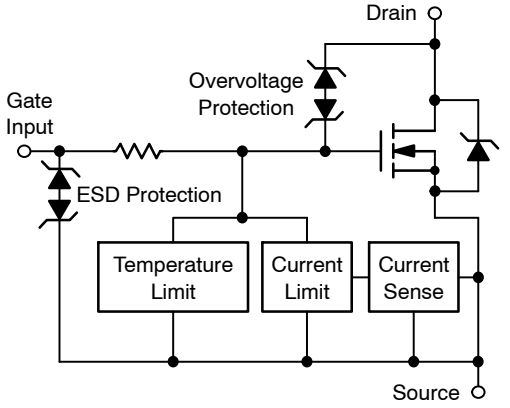
- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

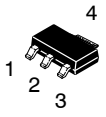
This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

ON Semiconductor®

http://onsemi.com

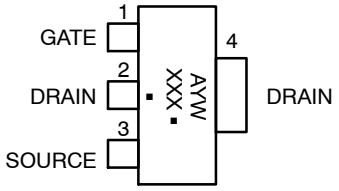
V_{DSS} (Clamped)	$R_{DS(on)}$ TYP	I_D MAX (Limited)
42 V	53 mΩ @ 10 V	15 A





SOT−223
CASE 318E
STYLE 3

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
XXX = Specific Device Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

© Semiconductor Components Industries, LLC, 2009

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage Internally Clamped	V_{DSS}	42	Vdc
Gate−to−Source Voltage	V_{GS}	±14	Vdc
Drain Current Continuous	I_D	Internally Limited	
Total Power Dissipation @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 2)	P_D	 1.25 1.9	W
Thermal Resistance Junction−to−Case Junction−to−Ambient (Note 1) Junction−to−Ambient (Note 2)	 $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 12 100 65	°C/W
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, I_L = 7.0 Apk, L = 9.5 mH, R_G = 25 Ω)	E_{AS}	233	mJ
Operating and Storage Temperature Range (Note 3)	T_J, T_{stg}	−55 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted onto minimum pad size (0.412″ square) FR4 PCB, 1 oz cu.
2. Mounted onto 1″ square pad size (1.127″ square) FR4 PCB, 1 oz cu.
3. Normal pre−fault operating range. See thermal limit range conditions.

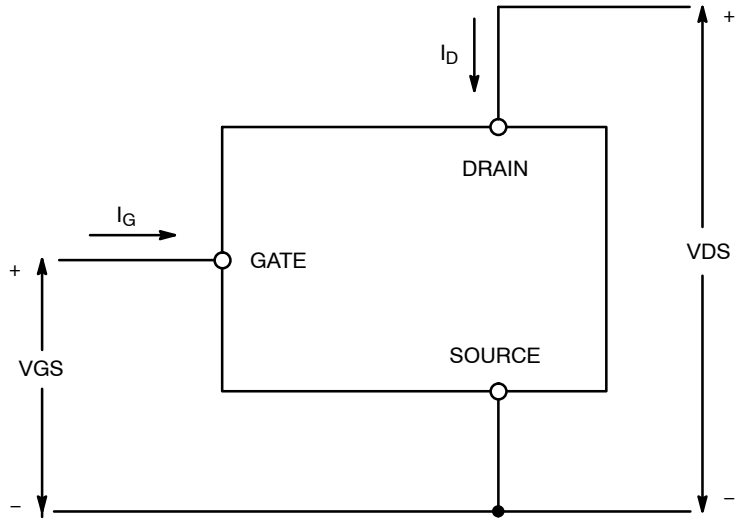


Figure 1. Voltage and Current Convention

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain−to−Source Clamped Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) (V_{GS} = 0 Vdc, I_D = 250 μAdc, T_J = −40°C to 150°C) (Note 4)	$V_{(BR)DSS}$	 42 40	 46 45	 51 51	 Vdc Vdc
Zero Gate Voltage Drain Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc, T_J = 150°C) (Note 4)	I_{DSS}	 − −	 0.6 2.5	 5.0 −	μAdc
Gate Input Current (V_{GS} = 5.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	−	50	125	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.2 mAdc) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	 1.0 −	 1.7 5.0	 2.2 −	 Vdc mV/°C
Static Drain−to−Source On−Resistance (Note 5) (V_{GS} = 10 Vdc, I_D = 3.0 Adc, T_J @ 25°C) (V_{GS} = 10 Vdc, I_D = 3.0 Adc, T_J @ 150°C) (Note 4)	$R_{DS(on)}$	 − −	 53 95	 68 123	mΩ
Static Drain−to−Source On−Resistance (Note 5) (V_{GS} = 5.0 Vdc, I_D = 3.0 Adc, T_J @ 25°C) (V_{GS} = 5.0 Vdc, I_D = 3.0 Adc, T_J @ 150°C) (Note 4)	$R_{DS(on)}$	 − −	 63 105	 76 135	mΩ
Source−Drain Forward On Voltage (I_S = 7.0 A, V_{GS} = 0 V)	V_{SD}	−	0.95	1.1	V

SWITCHING CHARACTERISTICS (Note 4)

Turn−ON Time (10% V_{IN} to 90% I_D)	V_{IN} = 0 V to 5 V, V_{DD} = 25 V I_D = 1.0 A, Ext R_G = 2.5 Ω	t_{ON}		44		μs
Turn−OFF Time (90% V_{IN} to 10% I_D)		t_{OFF}		84		
Turn−ON Time (10% V_{IN} to 90% I_D)	V_{IN} = 0 V to 10 V, V_{DD} = 25 V, I_D = 1.0 A, Ext R_G = 2.5 Ω	t_{ON}		15		
Turn−OFF Time (90% V_{IN} to 10% I_D)		t_{OFF}		116		
Slew−Rate ON (20% V_{DS} to 50% V_{DS})	V_{in} = 0 to 10 V, V_{DD} = 12 V, R_L = 4.7 Ω	$-dV_{DS}/dt_{ON}$		2.43		V/μs
Slew−Rate OFF (80% V_{DS} to 50% V_{DS})		dV_{DS}/dt_{OFF}		0.83		

SELF PROTECTION CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 6)

Current Limit	V_{GS} = 5.0 V, V_{DS} = 10 V V_{GS} = 5.0 V, T_J = 150°C (Note 4)	I_{LIM}	10 5.0	15 10	20 15	Adc
Current Limit	V_{GS} = 10 V, V_{DS} = 10 V V_{GS} = 10 V, T_J = 150°C (Note 4)	I_{LIM}	12 8.0	17 13	22 18	Adc
Temperature Limit (Turn−off)	V_{GS} = 5.0 Vdc	$T_{LIM(off)}$	150	175	200	°C
Thermal Hysteresis	V_{GS} = 5.0 Vdc	$\Delta T_{LIM(on)}$	−	15	−	°C
Temperature Limit (Turn−off)	V_{GS} = 10 Vdc	$T_{LIM(off)}$	150	165	185	°C
Thermal Hysteresis	V_{GS} = 10 Vdc	$\Delta T_{LIM(on)}$	−	15	−	°C

GATE INPUT AND FAULT DIAGNOSTICS CHARACTERISTICS (Note 4)

Device ON Gate Input Current	V_{GS} = 5 V I_D = 1.0 A	I_{GON}		50		μA
	V_{GS} = 10 V I_D = 1.0 A			400		
Current Limit Gate Input Current	V_{GS} = 5 V, V_{DS} = 10 V	I_{GCL}		0.1		mA
	V_{GS} = 10 V, V_{DS} = 10 V			0.6		
Thermal Limit Fault Gate Input Current	V_{GS} = 5 V, V_{DS} = 10 V	I_{GTL}		0.45		mA
	V_{GS} = 10 V, V_{DS} = 10 V			1.5		

ESD ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Electro−Static Discharge Capability	Human Body Model (HBM)	ESD	4000	−	−	V
Electro−Static Discharge Capability	Machine Model (MM)	ESD	400	−	−	V

4. Not subject to production testing.
5. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
6. Fault conditions are viewed as beyond the normal operating range of the part.

TYPICAL PERFORMANCE CURVES

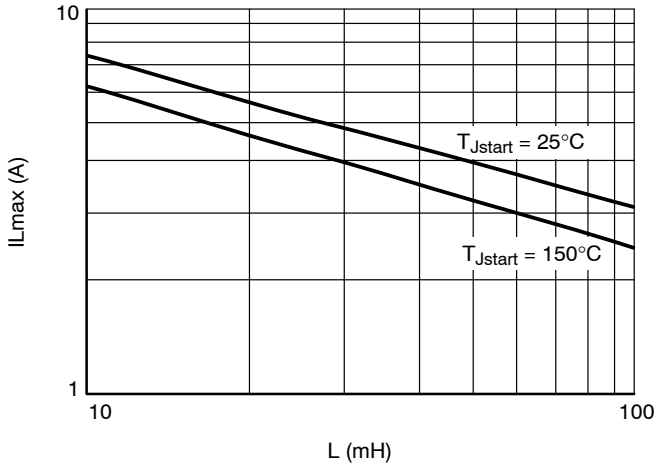


Figure 2. Single Pulse Maximum Switch−off Current vs. Load Inductance

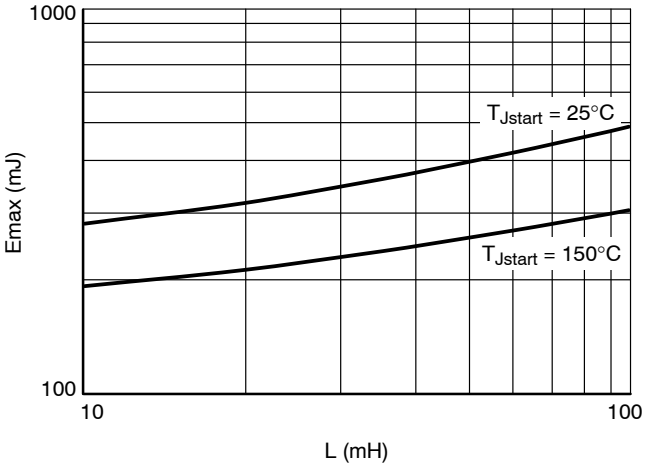


Figure 3. Single−Pulse Maximum Switching Energy vs. Load Inductance

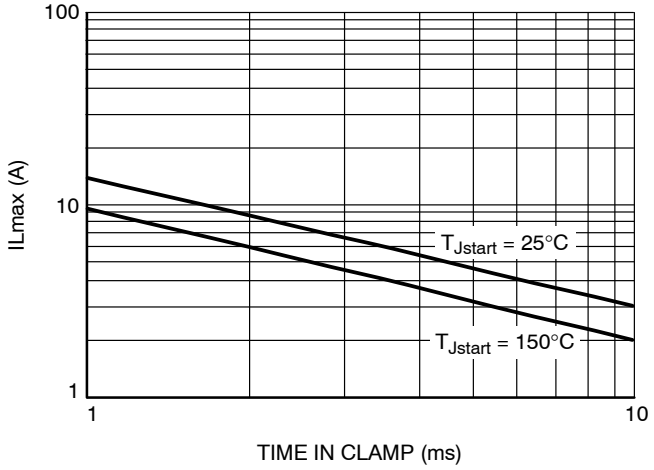


Figure 4. Single Pulse Maximum Inductive Switch−off Current vs. Time in Clamp

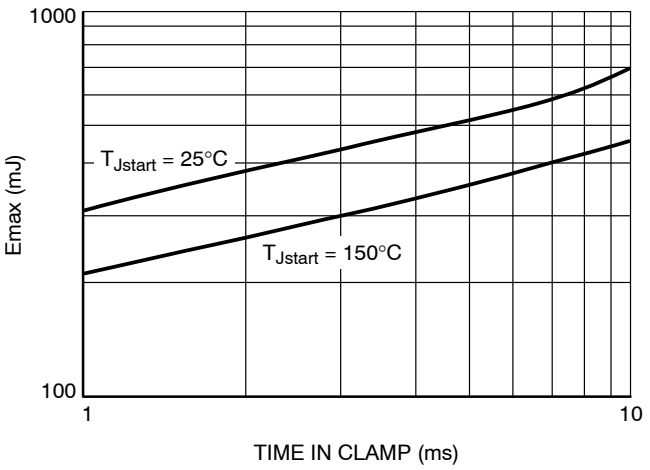


Figure 5. Single−Pulse Maximum Inductive Switching Energy vs. Time in Clamp

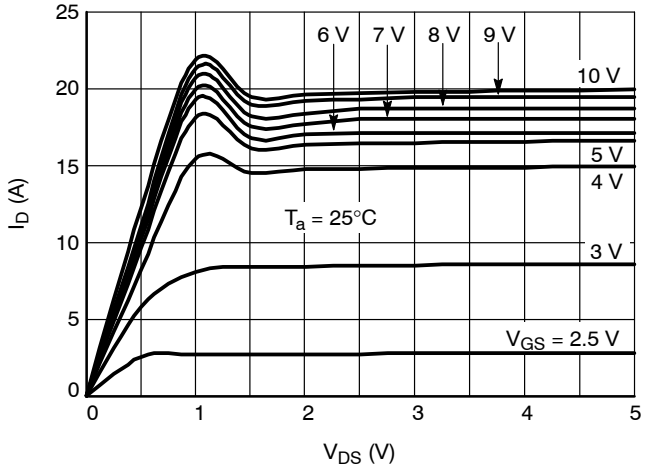


Figure 6. On−state Output Characteristics

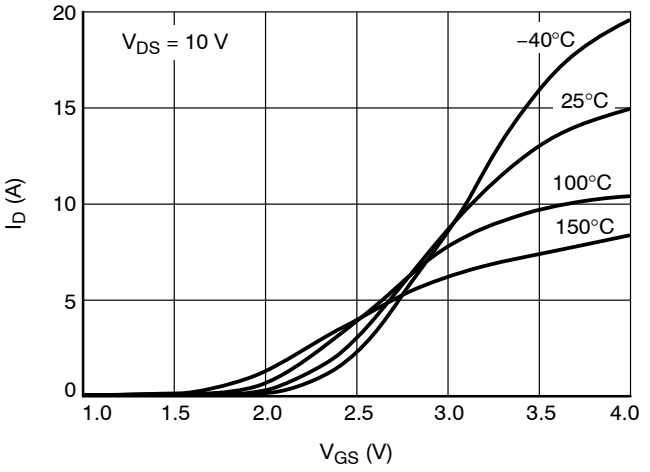


Figure 7. Transfer Characteristics

TYPICAL PERFORMANCE CURVES

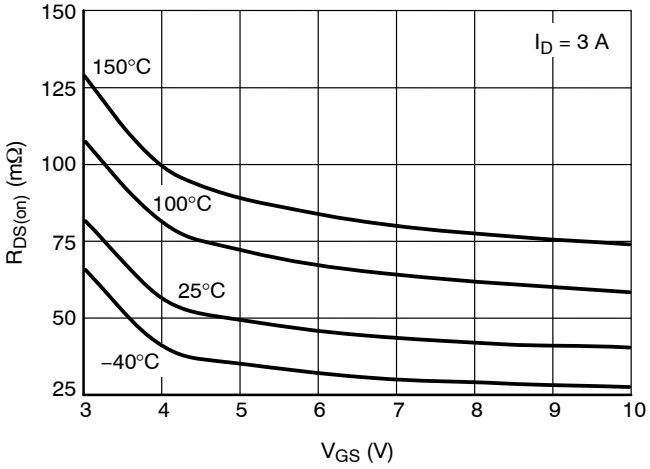


Figure 8. $R_{DS(on)}$ vs. Gate−Source Voltage

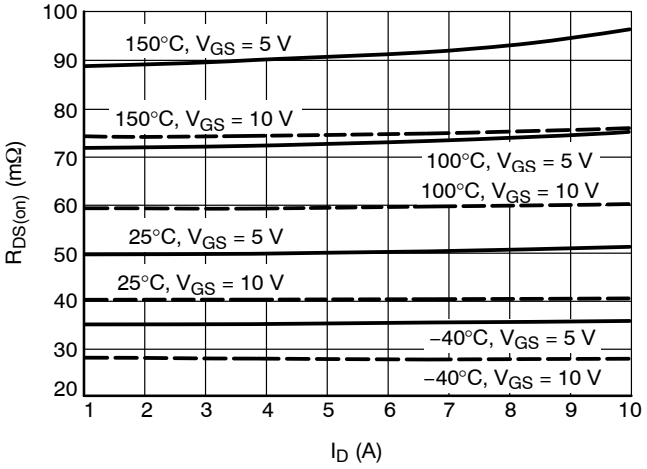


Figure 9. $R_{DS(on)}$ vs. Drain Current

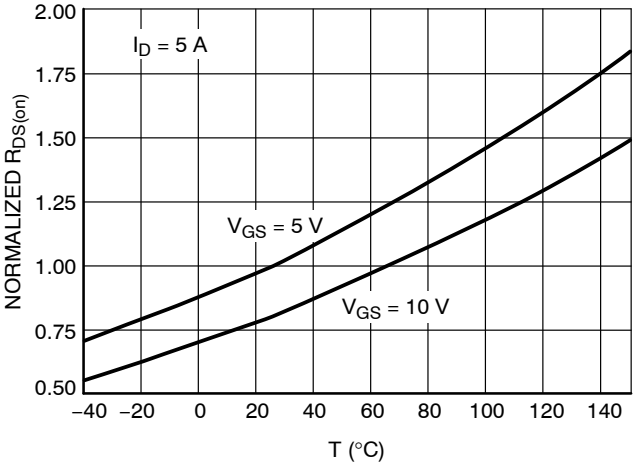


Figure 10. Normalized $R_{DS(on)}$ vs. Temperature

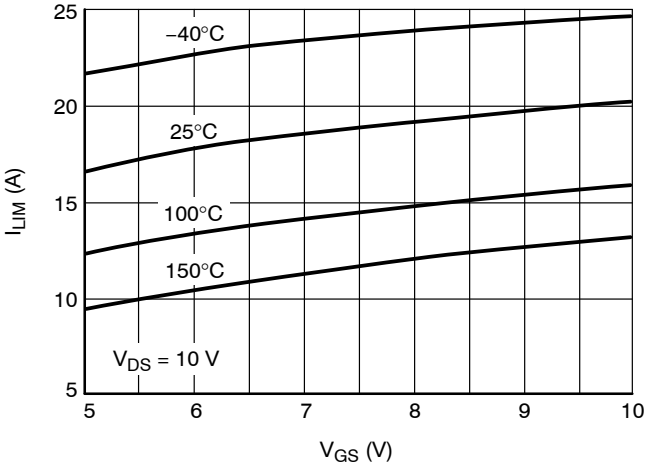


Figure 11. Current Limit vs. Gate−Source Voltage

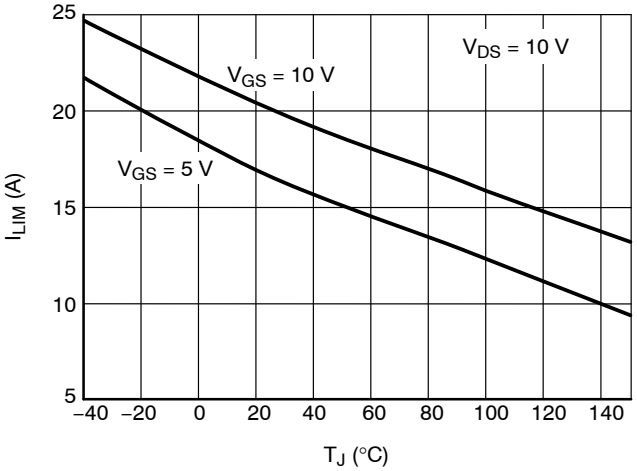


Figure 12. Current Limit vs. Junction Temperature

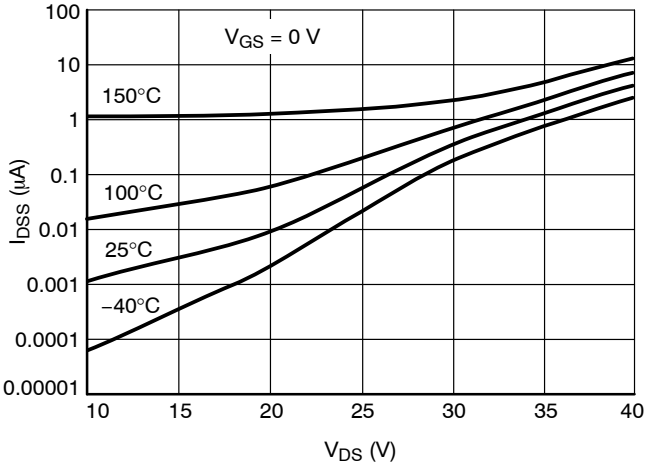


Figure 13. Drain−to−Source Leakage Current

TYPICAL PERFORMANCE CURVES

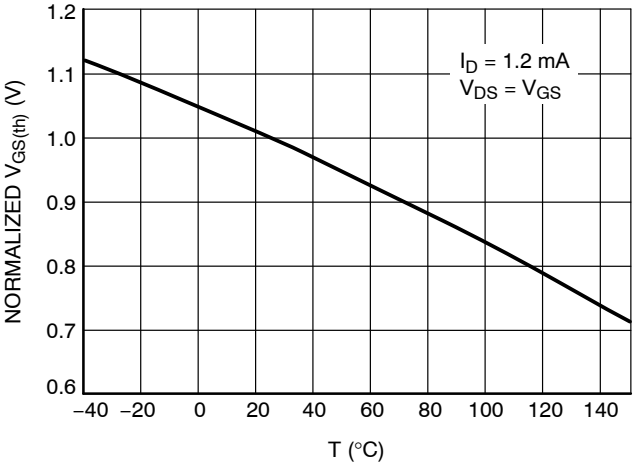


Figure 14. Normalized Threshold Voltage vs. Temperature

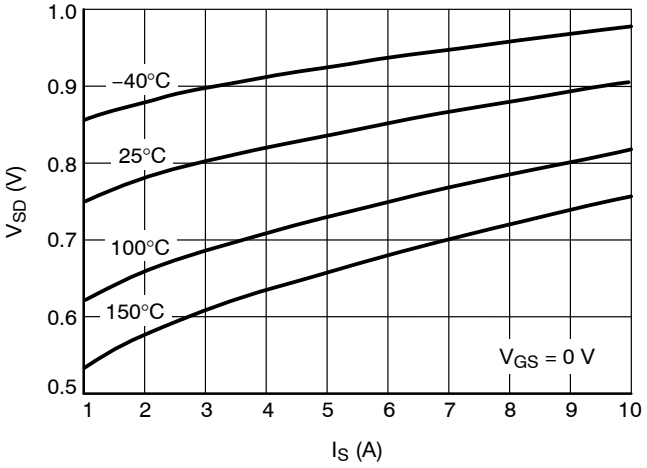


Figure 15. Source−Drain Diode Forward Characteristics

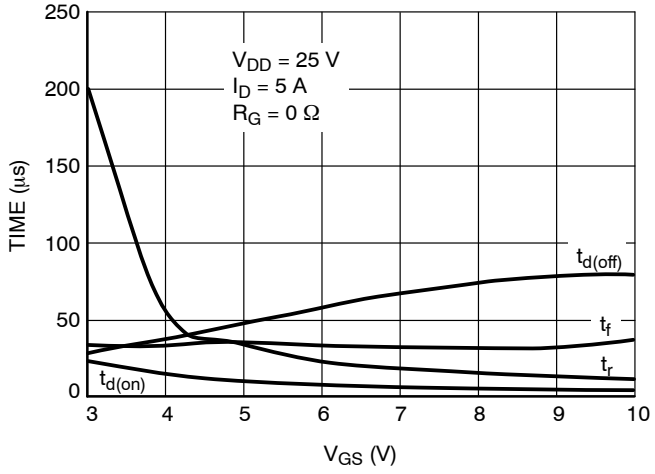


Figure 16. Resistive Load Switching Time vs. Gate−Source Voltage

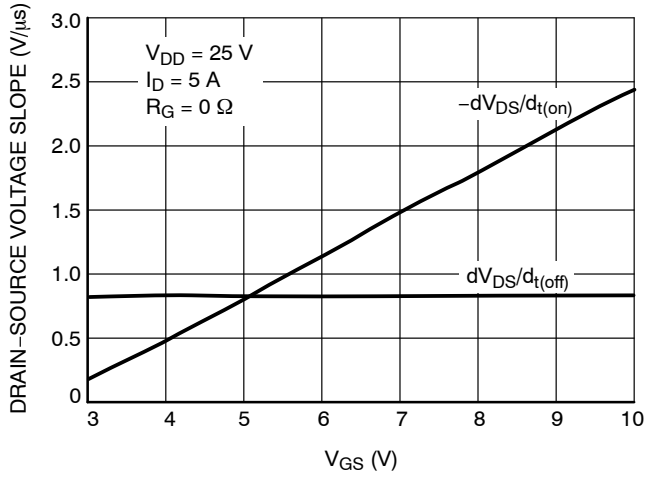


Figure 17. Resistive Load Switching Drain−Source Voltage Slope vs. Gate−Source Voltage

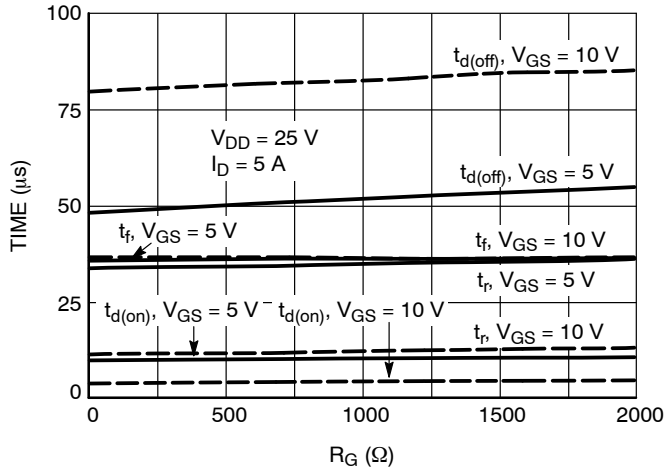


Figure 18. Resistive Load Switching Time vs. Gate Resistance

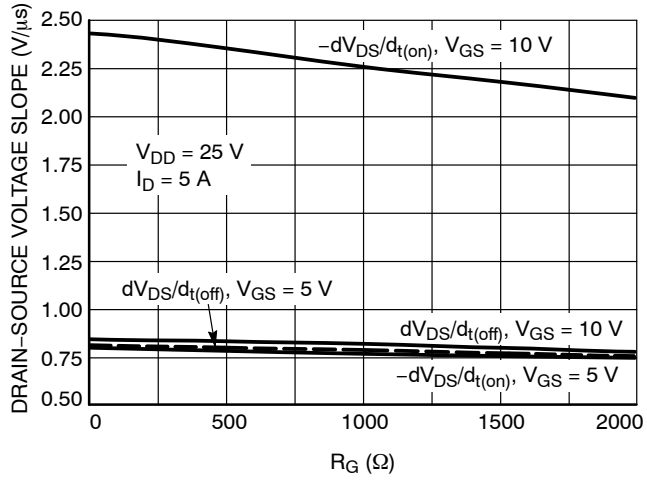


Figure 19. Drain−Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance

TYPICAL PERFORMANCE CURVES

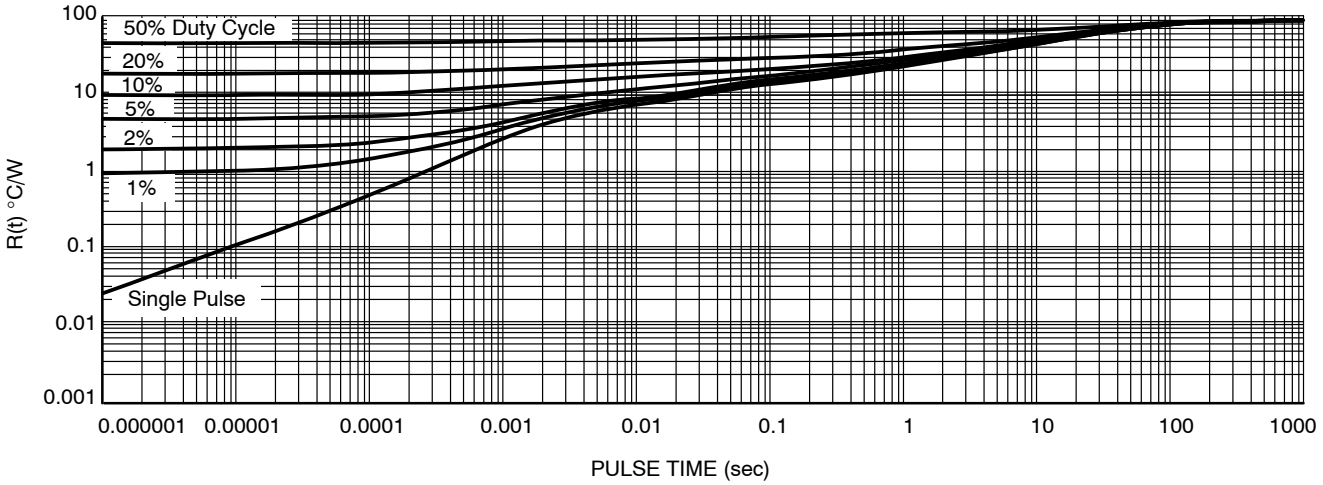


Figure 20. Transient Thermal Resistance

TEST CIRCUITS AND WAVEFORMS

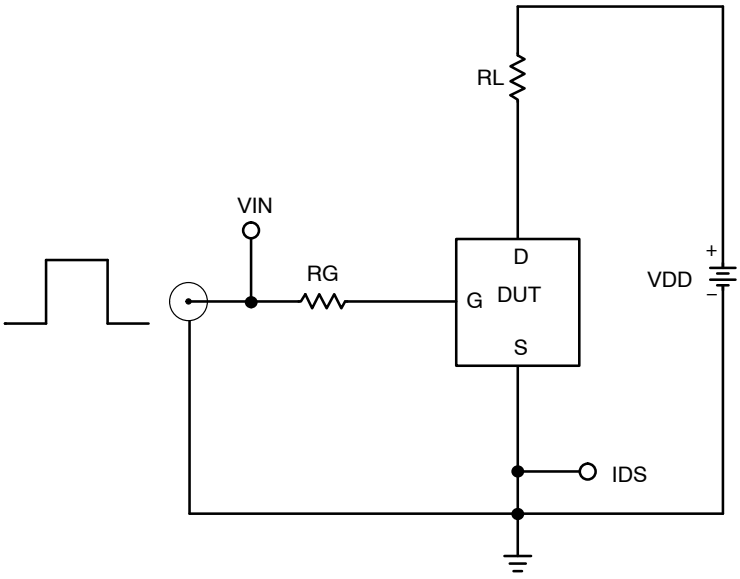


Figure 21. Resistive Load Switching Test Circuit

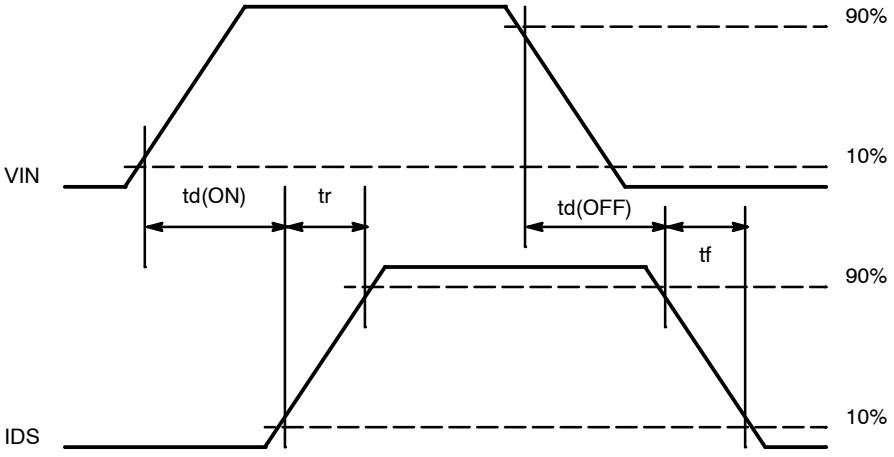


Figure 22. Resistive Load Switching Waveforms

TEST CIRCUITS AND WAVEFORMS

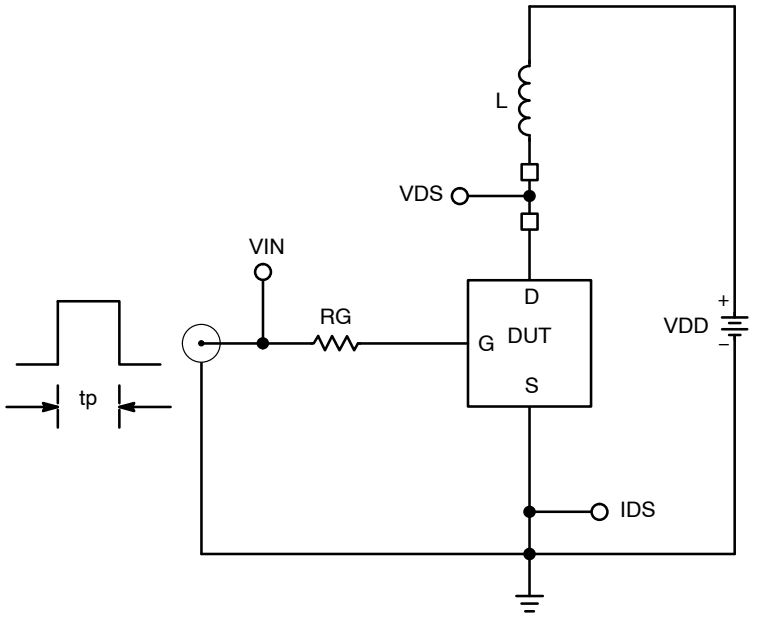


Figure 23. Inductive Load Switching Test Circuit

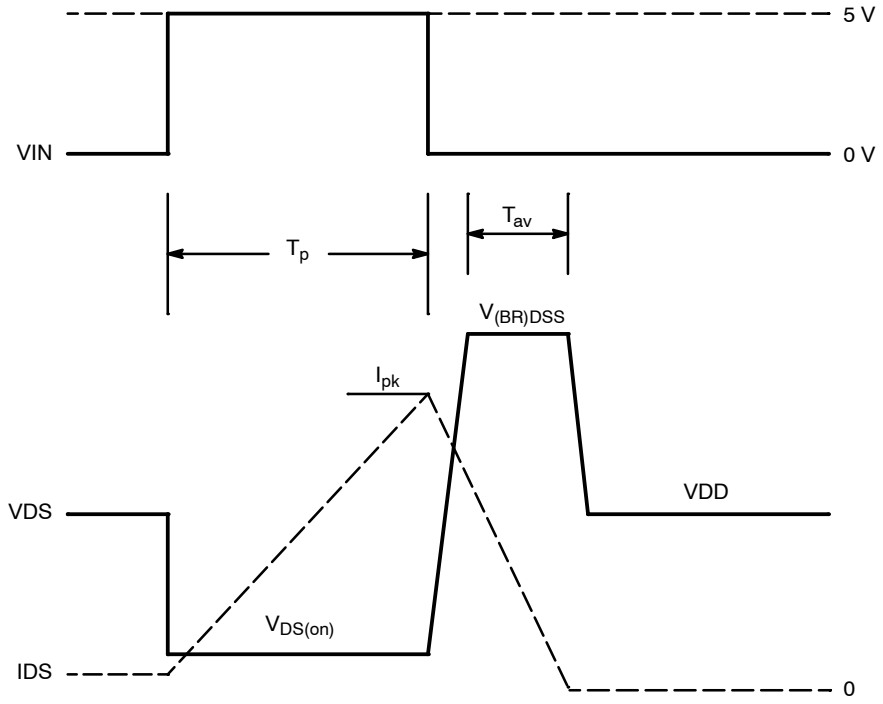


Figure 24. Inductive Load Switching Waveforms

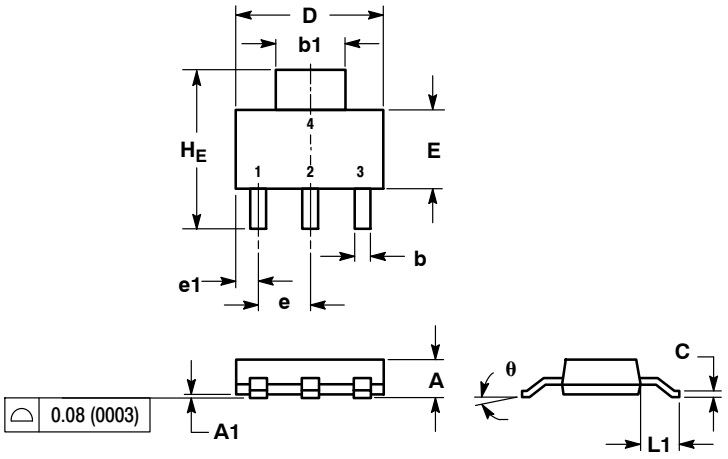
ORDERING INFORMATION

Device	Package	Shipping†
NCV8403	SOT−223 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SOT−223 (TO−261)
CASE 318E−04
ISSUE M

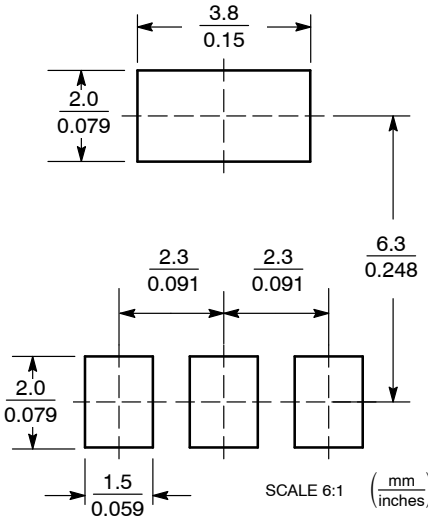


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	–	10°	0°	–	10°

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

HDPlus is a trademark of Semiconductor Components Industries, LLC (SCILLC)

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative