

P-Channel Enhancement Mode MOSFET

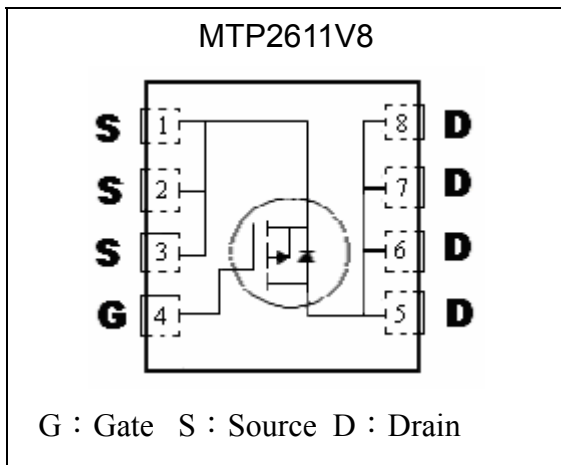
MTP2611V8

BV_{DSS}	-20V
I_D	-45A
$R_{DS(on)}@V_{GS}=-4.5V, I_D=-15.3A$	8.8mΩ (typ)
$R_{DS(on)}@V_{GS}=-2.5V, I_D=-13.1A$	12.8mΩ (typ)

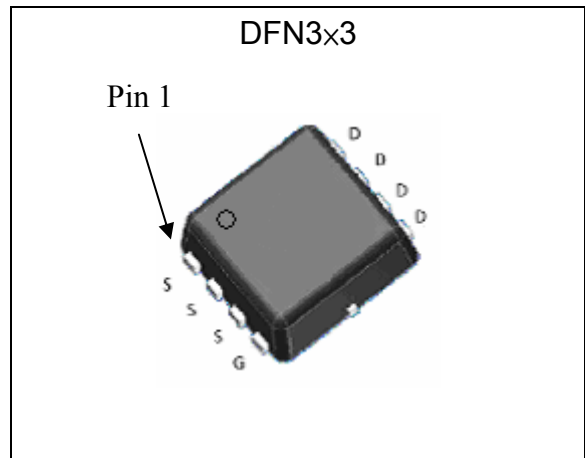
Features

- Simple drive requirement
- Low on-resistance
- Fast switching speed
- Pb-free lead plating and halogen-free package

Equivalent Circuit

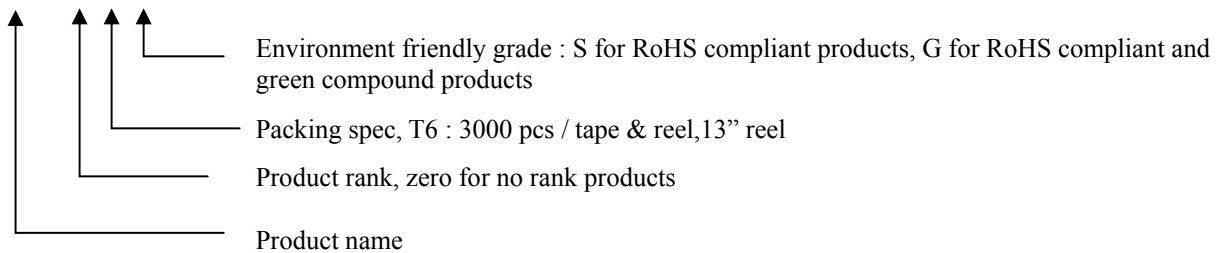


Outline



Ordering Information

Device	Package	Shipping
MTP2611V8-0-T6-G	DFN3x3 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel





Absolute Maximum Ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Drain-Source Voltage		V _{DS}	-20	V
Gate-Source Voltage		V _{GS}	±12	
Continuous Drain Current @ T _C =25°C, V _{GS} =-4.5V		I _D	-45	A
Continuous Drain Current @ T _C =100°C, V _{GS} =-4.5V			-28	
Continuous Drain Current @ T _A =25°C, V _{GS} =-4.5V			-12	
Continuous Drain Current @ T _A =70°C, V _{GS} =-4.5V			-9.6	
Pulsed Drain Current		I _{DM}	-90 *1	
Total Power Dissipation	T _C =25°C	P _D	31	W
	T _C =100°C		12	
	T _A =25°C		2.5 *3	
	T _A =70°C		1.6 *3	
Operating Junction and Storage Temperature Range		T _j , T _{stg}	-55~+150	°C

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R _{th,j-c}	4	°C/W
Thermal Resistance, Junction-to-ambient, max	R _{th,j-a}	50 *3	°C/W

- Note : 1. Pulse width limited by maximum junction temperature
 2. Duty cycle ≤ 1%
 3. Surface mounted on 1 in² copper pad of FR-4 board, t ≤ 10s ; 125°C/W when mounted on minimum copper pad.

Electrical Characteristics (T_j=25°C, unless otherwise specified)

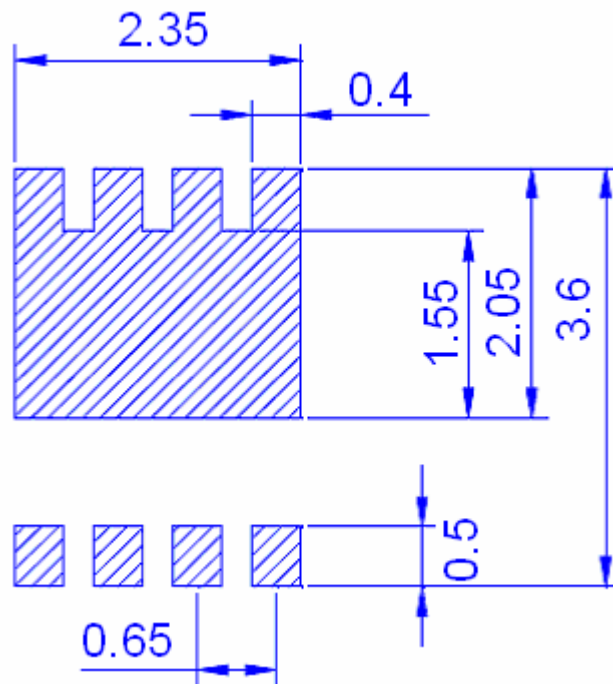
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	-20	-	-	V	V _{GS} =0, I _D =-250μA
V _{GS(th)}	-0.4	-0.62	-1.5		V _{DS} =V _{GS} , I _D =-250μA
I _{GSS}	-	-	±100	nA	V _{GS} =±12V, V _{DS} =0
I _{DSS}	-	-	-1	μA	V _{DS} =-16V, V _{GS} =0
I _{DSS}	-	-	-25		V _{DS} =-16V, V _{GS} =0, T _j =125°C
R _{DS(ON)} *1	-	8.8	11	mΩ	V _{GS} =-4.5V, I _D =-15.3A
	-	12.8	17		V _{GS} =-2.5V I _D =-13.1A
G _{FS} *1	-	22	-	S	V _{DS} =-10V, I _D =-10A
Dynamic					
C _{iss}	-	4107	-	pF	V _{DS} =-10V, V _{GS} =0, f=1MHz
C _{oss}	-	415	-		
C _{rss}	-	368	-		
t _{d(ON)} *1, 2	-	42	-	ns	V _{DS} =-10V, I _D =-1A, V _{GS} =-4.5V, R _G =6Ω
t _r *1, 2	-	23	-		
t _{d(OFF)} *1, 2	-	136	-		
t _f *1, 2	-	74	-		

Electrical Characteristics(Cont.) (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Qg *1,2	-	44	-	nC	V _{DS} =-10V, I _D =-12A, V _{GS} =-4.5V
Qgs *1,2	-	8.9	-		
Qgd *1,2	-	11	-		
Source-Drain Diode					
V _{SD} *1	-	-0.67	-1	V	I _S =-1.5A, V _{GS} =0V
trr	-	80	-	ns	I _F =-12A, dI _F /dt=100A/μs
Qrr	-	65	-	nC	

Note : *1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
 *2.Independent of operating temperature
 *3.Pulse width limited by maximum junction temperature.

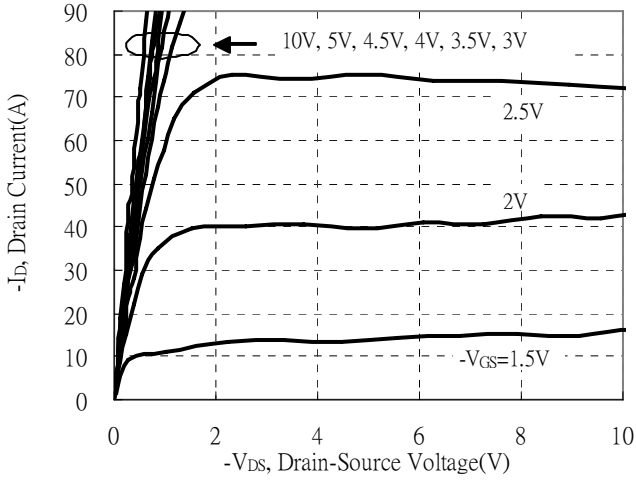
Recommended Soldering Footprint



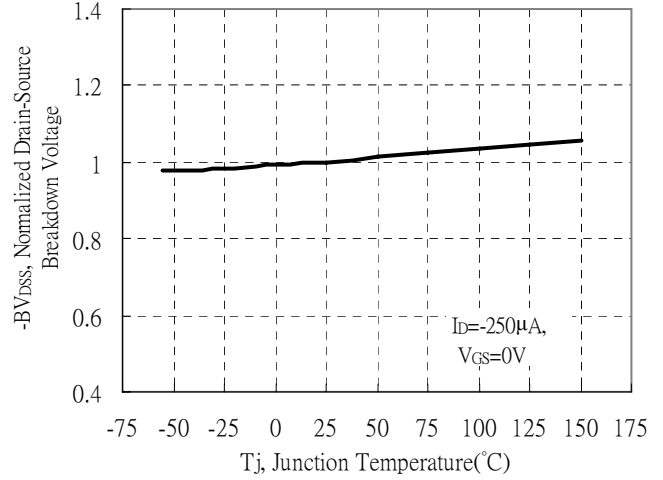
unit : mm

Typical Characteristics

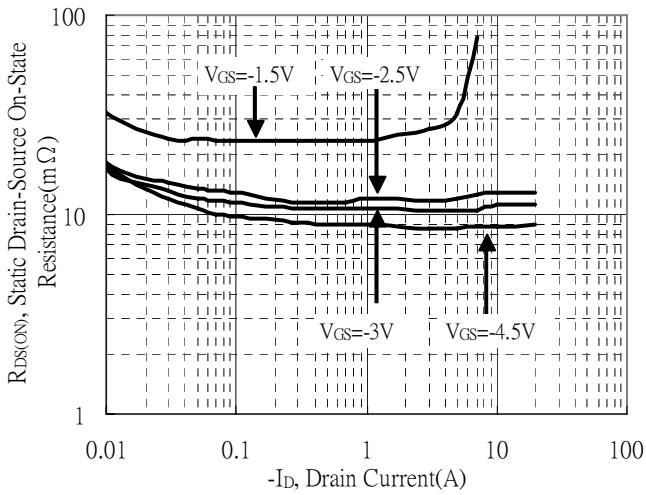
Typical Output Characteristics



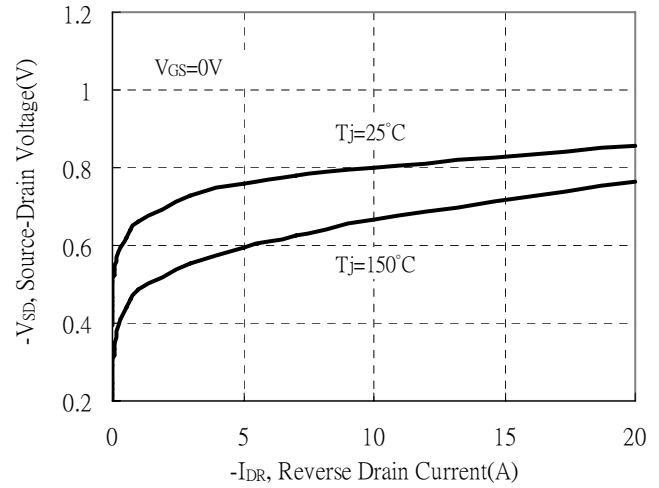
Breakdown Voltage vs Ambient Temperature



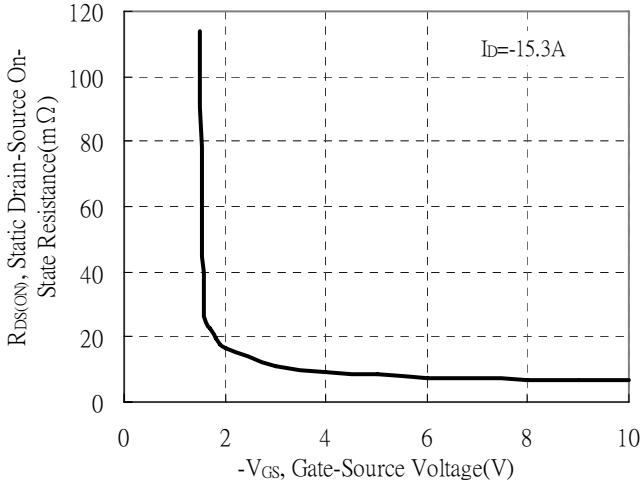
Static Drain-Source On-State resistance vs Drain Current



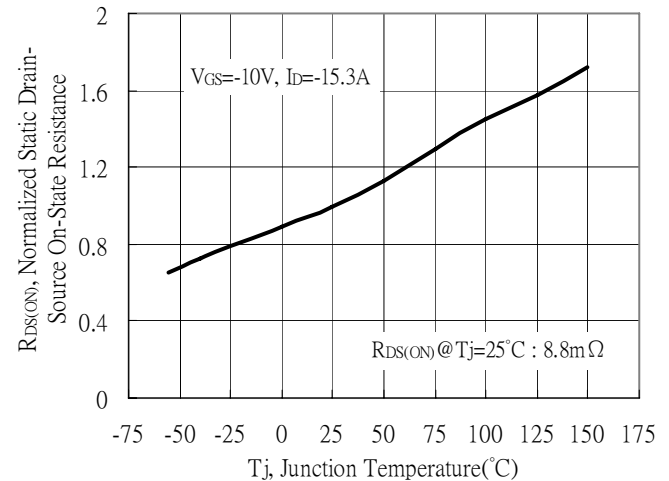
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

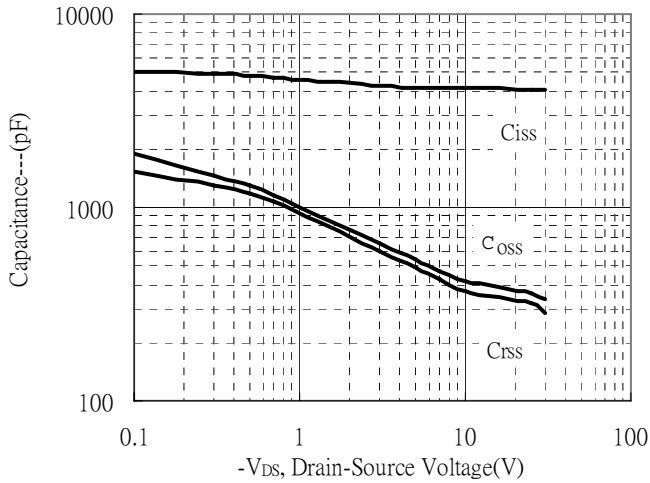


Drain-Source On-State Resistance vs Junction Temperature

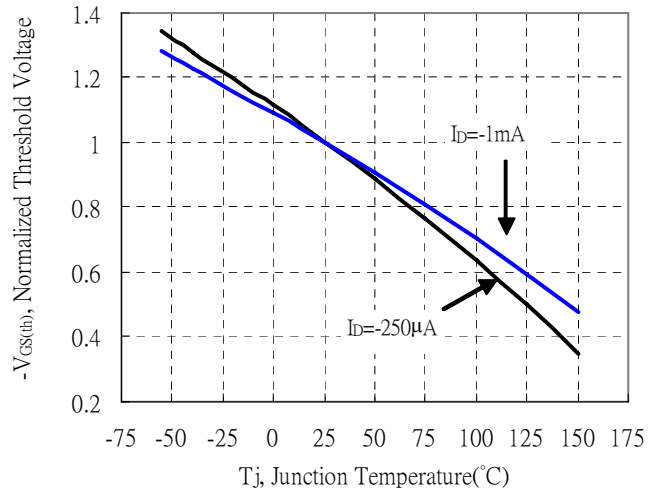


Typical Characteristics(Cont.)

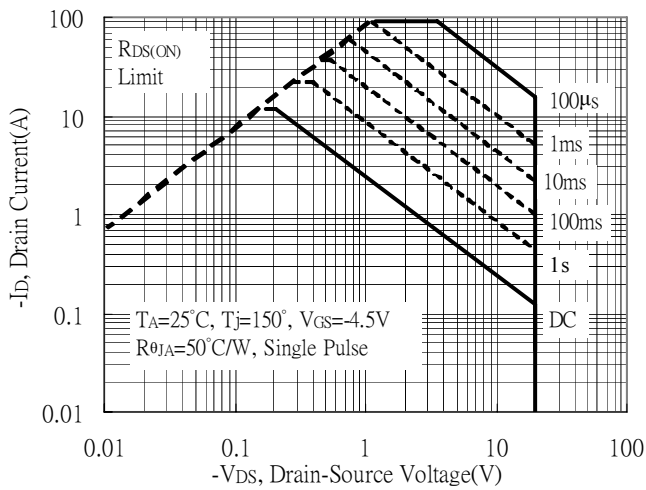
Capacitance vs Drain-to-Source Voltage



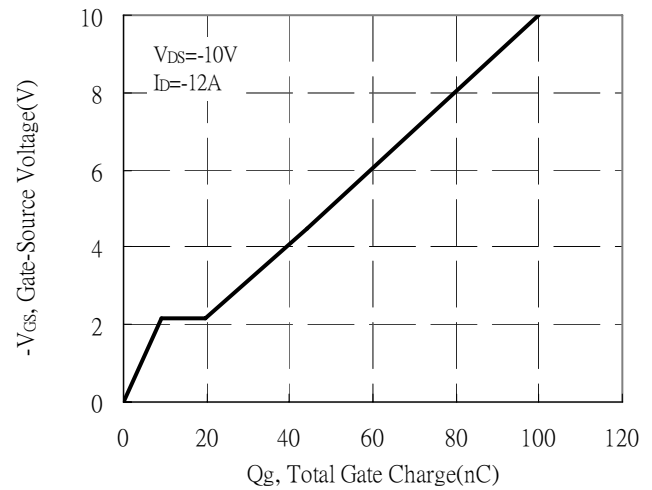
Threshold Voltage vs Junction Temperature



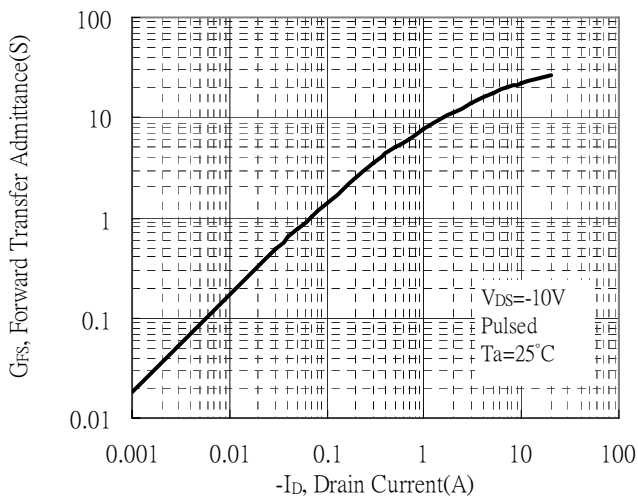
Maximum Safe Operating Area



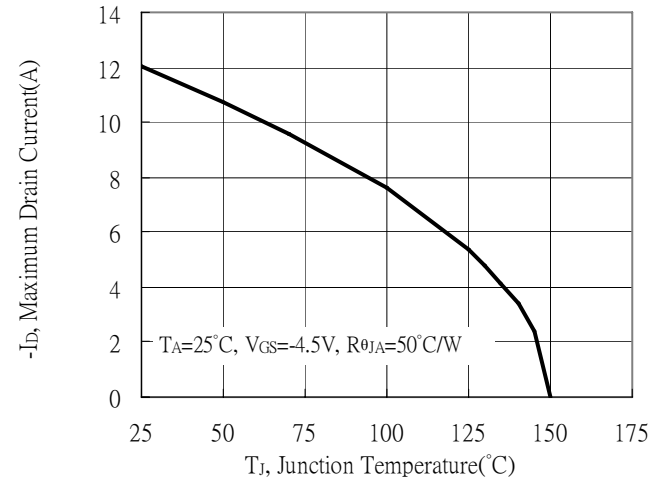
Gate Charge Characteristics



Forward Transfer Admittance vs Drain Current



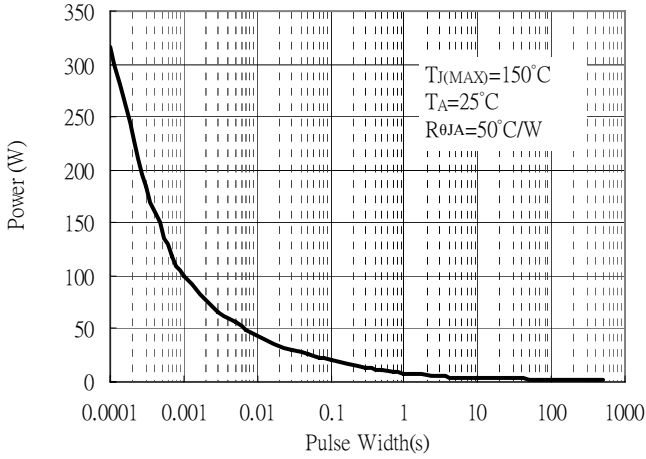
Maximum Drain Current vs Junction Temperature



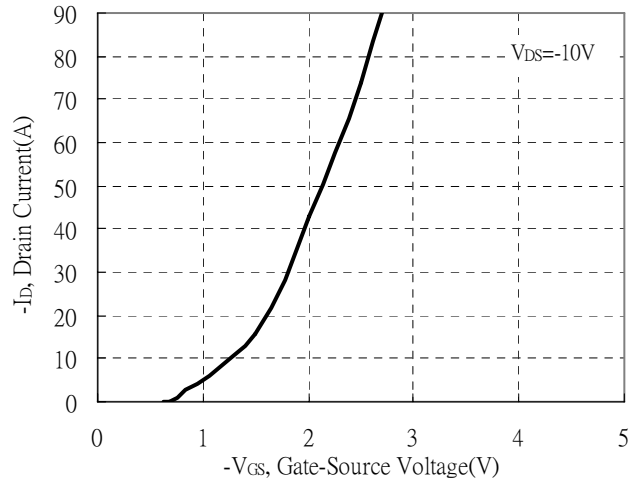


Typical Characteristics(Cont.)

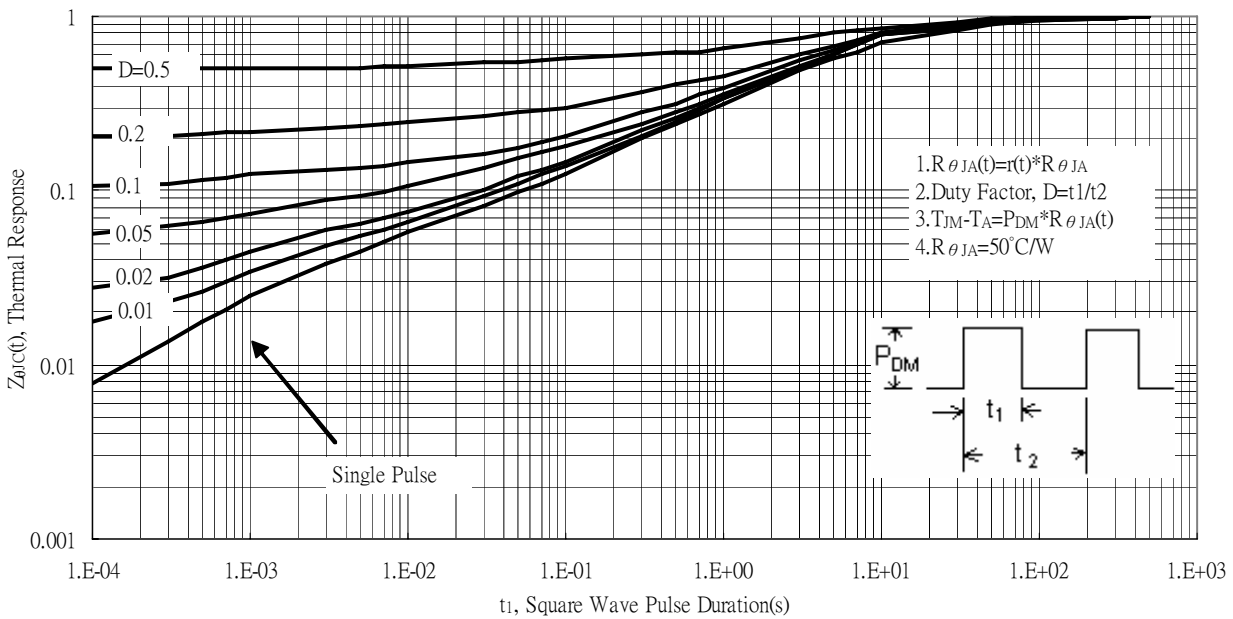
Single Pulse Power Rating, Junction to Ambient
 (Note on page 2)



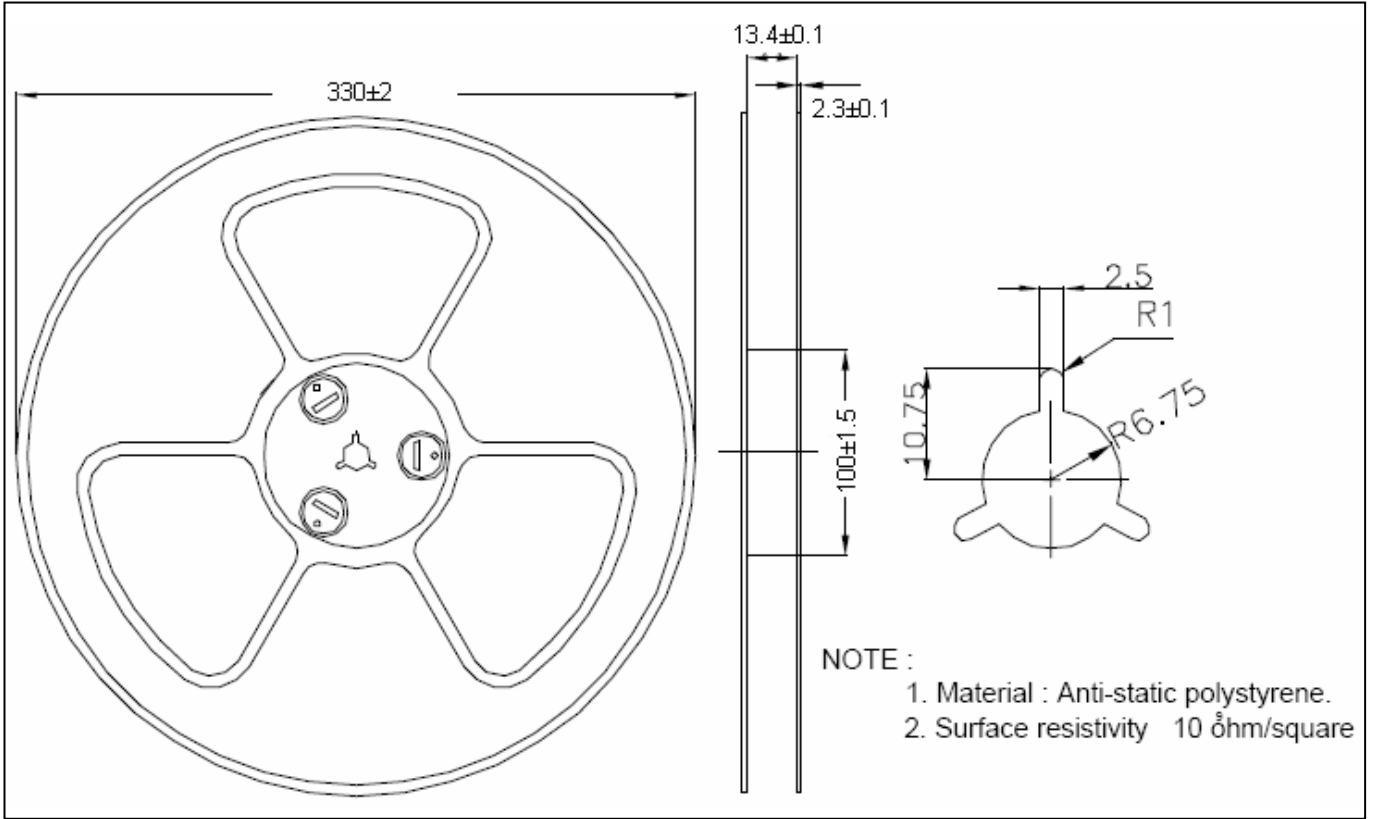
Typical Transfer Characteristics



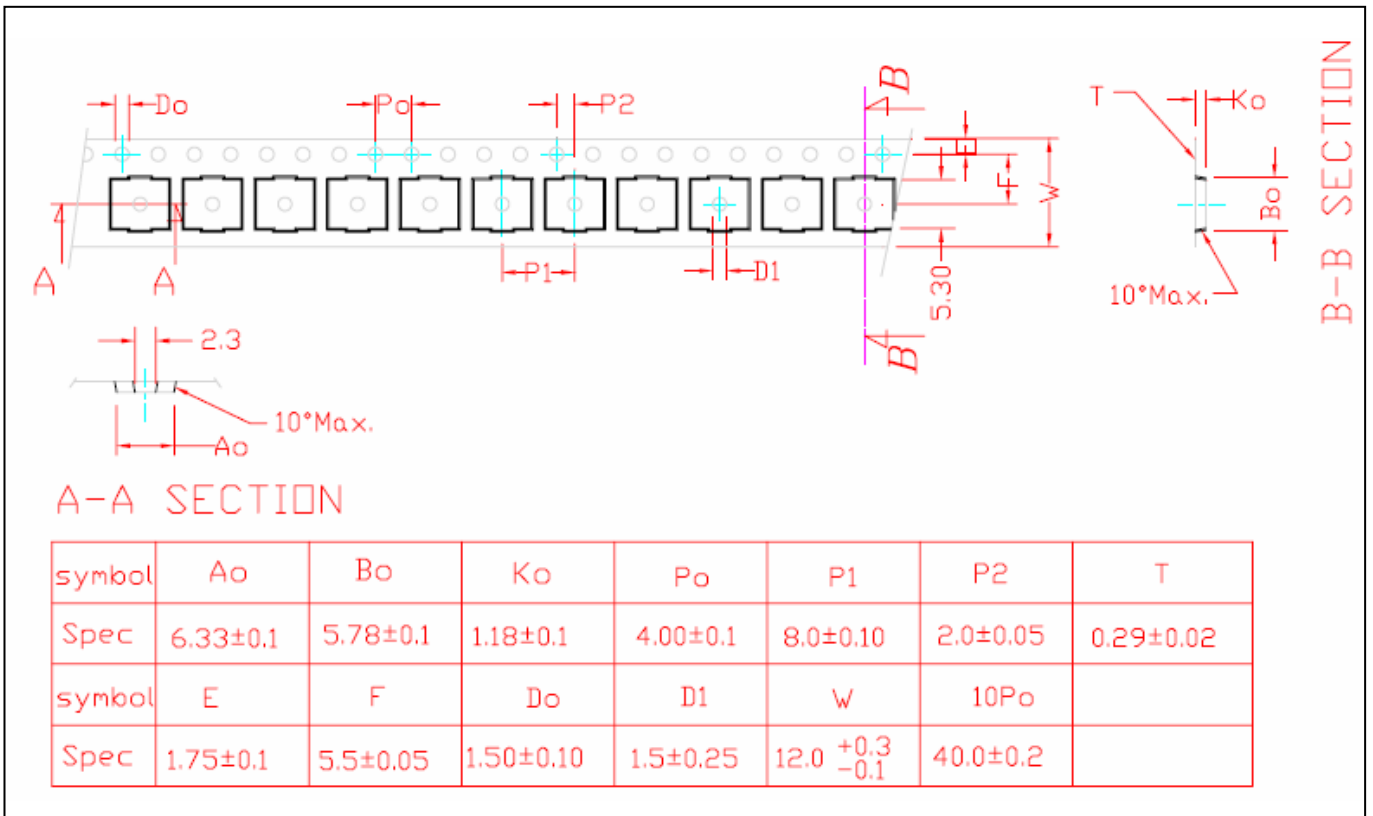
Transient Thermal Response Curves



Reel Dimension



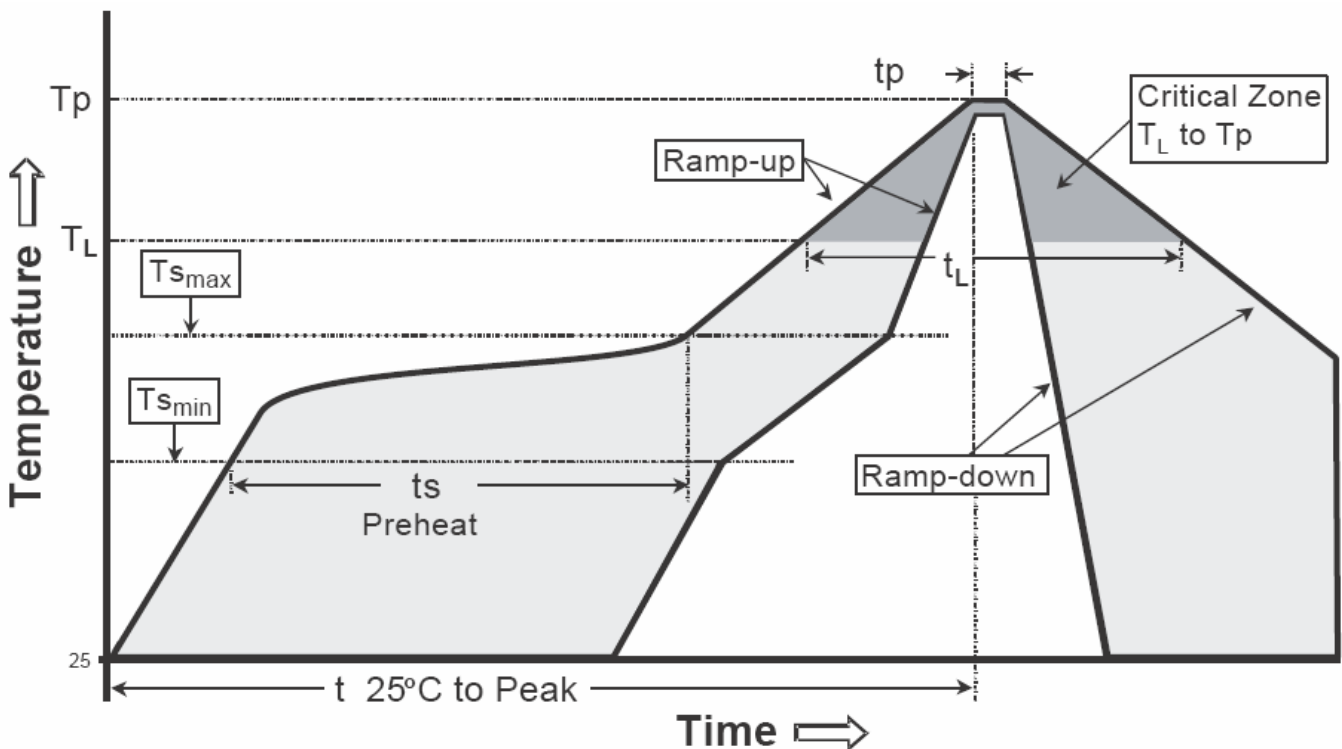
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

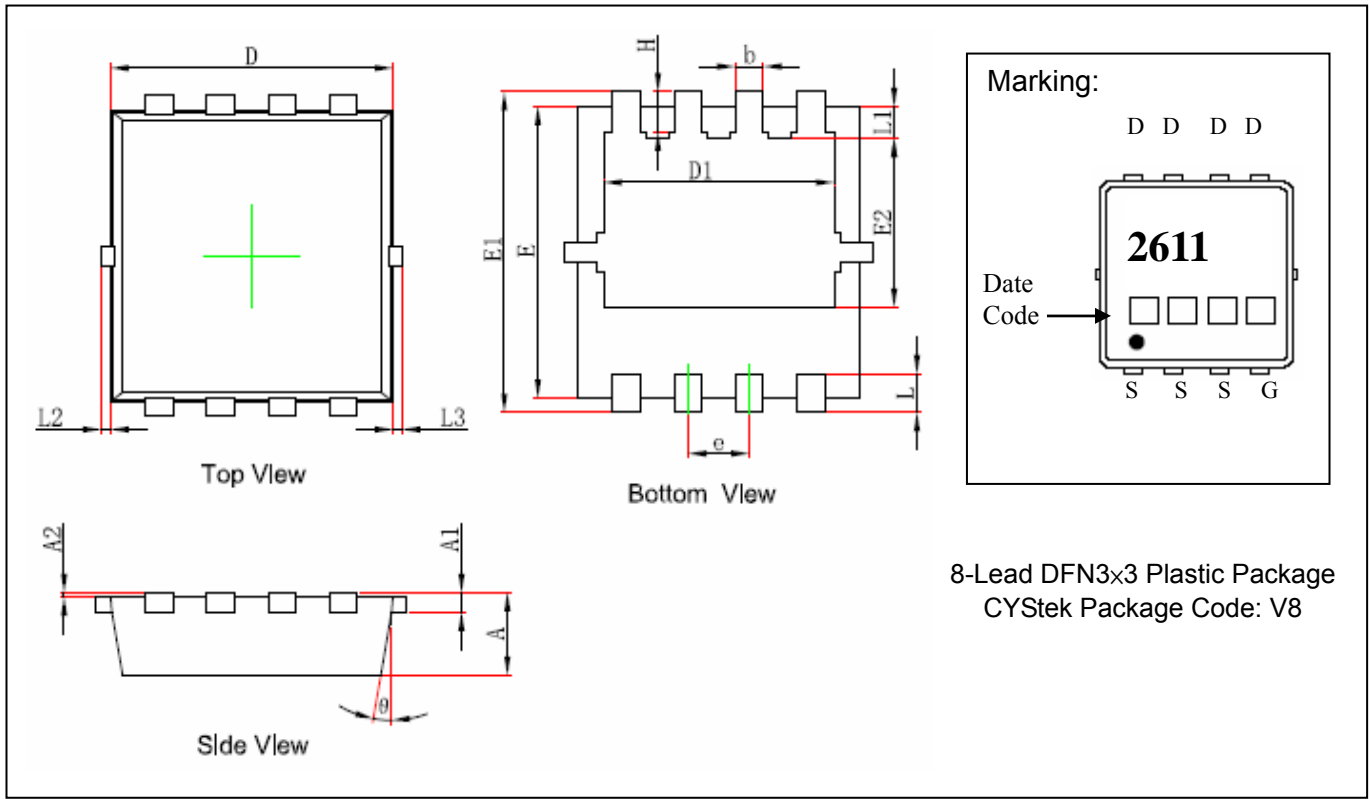
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

DFN3x3 Dimension



*: Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.605	0.850	0.026	0.033	b	0.200	0.400	0.008	0.016
A1	0.152	REF	0.006	REF	e	0.550	0.750	0.022	0.030
A2	0.000	0.050	0.000	0.002	L	0.300	0.500	0.012	0.020
D	2.900	3.100	0.114	0.122	L1	0.180	0.480	0.007	0.019
D1	2.300	2.600	0.091	0.102	L2	0.000	0.100	0.000	0.004
E	2.900	3.100	0.114	0.122	L3	0.000	0.100	0.000	0.004
E1	3.150	3.450	0.124	0.136	H	0.315	0.515	0.012	0.020
E2	1.535	1.935	0.060	0.076	θ	9°	13°	9°	13°

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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