MOTOROLA

MC14066B
See Page 6-5

MC14069UB

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX INVERTER

HEX INVERTER

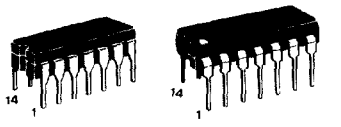
The MC14069UB hex inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4069UB
- Meets JEDEC UB Specifications

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C



L SUFFIX
CERAMIC PACKAGE
CASE 632

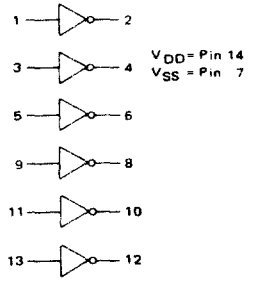
P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

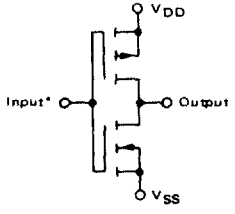
A Series: −55°C to +125°C
MC14XXXUBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXUBCP (Plastic Package)
MC14XXXUBCL (Ceramic Package)

LOGIC DIAGRAM



CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



*Double diode protection on all inputs not shown.

PIN ASSIGNMENT

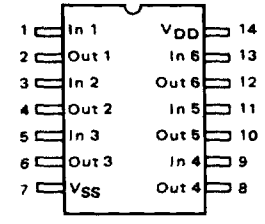
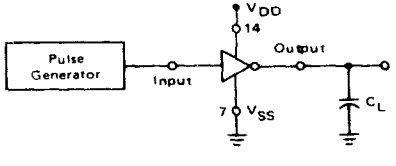
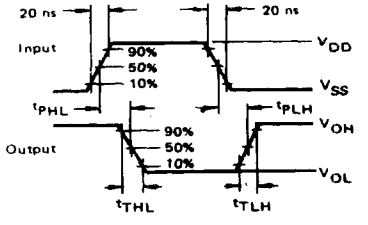


FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level $V_{in} = 0$	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 Vdc)		5.0	—	1.0	—	2.25	1.0	—	1.0	
(V_O = 9.0 Vdc)		10	—	2.0	—	4.50	2.0	—	2.0	
(V_O = 13.5 Vdc)		15	—	2.5	—	6.75	2.5	—	2.5	
"1" Level	V_{IH}									
(V_O = 0.5 Vdc)		5.0	4.0	—	4.0	2.75	—	4.0	—	Vdc
(V_O = 1.0 Vdc)		10	8.0	—	8.0	5.50	—	8.0	—	
(V_O = 1.5 Vdc)		15	12.5	—	12.5	8.25	—	12.5	—	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V_{OH} = 9.5 Vdc)		10	-1.6	—	-1.3	-2.25	—	-0.9	—	
(V_{OH} = 13.5 Vdc)		15	-4.2	—	-3.4	-8.8	—	-2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	—	-2.1	-4.2	—	-1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	—	-0.44	-0.88	—	-0.36	—	
(V_{OH} = 9.5 Vdc)		10	-1.3	—	-1.1	-2.25	—	-0.9	—	
(V_{OH} = 13.5 Vdc)		15	-3.6	—	-3.0	-8.8	—	-2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	—	0.44	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	—	1.1	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	3.6	—	3.0	8.8	—	2.4	—	
Input Current (AL Device)	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	—	±0.3	—	±0.00001	±0.3	—	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	—	0.25	—	0.0005	0.25	—	7.5	µAdc
		10	—	0.50	—	0.0010	0.50	—	15	
		15	—	1.00	—	0.0015	1.00	—	30	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	—	1.0	—	0.0005	1.0	—	7.5	µAdc
		10	—	2.0	—	0.0010	2.0	—	15	
		15	—	4.0	—	0.0015	4.0	—	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate) (C_L = 50 pF)	I_T	5.0	$I_T = (0.3\ \mu A/kHz)\ f + I_{DD}/6$							µAdc
		10	$I_T = (0.6\ \mu A/kHz)\ f + I_{DD}/6$							
		15	$I_T = (0.9\ \mu A/kHz)\ f + I_{DD}/6$							
Output Rise and Fall Times** (C_L = 50 pF)	t_{TLH}, t_{THL}									ns
t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 33 ns		5.0	—	—	—	100	200	—	—	
t_{TLH}, t_{THL} = (0.60 ns/pF) C_L + 20 ns		10	—	—	—	50	100	—	—	
t_{TLH}, t_{THL} = (0.40 ns/pF) C_L + 20 ns		15	—	—	—	40	80	—	—	
Propagation Delay Times** (C_L = 50 pF)	t_{PLH}, t_{PHL}									ns
t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 20 ns		5.0	—	—	—	65	125	—	—	
t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 22 ns		10	—	—	—	40	75	—	—	
t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 17 ns		15	—	—	—	30	55	—	—	

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = $(V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.002.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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