A/D Flash USB 8-Bit MCU with SPI

HT66FB540/HT66FB550/HT66FB560

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Table of Contents

Features **8**
CPU Features 8
Peripheral Features 8
General Description **9**
Selection Table **10**
Block Diagram **10**
Pin Assignment **11**
Pin Description **14**
Absolute Maximum Ratings **23**
D.C. Characteristics **24**
A.C. Characteristics **26**
LVD & LVR Electrical Characteristics **27**
ADC Electrical Characteristics **28**
Comparator Electrical Characteristics **28**
Power on Reset (AC+DC) Electrical Characteristics **28**
System Architecture **29**
Clocking and Pipelining 29
Program Counter 30
Stack 31
Arithmetic and Logic Unit – ALU 31
Flash Program Memory **32**
Structure 32
Special Vectors 32
Look-up Table 33
Table Program Example 33
Partial Lock 34
In System Programming – ISP 35
Flash Memory Read/Write Page Size 35
ISP Bootloader 37
Flash Program Memory Registers 37
In Application Programming – IAP 41
Enable Flash Write Control Procedure 41
Flash Memory Write and Read Procedures 43
In Circuit Programming – ICP 45
On-Chip Debug Support – OCDS 45

RAM Data Memory 46
Structure 46
Special Function Register Description 50
Indirect Addressing Registers – IAR0, IAR1 50
Memory Pointers – MP0, MP1 50
Bank Pointer – BP 51
Accumulator – ACC 52
Program Counter Low Register – PCL 52
Look-up Table Registers – TBLP, TBHP, TBLH 52
Status Register – STATUS 53
Oscillator 54
Oscillator Overview 54
System Clock Configurations 54
External Crystal Oscillator – HXT 55
Internal PLL Frequency Generator 56
Internal RC Oscillator – HIRC 58
External 32.768kHz Crystal Oscillator – LXT 58
LXT Oscillator Low Power Function 59
Internal 32kHz Oscillator – LIRC 59
Supplementary Internal Clocks 60
Operating Modes and System Clocks 60
System Clocks 60
System Operation Modes 61
Control Register 63
Fast Wake-up 64
Operating Mode Switching and Wake-up 65
NORMAL Mode to SLOW Mode Switching 65
SLOW Mode to NORMAL Mode Switching 67
Entering the SLEEP0 Mode 67
Entering the SLEEP1 Mode 67
Entering the IDLE0 Mode 68
Entering the IDLE1 Mode 68
Standby Current Considerations 68
Wake-up 69
Programming Considerations 69
Watchdog Timer 70
Watchdog Timer Clock Source 70
Watchdog Timer Control Register 70
Watchdog Timer Operation 71
WDT Enable/Disabled using the WDT Control Register 72

Reset and Initialisation 73
Reset Overview 73
Reset Functions 74
WDTC Register Software Reset 77
Reset Initial Conditions 78
Input/Output Ports 88
Pull-high Resistors 91
Port Wake-up 93
Port A Wake-up Polarity Control Register 94
I/O Port Control Registers 95
I/O Output Current Control Registers 97
I/O Output Slew Rate Control Registers 98
Port A Power Source Control Registers 100
I/O Pin Structures 101
Programming Considerations 102
Timer Modules – TM 103
Introduction 103
TM Operation 103
TM Clock Source 104
TM Interrupts 104
TM External Pins 104
TM Input/Output Pin Control Registers 105
Programming Considerations 109
Compact Type TM – CTM 110
Compact TM Operation 111
Compact Type TM Register Description 111
Compact Type TM Operating Modes 116
Compare Match Output Mode 116
Timer/Counter Mode 119
PWM Output Mode 119
Standard Type TM – STM 122
Standard TM Operation 122
Standard Type TM Register Description 122
Standard Type TM Operating Modes 130
Compare Output Mode 130
Timer/Counter Mode 133
PWM Output Mode 133
Single Pulse Mode 136
Capture Input Mode 138

Analog to Digital Converter 140
A/D Overview 140
A/D Converter Register Description 140
A/D Converter Data Registers – ADRL, ADRH 141
A/D Converter Control Registers – ADCR0, ADCR1, ACER0, ACER1 141
A/D Operation 147
A/D Input Pins 148
Summary of A/D Conversion Steps 148
Programming Considerations 149
A/D Transfer Function 149
A/D Programming Example 150

Comparators 152
Comparator Operation 152
Comparator Registers 152
Comparator Interrupt 152
Programming Considerations 153

Serial Interface Module – SIM 155
SPI Interface 155
SPI Interface Operation 155
SPI Registers 157
SPI Communication 160
SPI Bus Enable/Disable 162
SPI Operation 163
Error Detection 164
I^2C Interface 164
I^2C Interface Operation 165
I^2C Registers 165
I^2C Bus Communication 170
I^2C Bus Start Signal 171
Slave Address 171
I^2C Bus Read/Write Signal 171
I^2C Bus Slave Address Acknowledge Signal 171
I^2C Bus Data and Acknowledge Signal 172
I^2C Time Out function 173
I^2C Time Out operation 174

Serial Interface – SPIA 175
SPIA Interface Operation 175
SPIA Registers 176
SPIA Communication 179
SPIA Bus Enable/Disable 181
SPIA Operation 182
Error Detection 183

Peripheral Clock Output 184
Peripheral Clock Operation 184
Interrupts 185
Interrupt Registers 185
Interrupt Operation 192
External Interrupt 194
Comparator Interrupt 194
USB Interrupt 194
Multi-function Interrupt 195
A/D Converter Interrupt 195
Time Base Interrupts 195
Serial Interface Module Interrupts – SIM Interrupt 196
Serial Peripheral Interface Interrupt – SPIA Interrupt 197
LVD Interrupt 197
TM Interrupts 197
Interrupt Wake-up Function 197
Programming Considerations 198
Low Voltage Detector – LVD 199
LVD Register 199
LVD Operation 200
USB Interface 200
Power Plane 200
USB Suspend Wake-Up Remote Wake-Up 201
USB Interface Operation 202
USB Interface Registers 203
Configuration Options 224
Application Circuits 225
Instruction Set 226
Introduction 226
Instruction Timing 226
Moving and Transferring Data 226
Arithmetic Operations 226
Logical and Rotate Operation 227
Branches and Control Transfer 227
Bit Operations 227
Table Read Operations 227
Other Operations 227
Instruction Set Summary 228

Instruction Definition 230
Package Information 240
28-pin SSOP(150mil) Outline Dimensions 241
SAW Type 40-pin (6mm×6mm for 0.75mm) QFN Outline Dimensions 242
48-pin LQFP (7mm×7mm) Outline Dimensions 243
64-pin LQFP (7mm×7mm) Outline Dimensions 244

Features

CPU Features

- Operating voltage
  - V_{DD}(MCU):
    f_{SYS}=4MHz/6MHz: 2.2V~5.5V
    f_{SYS}=12MHz: 2.7V~5.5V
  - V_{DD} (USB mode):
    f_{SYS}=6MHz/12MHz: 3.3V~5.5V
    f_{SYS}=16MHz: 4.5V~5.5V
- Up to 0.25μs instruction cycle with 16MHz system clock at V_{DD}=5V
- Power down and wake-up functions to reduce power consumption
- Four oscillators
  - External Crystal – HXT
  - External 32.768kHz Crystal – LXT
  - Internal RC – HIRC
  - Internal 32kHz RC – LIRC
- Multi-mode operation: NORMAL, SLOW, IDLE and SLEEP
- All instructions executed in one or two instruction cycles
- Table read instructions
- 63 powerful instructions
- Up to 12-level subroutine nesting
- Bit manipulation instruction

Peripheral Features

- Flash Program Memory: 4K×16~16K×16
- RAM Data Memory: 512×8~1024×8
- USB 2.0 Full Speed compatible
- Up to 8 endpoints supported including endpoint 0
- All endpoints except endpoint 0 can support interrupt and bulk transfer
- All endpoints except endpoint 0 can be configured as 8, 16, 32, 64 bytes FIFO size
- Endpoint 0 support control transfer
- Endpoint 0 has 8 byte FIFO
- Support 3.3V LDO and internal UDP 1.5kΩ pull-up resistor
- Internal 12MHz RC OSC with 0.25% accuracy for all USB modes
- Watchdog Timer function
- Up to 45 bidirectional I/O lines
- Dual pin-shared external interrupts

- Multiple Timer Modules for time measurement, input capture, compare match output or PWM output or single pulse output function
  - 2 Compact type 10-bit Timer Module - CTM
  - 1 Standard type 10-bit Timer Module - STM
  - 1 Standard type 16-bit Timer Module - STM
- Serial Interface Modules with Dual SPI and I^2C interfaces
- Single Serial SPI Interface
- Dual Comparator functions
- Dual Time-Base functions for generation of fixed time interrupt signals
- Up to 16 channel 12-bit resolution A/D converter
- Low voltage reset function
- Low voltage detect function
- Flash program memory can be re-programmed up to 1,000,000 times
- Flash program memory data retention > 10 years
- Support In System Programing function - ISP
- Wide range of available package types
- Partial lock function

General Description

The HT66FB540, HT66FB550 and HT66FB560 are Flash Memory A/D with USB type 8-bit high performance RISC architecture microcontrollers, designed for applications that interface directly to analog signals and which require an USB interface. Offering users the convenience of Flash Memory multi-programming features, these devices also include a wide range of functions and features. Other memory includes an area of RAM Data Memory.

Analog features include a multi-channel 12-bit A/D converter and dual comparator functions. Multiple and extremely flexible Timer Modules provide timing, pulse generation and PWM generation functions. Communication with the outside world is catered for by including fully integrated SPI, I^2C and USB interface functions, three popular interfaces which provide designers with a means of easy communication with external peripheral hardware. Protective features such as an internal Watchdog Timer, Low Voltage Reset and Low Voltage Detector coupled with excellent noise immunity and ESD protection ensure that reliable operation is maintained in hostile electrical environments. The external interrupt can be triggered with falling edges or both falling and rising edges.

A full choice of four oscillator functions are provided including two fully integrated system oscillators which requires no external components for their implementation. The ability to operate and switch dynamically between a range of operating modes using different clock sources gives users the ability to optimize microcontroller operation and minimize power consumption.

The inclusion of flexible I/O programming features, Time-Base functions along with many other features ensure that these devices will find specific excellent use in a wide range of application possibilities such as sensor signal processing, motor driving, industrial control, consumer products, subsystem controllers, etc.

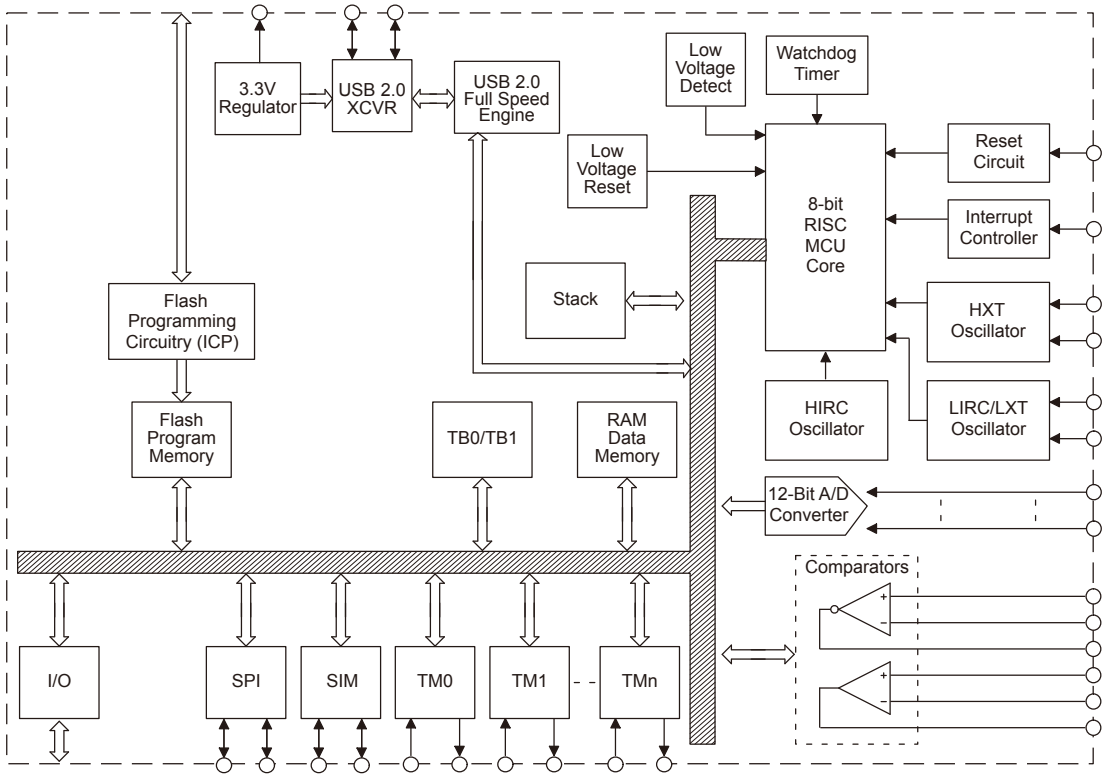
These devices are fully supported by the Holtek range of fully functional development and programming tools, providing a means for fast and efficient product development cycles.

Selection Table

Most features are common to all devices, the main feature distinguishing them are Program Memory capacity, I/O count, AD channels, stack capacity and package types. The following table summarises the main features of each device.

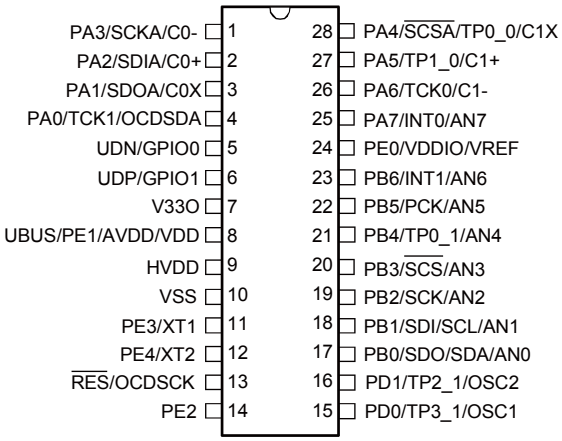
Part No.	V_{DD}	Program Memory	Data Memory	I/O	External Interrupt	A/D	Timer Module	SIM (SPI/I^2C)	SPI	Stack	Package
HT66FB540	2.2V~5.5V	4K×16	512×8	25	2	12-bit ×8	10-bit CTM×2, 10-bit STM×1, 16-bit STM×1	√	√	8	28SSOP 48LQFP
HT66FB550	2.2V~5.5V	8K×16	768×8	37	2	12-bit ×16	10-bit CTM×2, 10-bit STM×1, 16-bit STM×1	√	√	8	28SSOP 40QFN 48LQFP
HT66FB560	2.2V~5.5V	16K×16	1024×8	45	2	12-bit ×16	10-bit CTM×2, 10-bit STM×1, 16-bit STM×1	√	√	12	40QFN 48/64LQFP

Block Diagram

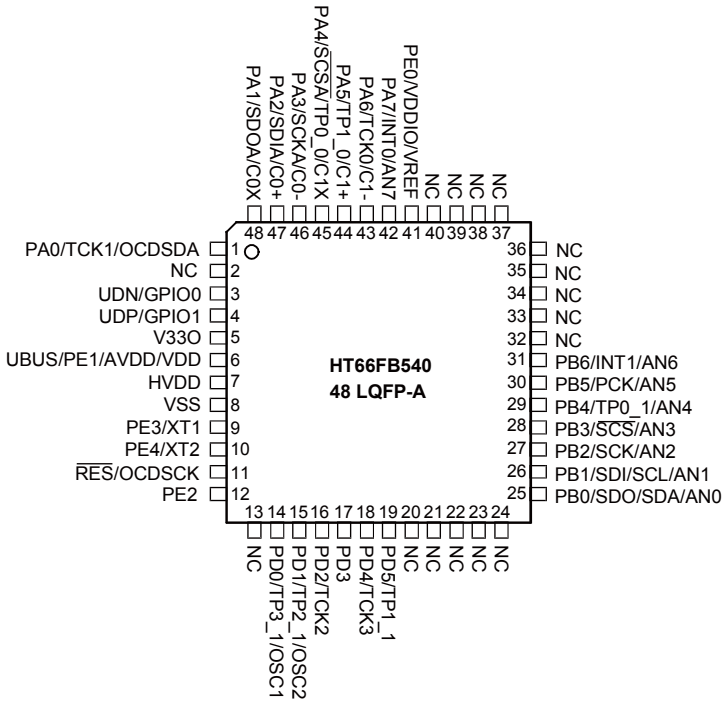


Pin Assignment

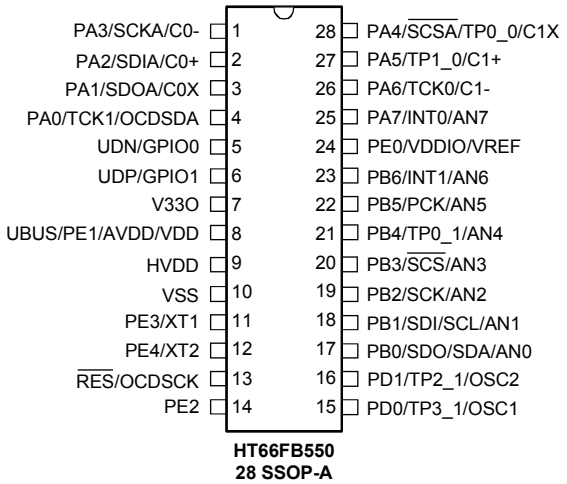
HT66FB540

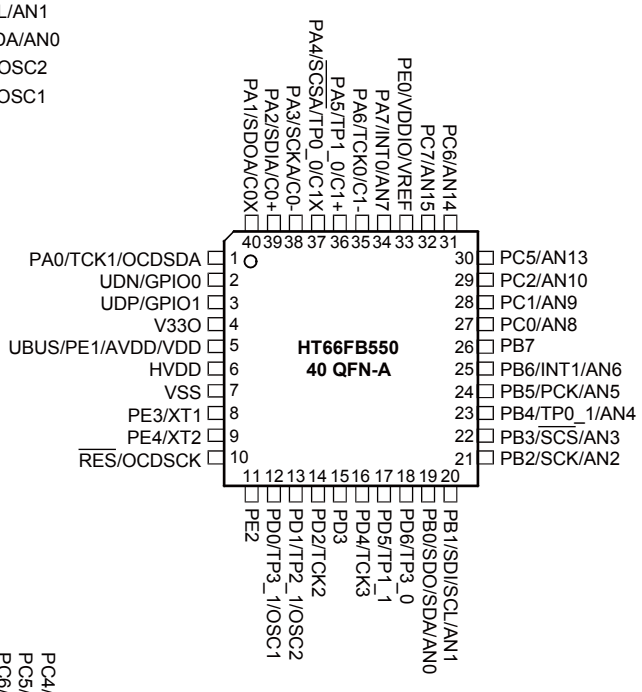


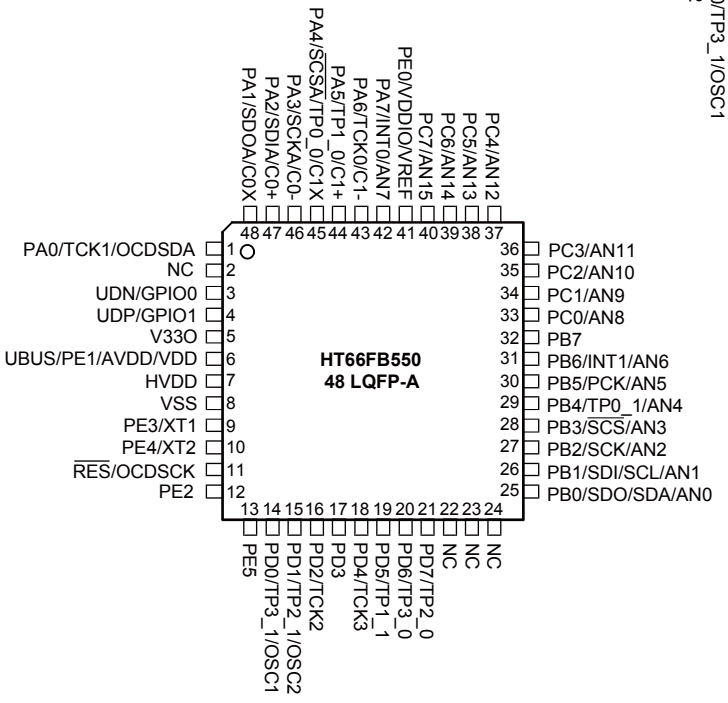
HT66FB540
28 SSOP-A



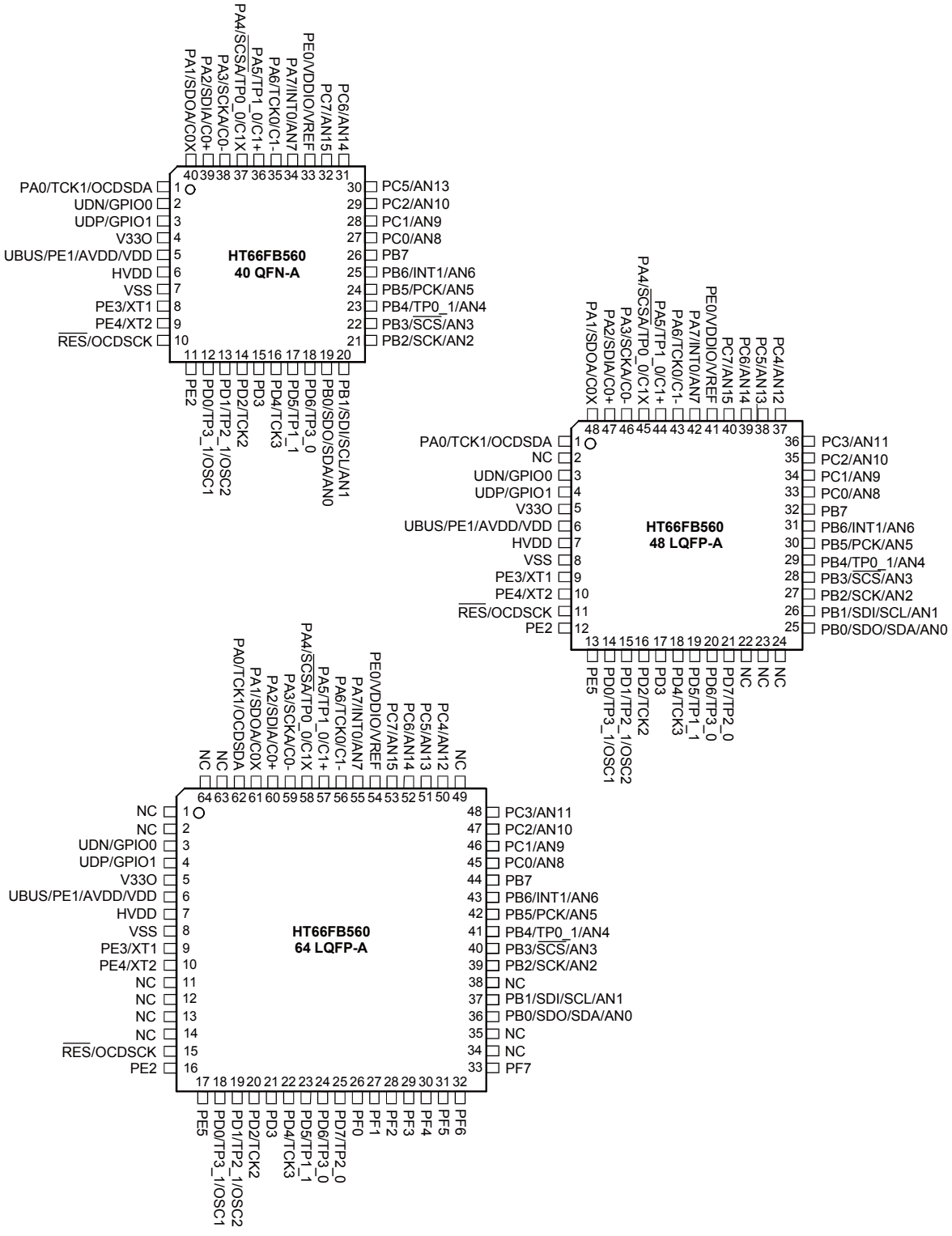
HT66FB550


PA3/SCKA/C0- 1
PA2/SDIA/C0+ 2
PA1/SDOA/C0X 3
PA0/TCK1/OCDSDA 4
UDN/GPIO0 5
UDP/GPIO1 6
V33O 7
UBUS/PE1/AVDD/VDD 8
HVDD 9
VSS 10
PE3/XT1 11
PE4/XT2 12
RES/OCDSCK 13
PE2 14
28 PA4/SCSA/TP0_0/C1X
27 PA5/TP1_0/C1+
26 PA6/TCK0/C1-
25 PA7/INT0/AN7
24 PE0/VDDIO/VREF
23 PB6/INT1/AN6
22 PB5/PCK/AN5
21 PB4/TP0_1/AN4
20 PB3/SCS/AN3
19 PB2/SCK/AN2
18 PB1/SDI/SCL/AN1
17 PB0/SDO/SDA/AN0
16 PD1/TP2_1/OSC2
15 PD0/TP3_1/OSC1
HT66FB550
28 SSOP-A


PA1/SDOA/C0X 40
PA2/SDIA/C0+ 39
PA3/SCKA/C0- 38
PA4/SCSA/TP0_0/C1X 37
PA5/TP1_0/C1+ 36
PA6/TCK0/C1- 35
PA7/INT0/AN7 34
PE0/VDDIO/VREF 33
PC7/AN15 32
PC6/AN14 31
PA0/TCK1/OCDSDA 1
UDN/GPIO0 2
UDP/GPIO1 3
V33O 4
UBUS/PE1/AVDD/VDD 5
HVDD 6
VSS 7
PE3/XT1 8
PE4/XT2 9
RES/OCDSCK 10
30 PC5/AN13
29 PC2/AN10
28 PC1/AN9
27 PC0/AN8
26 PB7
25 PB6/INT1/AN6
24 PB5/PCK/AN5
23 PB4/TP0_1/AN4
22 PB3/SCS/AN3
21 PB2/SCK/AN2
HT66FB550
40 QFN-A
11 PE2
12 PD0/TP3_1/OSC1
13 PD1/TP2_1/OSC2
14 PD2/TCK2
15 PD3
16 PD4/TCK3
17 PD5/TP1_1
18 PD6/TP3_0
19 PB0/SDO/SDA/AN0
20 PB1/SDI/SCL/AN1


PA1/SDOA/C0X 48
PA2/SDIA/C0+ 47
PA3/SCKA/C0- 46
PA4/SCSA/TP0_0/C1X 45
PA5/TP1_0/C1+ 44
PA6/TCK0/C1- 43
PA7/INT0/AN7 42
PE0/VDDIO/VREF 41
PC7/AN15 40
PC6/AN14 39
PC5/AN13 38
PC4/AN12 37
PA0/TCK1/OCDSDA 1
NC 2
UDN/GPIO0 3
UDP/GPIO1 4
V33O 5
UBUS/PE1/AVDD/VDD 6
HVDD 7
VSS 8
PE3/XT1 9
PE4/XT2 10
RES/OCDSCK 11
PE2 12
36 PC3/AN11
35 PC2/AN10
34 PC1/AN9
33 PC0/AN8
32 PB7
31 PB6/INT1/AN6
30 PB5/PCK/AN5
29 PB4/TP0_1/AN4
28 PB3/SCS/AN3
27 PB2/SCK/AN2
26 PB1/SDI/SCL/AN1
25 PB0/SDO/SDA/AN0
HT66FB550
48 LQFP-A
13 PE5
14 PD0/TP3_1/OSC1
15 PD1/TP2_1/OSC2
16 PD2/TCK2
17 PD3
18 PD4/TCK3
19 PD5/TP1_1
20 PD6/TP3_0
21 PD7/TP2_0
22 NC
23 NC
24 NC

HT66FB560


HT66FB560
40 QFN-A
PA0/TCK1/OCDSDA
UDN/GPIO0
UDP/GPIO1
V33O
UBUS/PE1/AVDD/VDD
HVDD
VSS
PE3/XT1
PE4/XT2
RES/OCDSCK
PA1/SDOA/C0X
PA2/SDIA/C0+
PA3/SCKA/C0-
PA4/SCSA/TP0_0/C1X
PA5/TP1_0/C1+
PA6/TCK0/C1-
PA7/INT0/AN7
PE0/VDDIO/VREF
PC7/AN15
PC6/AN14
PC5/AN13
PC4/AN12
PC3/AN11
PC2/AN10
PC1/AN9
PC0/AN8
PB7
PB6/INT1/AN6
PB5/PCK/AN5
PB4/TP0_1/AN4
PB3/SCS/AN3
PB2/SCK/AN2
PB1/SDI/SCL/AN1
PB0/SDO/SDA/AN0
PE2
PD0/TP3_1/OSC1
PD1/TP2_1/OSC2
PD2/TCK2
PD3
PD4/TCK3
PD5/TP1_1
PD6/TP3_0
PD7/TP2_0
HT66FB560
48 LQFP-A
NC
HT66FB560
64 LQFP-A
PF0
PF1
PF2
PF3
PF4
PF5
PF6
PF7

Pin Description

The pins on these devices can be referenced by their Port name, e.g. PA.0, PA.1 etc, which refer to the digital I/O function of the pins. However these Port pins are also shared with other functions such as the Analog to Digital Converter, Serial Port pins etc. The function of each pin is listed in the following table, however the details behind how each pin is configured is contained in other sections of the datasheet.

HT66FB540

Pin Name	Function	OPT	I/T	O/T	Description
PA0/TCK1/OCDSDA	PA0	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TCK1	—	ST	—	TM1 input
	OCDSDA	—	ST	CMOS	Debug Data I/O in On - Chip Debug Support mode
PA1/SDOA/C0X	PA1	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SDOA	—	—	CMOS	SPIA Data output
	C0X	—	—	CMOS	Comparator 0 output
PA2/SDIA/C0+	PA2	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SDIA	—	ST	—	SPIA Data input
	C0+	—	AN	—	Comparator 0 positive input
PA3/SCKA/C0-	PA3	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SCKA	—	ST	NMOS	SPIA Serial Clock
	C0-	—	AN	—	Comparator 0 negative input
PA4/$\overline{\text{SCSA}}$/TP0_0/C1X	PA4	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	$\overline{\text{SCSA}}$	—	ST	CMOS	SPIA Slave select
	TP0_0	TMPC0	ST	CMOS	TM0 I/O
	C1X	—	—	CMOS	Comparator 1 output
PA5/TP1_0/C1+	PA5	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP1_0	TMPC0	ST	CMOS	TM1 I/O
	C1+	—	AN	—	Comparator 1 positive input
PA6/TCK0/C1-	PA6	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TCK0	—	ST	—	TM0 input
	C1-	—	AN	—	Comparator 1 negative input
PA7/INT0/AN7	PA7	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	INT0	—	ST	—	External interrupt 0
	AN7	ACER0	AN	—	A/D Channel 7
PB0/SDO/SDA/AN0	PB0	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SDO	—	—	CMOS	SPI Data output
	SDA	—	ST	NMOS	I^2C Data
	AN0	ACER0	AN	—	A/D Channel 0
PB1/SDI/SCL/AN1	PB1	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SDI	—	ST	—	SPI Data input
	SCL	—	ST	NMOS	I^2C Clock
	AN1	ACER0	AN	—	A/D Channel 1

Pin Name	Function	OPT	I/T	O/T	Description
PB2/SCK/AN2	PB2	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SCK	—	ST	CMOS	SPI Serial Clock
	AN2	ACER0	AN	—	A/D Channel 2
PB3/$\overline{SCS}$/AN3	PB3	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	$\overline{SCS}$	—	ST	CMOS	SPI Slave select
	AN3	ACER0	AN	—	A/D Channel 3
PB4/TP0_1/AN4	PB4	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP0_1	TMPC0	ST	CMOS	TM0 I/O
	AN4	ACER0	AN	—	A/D Channel 4
PB5/PCK/AN5	PB5	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	PCK	—	—	CMOS	Peripheral output clock
	AN5	ACER0	AN	—	A/D Channel 5
PB6/INT1/AN6	PB6	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	INT1	—	ST	—	External interrupt 1
	AN6	ACER0	AN	—	A/D Channel 6
PD0/TP3_1/OSC1	PD0	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP3_1	TMPC1	ST	CMOS	TM3 I/O
	OSC1	—	HXT	—	HXT pin
PD1/TP2_1/OSC2	PD1	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP2_1	TMPC1	ST	CMOS	TM2 I/O
	OSC2	—	—	HXT	HXT pin
PD2/TCK2	PD2	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TCK2	—	ST	—	TM2 input
PD3	PD3	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
PD4/TCK3	PD4	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TCK3	TMPC1	ST	—	TM3 input
PD5/TP1_1	PD5	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP1_1	TMPC0	ST	CMOS	TM1 I/O
PE0/VDDIO/VREF	PE0	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	VDDIO	—	PWR	—	PA external power input
	VREF	—	AN	—	ADC reference power input
PE1/UBUS	PE1	—	ST	—	General purpose I/O. Input only
	UBUS	—	PWR	—	USB SIE VDD
PE2	PE2	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
PE3/XT1	PE3	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	XT1	CO	LXT	—	LXT pin
PE4/XT2	PE4	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	XT2	CO	—	LXT	LXT pin

Pin Name	Function	OPT	I/T	O/T	Description
$\overline{RES}$/OCDSCK	$\overline{RES}$	CO	ST	—	Reset input
	OCDSCK	—	ST	—	Debug clock input in On-Chip Debug Support mode
UDN/GPIO0	UDN	—	ST	CMOS	USB UDN line
	GPIO0	—	ST	CMOS	General purpose I/O
UDP/GPIO1	UDP	—	ST	CMOS	USB UDP line
	GPIO1	—	ST	CMOS	General purpose I/O
VDD/AVDD	VDD/ AVDD	—	PWR	—	Power supply
VSS/AVSS	VSS/ AVSS	—	PWR	—	Ground
V33O	V33O	—	—	PWR	3.3V regulator output
HVDD	HVDD	—	PWR	—	HIRC oscillator Positive Power supply

Note: I/T: Input type; O/T: Output type
OPT: Optional by configuration option (CO) or register option
PWR: Power; CO: Configuration option
ST: Schmitt Trigger input; CMOS: CMOS output;
HXT: High frequency crystal oscillator
LXT: Low frequency crystal oscillator
AN: Analog input pin

Where devices exist in more than one package type the table reflects the situation for the package with the largest number of pins. For this reason not all pins described in the table may exist on all package types.

HT66FB550

Pin Name	Function	OPT	I/T	O/T	Description
PA0/TCK1/OCDSDA	PA0	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TCK1	—	ST	—	TM1 input
	OCDSDA	—	ST	CMOS	Debug Data I/O in On-Chip Debug Support mode
PA1/SDOA/C0X	PA1	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SDOA	—	—	CMOS	SPIA Data output
	C0X	—	—	CMOS	Comparator 0 output
PA2/SDIA/C0+	PA2	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SDIA	—	ST	—	SPIA Data input
	C0+	—	AN	—	Comparator 0 positive input
PA3/SCKA/C0-	PA3	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SCKA	—	ST	NMOS	SPIA Serial Clock
	C0-	—	AN	—	Comparator 0 negative input
PA4/$\overline{\text{SCSA}}$/TP0_0/ C1X	PA4	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	$\overline{\text{SCSA}}$	—	ST	CMOS	SPIA Slave select
	TP0_0	TMPC0	ST	CMOS	TM0 I/O
	C1X	—	—	CMOS	Comparator 1 output
PA5/TP1_0/C1+	PA5	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP1_0	TMPC0	ST	CMOS	TM1 I/O
	C1+	—	AN	—	Comparator 1 positive input
PA6/TCK0/C1-	PA6	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TCK0	—	ST	—	TM0 input
	C1-	—	AN	—	Comparator 1 negative input
PA7/INT0/AN7	PA7	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	INT0	—	ST	—	External interrupt 0
	AN7	ACER0	AN	—	A/D Channel 7
PB0/SDO/SDA/AN0	PB0	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SDO	—	—	CMOS	SPI Data output
	SDA	—	ST	NMOS	I^2C Data
	AN0	ACER0	AN	—	A/D Channel 0
PB1/SDI/SCL/AN1	PB1	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SDI	—	ST	—	SPI Data input
	SCL	—	ST	NMOS	I^2C Clock
	AN1	ACER0	AN	—	A/D Channel 1
PB2/SCK/AN2	PB2	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SCK	—	ST	CMOS	SPI Serial Clock
	AN2	ACER0	AN	—	A/D Channel 2
PB3/$\overline{\text{SCS}}$/AN3	PB3	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	$\overline{\text{SCS}}$	—	ST	CMOS	SPI Slave select
	AN3	ACER0	AN	—	A/D Channel 3

Pin Name	Function	OPT	I/T	O/T	Description
PB4/TP0_1/AN4	PB4	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP0_1	TMPC0	ST	CMOS	TM0 I/O
	AN4	ACER0	AN	—	A/D Channel 4
PB5/PCK/AN5	PB5	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	PCK	—	—	CMOS	Peripheral output clock
	AN5	ACER0	AN	—	A/D Channel 5
PB6/INT1/AN6	PB6	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	INT1	—	ST	—	External interrupt 1
	AN6	ACER0	AN	—	A/D Channel 6
PB7	PB7	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
PC0/AN8	PC0	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	AN8	ACER1	AN	—	A/D Channel 8
PC1/AN9	PC1	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	AN9	ACER1	AN	—	A/D Channel 9
PC2/AN10	PC2	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	AN10	ACER1	AN	—	A/D Channel 10
PC3/AN11	PC3	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	AN11	ACER1	AN	—	A/D Channel 11
PC4/AN12	PC4	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	AN12	ACER1	AN	—	A/D Channel 12
PC5/AN13	PC5	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	AN13	ACER1	AN	—	A/D Channel 13
PC6/AN14	PC6	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	AN14	ACER1	AN	—	A/D Channel 14
PC7/AN15	PC7	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	AN15	ACER1	AN	—	A/D Channel 15
PD0/TP3_1/OSC1	PD0	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP3_1	TMPC1	ST	CMOS	TM3 I/O
	OSC1	—	HXT	—	HXT pin
PD1/TP2_1/OSC2	PD1	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP2_1	TMPC1	ST	CMOS	TM2 I/O
	OSC2	—	—	HXT	HXT pin
PD2/TCK2	PD2	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TCK2	—	ST	—	TM2 input
PD3	PD3	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
PD4/TCK3	PD4	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TCK3	TMPC1	ST	—	TM3 input

Pin Name	Function	OPT	I/T	O/T	Description
PD5/TP1_1	PD5	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP1_1	TMPC0	ST	CMOS	TM1 I/O
PD6/TP3_0	PD6	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP3_0	TMPC1	ST	CMOS	TM3 I/O
PD7/TP2_0	PD7	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP2_0	TMPC1	ST	CMOS	TM2 I/O
PE0/VDDIO/VREF	PE0	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	VDDIO	—	PWR	—	PA external power input
	VREF	—	AN	—	ADC reference power input
PE1/UBUS	PE1	—	ST	—	General purpose I/O. Input only
	UBUS	PWR	PWR	—	USB SIE VDD
PE2	PE2	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
PE3/XT1	PE3	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	XT1	CO	LXT	—	LXT pin
PE4/XT2	PE4	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	XT2	CO	—	LXT	LXT pin
PE5	PE5	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
$\overline{\text{RES}}$/OCDSCK	$\overline{\text{RES}}$	CO	ST	—	Reset input
	OCDSCK	—	ST	—	Debug clock input in On-Chip Debug Support mode
UDN/GPIO0	UDN	—	ST	CMOS	USB UDN line
	GPIO0	—	ST	CMOS	General purpose I/O
UDP/GPIO1	UDP	—	ST	CMOS	USB UDP line
	GPIO1	—	ST	CMOS	General purpose I/O
VDD/AVDD	VDD/ AVDD	—	PWR	—	Power supply
VSS/AVSS	VSS/ AVSS	—	PWR	—	Ground
V33O	V33O	—	—	PWR	3.3V regulator output
HVDD	HVDD	—	PWR	—	HIRC oscillator Positive Power supply.

Note: I/T: Input type; O/T: Output type
OPT: Optional by configuration option (CO) or register option
PWR: Power; CO: Configuration option
ST: Schmitt Trigger input; CMOS: CMOS output;
HXT: High frequency crystal oscillator
LXT: Low frequency crystal oscillator
AN: Analog input pin

Where devices exist in more than one package type the table reflects the situation for the package with the largest number of pins. For this reason not all pins described in the table may exist on all package types.

HT66FB560

Pin Name	Function	OPT	I/T	O/T	Description
PA0/TCK1/OCDSDA	PA0	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TCK1	—	ST	—	TM1 input
	OCDSDA	—	ST	CMOS	Debug Data I/O in On-Chip Debug Support mode
PA1/SDOA/C0X	PA1	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SDOA	—	—	CMOS	SPIA Data output
	C0X	—	—	CMOS	Comparator 0 output
PA2/SDIA/C0+	PA2	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SDIA	—	ST	—	SPIA Data input
	C0+	—	AN	—	Comparator 0 positive input
PA3/SCKA/C0-	PA3	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SCKA	—	ST	NMOS	SPIA Serial Clock
	C0-	—	AN	—	Comparator 0 negative input
PA4/$\overline{\text{SCSA}}$/TP0_0/C1X	PA4	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	$\overline{\text{SCSA}}$	—	ST	CMOS	SPIA Slave select
	TP0_0	TMPC0	ST	CMOS	TM0 I/O
	C1X	—	—	CMOS	Comparator 1 output
PA5/TP1_0/C1+	PA5	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP1_0	TMPC0	ST	CMOS	TM1 I/O
	C1+	—	AN	—	Comparator 1 positive input
PA6/TCK0/C1-	PA6	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TCK0	—	ST	—	TM0 input
	C1-	—	AN	—	Comparator 1 negative input
PA7/INT0/AN7	PA7	PAPU PAWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	INT0	—	ST	—	External interrupt 0
	AN7	ACER0	AN	—	A/D Channel 7
PB0/SDO/SDA/AN0	PB0	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SDO	—	—	CMOS	SPI Data output
	SDA	—	ST	NMOS	I^2C Data
	AN0	ACER0	AN	—	A/D Channel 0
PB1/SDI/SCL/AN1	PB1	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SDI	—	ST	—	SPI Data input
	SCL	—	ST	NMOS	I^2C Clock
	AN1	ACER0	AN	—	A/D Channel 1
PB2/SCK/AN2	PB2	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	SCK	—	ST	CMOS	SPI Serial Clock
	AN2	ACER0	AN	—	A/D Channel 2

Pin Name	Function	OPT	I/T	O/T	Description
PB3/$\overline{SCS}$/AN3	PB3	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	$\overline{SCS}$	—	ST	CMOS	SPI Slave select
	AN3	ACER0	AN	—	A/D Channel 3
PB4/TP0_1/AN4	PB4	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP0_1	TMPC0	ST	CMOS	TM0 I/O
	AN4	ACER0	AN	—	A/D Channel 4
PB5/PCK/AN5	PB5	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	PCK	—	—	CMOS	Peripheral output clock
	AN5	ACER0	AN	—	A/D Channel 5
PB6/INT1/AN6	PB6	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	INT1	—	ST	—	External interrupt 1
	AN6	ACER0	AN	—	A/D Channel 6
PB7	PB7	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
PC0/AN8	PC0	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	AN8	ACER1	AN	—	A/D Channel 8
PC1/AN9	PC1	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	AN9	ACER1	AN	—	A/D Channel 9
PC2/AN10	PC2	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	AN10	ACER1	AN	—	A/D Channel 10
PC3/AN11	PC3	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	AN11	ACER1	AN	—	A/D Channel 11
PC4/AN12	PC4	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
	AN12	ACER1	AN	—	A/D Channel 12
PC5/AN13	PC5	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	AN13	ACER1	AN	—	A/D Channel 13
PC6/AN14	PC6	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	AN14	ACER1	AN	—	A/D Channel 14
PC7/AN15	PC7	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	AN15	ACER1	AN	—	A/D Channel 15
PD0/TP3_1/OSC1	PD0	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP3_1	TMPC1	ST	CMOS	TM3 I/O
	OSC1	—	HXT	—	HXT pin
PD1/TP2_1/OSC2	PD1	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP2_1	TMPC1	ST	CMOS	TM2 I/O
	OSC2	—	—	HXT	HXT pin

Pin Name	Function	OPT	I/T	O/T	Description
PD2/TCK2	PD2	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TCK2	—	ST	—	TM2 input
PD3	PD3	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
PD4/TCK3	PD4	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TCK3	TMPC1	ST	—	TM3 input
PD5/TP1_1	PD5	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP1_1	TMPC0	ST	CMOS	TM1 I/O
PD6/TP3_0	PD6	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP3_0	TMPC1	ST	CMOS	TM3 I/O
PD7/TP2_0	PD7	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	TP2_0	TMPC1	ST	CMOS	TM2 I/O
PE0/VDDIO/VREF	PE0	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	VDDIO	—	PWR	—	PA external power input
	VREF	—	AN	—	ADC reference power input
PE1/UBUS	PE1	—	ST	—	General purpose I/O. Input only
	UBUS	PWR	PWR	—	USB SIE VDD
PE2	PE2	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
PE3/XT1	PE3	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	XT1	CO	LXT	—	LXT pin
PE4/XT2	PE4	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
	XT2	CO	—	LXT	LXT pin
PE5	PE5	PXPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
PF0	PF0	PFPU PXWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up.
PF1	PF1	PFPU PFWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
PF2	PF2	PFPU PFWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
PF3	PF3	PFPU PFWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
PF4	PF4	PFPU PFWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
PF5	PF5	PFPU PFWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
PF6	PF6	PFPU PFWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up
PF7	PF7	PFPU PFWU	ST	CMOS	General purpose I/O. Register enabled pull-up and wake-up

Pin Name	Function	OPT	I/T	O/T	Description
$\overline{RES}$/OCDSCK	$\overline{RES}$	CO	ST	—	Reset input
	OCDSCK	—	ST	—	Debug clock input in On-Chip Debug Support mode
UDN/GPIO0	UDN	—	ST	CMOS	USB UDN line
	GPIO0	—	ST	CMOS	General purpose I/O
UDP/GPIO1	UDP	—	ST	CMOS	USB UDP line
	GPIO1	—	ST	CMOS	General purpose I/O
VDD/AVDD	VDD/ AVDD	—	PWR	—	Power supply
VSS/AVSS	VSS/ AVSS	—	PWR	—	Ground
V33O	V33O	—	—	PWR	3.3V regulator output
HVDD	HVDD	—	PWR	—	HIRC oscillator Positive Power supply

Note: I/T: Input type; O/T: Output type
OPT: Optional by configuration option (CO) or register option
PWR: Power; CO: Configuration option
ST: Schmitt Trigger input; CMOS: CMOS output;
HXT: High frequency crystal oscillator
LXT: Low frequency crystal oscillator
AN: Analog input pin

Where devices exist in more than one package type the table reflects the situation for the package with the largest number of pins. For this reason not all pins described in the table may exist on all package types.

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}−0.3V to V_{SS}+6.0V
Input Voltage ..... V_{SS}−0.3V to V_{DD}+0.3V
Storage Temperature ..... -50°C to 125°C
Operating Temperature ..... -40°C to 85°C
I_{OH} Total ..... -100mA
I_{OL} Total 150mA
Total Power Dissipation 500mW

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to these devices. Functional operation of these devices at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect devices reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD1}	Operating Voltage (Crystal OSC)	—	f_{SYS}=4MHz	2.2	—	5.5	V
			f_{SYS}=6MHz	2.2	—	5.5	V
			f_{SYS}=8MHz	2.2	—	5.5	V
			f_{SYS}=12MHz	2.7	—	5.5	V
			f_{SYS}=16MHz	4.5	—	5.5	V
V_{DD2}	Operating Voltage (High Frequency Internal RC OSC)	—	f_{SYS}=12MHz	2.7	—	5.5	V
I_{DD1}	Operating Current (Crystal OSC, $f_{SYS}=f_H$, $f_S=f_{SUB}=f_{LXT}$ or f_{LIRC})	3V	No load, f_H=4MHz, ADC off, WDT enable	—	0.8	1.5	mA
		5V		—	1.8	4.0	mA
		3V	No load, f_H=6MHz, ADC off, WDT enable	—	1.0	2.0	mA
		5V		—	2.5	5.0	mA
		3V	No load, f_H=8MHz, ADC off, WDT enable	—	1.3	3.0	mA
		5V		—	3.0	5.5	mA
		3V	No load, f_H=12MHz, ADC off, WDT enable	—	2.0	4.0	mA
		5V		—	4.0	7.0	mA
I_{DD2}	Operating Current (HIRC OSC, $f_{SYS}=f_H$, $f_S=f_{SUB}=f_{LXT}$ or f_{LIRC})	3V	No load, f_H=12MHz, ADC off, WDT enable	—	2.0	4.0	mA
		5V		—	4.0	7.0	mA
I_{DD3}	Operating Current (LXT OSC, $f_{SYS}=f_L=f_{LXT}$, $f_S=f_{SUB}=f_{LXT}$)	3V	No load, ADC off, WDT enable. LVR enable	—	40	80	μA
		5V		—	70	150	μA
I_{DD4}	Operating Current (LIRC OSC, $f_{SYS}=f_L=f_{LIRC}$, $f_S=f_{SUB}=f_{LIRC}$)	3V	No load, ADC off, WDT enable, LVR enable, f_{LIRC}=32kHz	—	40	80	μA
		5V		—	70	150	μA
I_{DD5}	Operating Current (HIRC OSC, $f_{SYS}=f_H$, $f_S=f_{SUB}=f_{LXT}$ or f_{LIRC})	3V	No load, f_H=12MHz, ADC off, WDT enable, USB enable, PLL on, V33O on	—	5.5	10.0	mA
		5V		—	11	16	mA
I_{DD6}	Operating Current (Crystal OSC, $f_{SYS}=f_H$, $f_S=f_{SUB}=f_{LIRC}$)	5V	No load, f_H=6MHz, ADC off, WDT enable, USB enable, PLL on, V33O on	—	10	15	mA
		5V	No load, f_H=12MHz, ADC off, WDT enable, USB enable, PLL on, V33O on	—	11	16	mA
		5V	No load, f_H=16MHz, ADC off, WDT enable, USB enable, PLL on, V33O on	—	12	17	mA
I_{STB1}	Stanby Current (Idle 1) (Crystal OSC, $f_{SYS}=f_H$, $f_S=f_{SUB}=f_{LXT}$ or f_{LIRC})	3V	No load, system HALT, ADC off, WDT enable, f_{SYS}=oscillator on (FSYSON=1)	—	0.8	1.5	mA
		5V		—	1.5	3.0	mA
I_{STB2}	Stanby Current (Idle 0) (Crystal or HIRC OSC, f_{SYS}=off, $f_S=f_{SUB}=f_{LXT}$ or f_{LIRC})	3V	No load, system HALT, ADC off, WDT enable, f_{SYS}=oscillator off (FSYSON=0)	—	1.5	3.0	μA
		5V		—	3.0	6.0	μA
I_{STB3}	Stanby Current (Idle 0) (LXT OSC, f_{SYS}=off, $f_S=f_{SUB}=f_{LXT}$)	3V	No load, system HALT, ADC off, WDT enable	—	2.0	4.0	μA
		5V		—	3.5	7.0	μA
I_{STB4}	Stanby Current (Idle) (LIRC OSC, f_{SYS}=off, $f_S=f_{SUB}=f_{LIRC}$)	3V	No load, system HALT, ADC off, WDT enable	—	1.5	3.0	μA
		5V		—	3.0	6.0	μA
I_{STB5}	Stanby Current (Sleep 0) (Crystal or HIRC OSC, f_{SYS}=off, $f_S=f_{SUB}=f_{LXT}$ or f_{LIRC})	3V	No load, system HALT, ADC off, WDT disable	—	0.1	1.0	μA
		5V		—	0.3	2.0	μA

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
I_{STB6}	Stanby Current (Sleep 1) (Crystal or HIRC OSC, f_{SYS}=off, $f_S=f_{SUB}=f_{LXT}$ or f_{LIRC})	3V	No load, system HALT, ADC off, WDT enable	—	1.5	3.0	μA
		5V		—	3.0	6.0	μA
I_{STB7}	Stanby Current (Sleep 0) (Crystal or HIRC OSC, f_{SYS}=off, $f_S=f_{SUB}=f_{LXT}$ or f_{LIRC})	—	No load, system HALT, ADC off, WDT disable, LVR enable and LVDEN=1	—	60	90	μA
I_{SUS1}	Suspend Current (Sleep 0) (Crystal or HIRC OSC, f_{SYS}=off, $f_S=f_{SUB}=f_{LXT}$ or f_{LIRC})	5V	No load, system HALT, ADC off, WDT disable, USB transceiver, 3.3V Regulator on and clr suspend2 (UCC.4)	—	360	420	μA
I_{SUS2}	Suspend Current (Sleep 0) (Crystal or HIRC OSC, f_{SYS}=off, $f_S=f_{SUB}=f_{LXT}$ or f_{LIRC})	5V	No load, system HALT, ADC off, WDT disable, USB transceiver, 3.3V Regulator on and set suspend2 (UCC.4)	—	240	320	μA
V_{IL1}	Input Low Voltage for I/O Ports, TCK and INT	—	—	0	—	$0.2V_{DD}$	V
V_{IH1}	Input High Voltage for I/O Ports, TCK and INT	—	—	$0.8V_{DD}$	—	V_{DD}	V
V_{IL2}	Input Low Voltage ($\overline{RES}$)	—	—	0	—	$0.4V_{DD}$	V
V_{IH2}	Input High Voltage ($\overline{RES}$)	—	—	$0.9V_{DD}$	—	V_{DD}	V
I_{OL}	I/O Port Sink Current	3V	$V_{OL}=0.1V_{DD}$ (PAOI or PXOI=1)	4	8	—	mA
		5V	$V_{OL}=0.1V_{DD}$ (PAOI or PXOI=1)	10	20	—	mA
		5V	$V_{OL}=0.1V_{DD}$ (PAOI or PXOI=0)	2	4	—	mA
I_{OH}	I/O Port, Source Current	3V	$V_{OH}=0.9V_{DD}$ (PAOI or PXOI=1)	-2	-4	—	mA
		5V	$V_{OH}=0.9V_{DD}$ (PAOI or PXOI=1)	-5	-10	—	mA
		5V	$V_{OH}=0.9V_{DD}$ (PAOI or PXOI=0)	-2	-4	—	mA
V_{V33O}	3.3V regulator output	5V	I_{V33O}=70mA	3.0	3.3	3.6	V
R_{UDP}	Pull-high Resistance of UDP to V33O	3.3V	—	-5%	1.5	+5%	kΩ
R_{PH}	Pull-high Resistance of I/O Ports	3V	—	20	60	100	kΩ
		5V	—	10	30	50	kΩ
R_{PL}	Pull-low Resistance of UBUS pin	5V	SUSP2=1, RUBUS=0	0.5	1	1.5	MΩ

A.C. Characteristics

Ta=25°C

Symbol	Parameter	V_{DD}	Condition	Min.	Typ.	Max.	Unit
f_{SYS1}	System clock (Crystal OSC)	2.2~5.5V	—	2	—	4	MHz
		2.2~5.5V		2	—	6	MHz
		2.2~5.5V		2	—	8	MHz
		2.7~5.5V		2	—	12	MHz
		4.5~5.5V		2	—	16	MHz
f_{SYS2}	System Clock (HIRC OSC)	2.2~5.5V	Non-USB mode, Ta=25°C	-3%	12	+3%	MHz
		3.0~5.5V	Non-USB mode, Ta=-40~85°C	-6%	12	+6%	MHz
		2.2~5.5V	Non-USB mode, Ta=-40~85°C	-10%	12	+10%	MHz
		3.3~5.5V	USB mode	-0.25%	12	+0.25%	MHz
f_{SYS3}	System Clock (32768 Crystal)	—	—	—	32768	—	Hz
f_{LIRC}	System Clock (32K RC)	5V	Ta=25°C	-10%	32	+10%	kHz
		2.2~5.5V	Ta=-40°C to 85°C	-50%	32	+60%	kHz
f_{TIMER}	Timer I/P Frequency (TMR)	2.2~5.5V	—	2	—	8	MHz
		2.7~5.5V		2	—	12	MHz
		4.5~5.5V		2	—	16	MHz
t_{BGS}	VBG turn on stable time	—	—	10	—	—	ms
t_{TIMER}	TCKn Input Pin Minimum Pulse Width	—	—	0.3	—	—	μs
t_{RES}	External Reset Minimum Low Pulse Width	—	—	10	—	—	μs
t_{INT}	Interrupt Minimum Pulse Width	—	—	10	—	—	μs
t_{SST}	System Start-up Timer Period (Wake-up from HALT, f_{SYS} off at HALT state, Slow Mode → Normal Mode, Normal Mode → Slow Mode)	—	f_{SYS}=HXT or LXT (Slow Mode → Normal Mode(HXT), Normal Mode → Slow Mode(LXT))	1024	—	—	t_{SYS}
		—	f_{SYS}=HXT (Wake-up from HALT, f_{SYS} off at HALT state)	1024	—	—	t_{SYS}
		—	f_{SYS}=HIRC	1024	—	—	t_{SYS}
		—	f_{SYS}=LIRC	2	—	—	t_{SYS}
	System Start-up Timer Period (Wake-up from HALT, f_{SYS} on at HALT state)	—	—	2	—	—	t_{SYS}
	System Start-up Timer Period (Reset)	—	—	1024	—	—	t_{SYS}
t_{RSTD}	System Reset Delay Time (Power On Reset)	—	—	25	50	100	ms
	System Reset Delay Time (Any Reset except Power On Reset)	—	—	8.3	16.7	33.3	ms

LVD & LVR Electrical Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{LVR1}	Low Voltage Reset Voltage	—	LVR Enable, 2.1V option	-5% ×Typ.	2.1	+5% ×Typ.	V
V_{LVR2}			LVR Enable, 2.55V option		2.55		V
V_{LVR3}			LVR Enable, 3.15V option		3.15		V
V_{LVR4}			LVR Enable, 3.8V option		3.8		V
V_{LVD1}	Low Voltage Detector Voltage	—	LVDEN=1, V_{LVD}=2.0V	-5% ×Typ.	2.0	+5% ×Typ.	V
V_{LVD2}			LVDEN=1, V_{LVD}=2.2V		2.2		V
V_{LVD3}			LVDEN=1, V_{LVD}=2.4V		2.4		V
V_{LVD4}			LVDEN=1, V_{LVD}=2.7V		2.7		V
V_{LVD5}			LVDEN=1, V_{LVD}=3.0V		3.0		V
V_{LVD6}			LVDEN=1, V_{LVD}=3.3V		3.3		V
V_{LVD7}			LVDEN=1, V_{LVD}=3.6V		3.6		V
V_{LVD8}			LVDEN=1, V_{LVD}=4.0V		4.0		V
V_{BG}	Reference Voltage with Buffer Voltage	—	—	-3%	1.25	+3%	V
I_{BG}	Additional Power Consumption if Reference with Buffer is used	—	—	—	200	300	μA
I_{LVD}	Additional Power Consumption if LVD/LVR is Used	3V	LVD disable → LVD enable (LVR enable)	—	30	45	μA
		5V		—	60	90	μA
t_{LVR}	Low Voltage Width to Reset	—	—	7	—	8	t_{LIRC}
t_{LVR}	Low Voltage Width to Reset	—	—	120	240	480	us
t_{LVD}	Low Voltage Width to Interrupt	—	—	1	—	2	t_{LIRC}
t_{LVD}	Low Voltage Width to Interrupt	—	—	20	45	90	μs
t_{SRESET}	Software Reset Width to Reset	—	—	2	—	3	t_{LIRC}
t_{SRESET}	Software Reset Width to Reset	—	—	45	90	120	μs
t_{LVDS}	LVDO stable time	—	For LVR enable, LVD off → on	15	—	—	μs

ADC Electrical Characteristics

Ta=25°C

Symbol	Parameter	V_{DD}	Condition	Min.	Typ.	Max.	Unit
AV_{DD}	Analog operating voltage	—	$V_{REF}=AV_{DD}$	2.7	—	5.5	V
V_{ADI}	A/D Input Voltage	—	—	0	—	V_{REF}	V
V_{REF}	ADC input reference voltage range	—	AV_{DD}=3V	2.0	—	AV_{DD}	V
		—	AV_{DD}=5V	2.0	—	AV_{DD}	V
t_{ADC}	A/D Conversion Time	2.7~5.5V	12 bit ADC	16	—	20	t_{AD}
t_{ADCK}	A/D Converter Clock Period	2.7~5.5V	—	0.5	—	10	μs
t_{ON2ST}	ADC on to ADC start	2.7~5.5V	—	4	—	—	μs
DNL	Differential non-linearity	3V/5V	$V_{REF}=AV_{DD}$	-3	—	+3	LSB
INL	Integral non-linearity	3V/5V	$V_{REF}=AV_{DD}$	-4	—	+4	LSB
I_{ADC}	only ADC Enable, Others Disable	3V	No load (t_{AD}=0.5μs)	—	1.0	2.0	mA
		5V	No load (t_{AD}=0.5μs)	—	1.5	3.0	mA

Comparator Electrical Characteristics

Ta=25°C

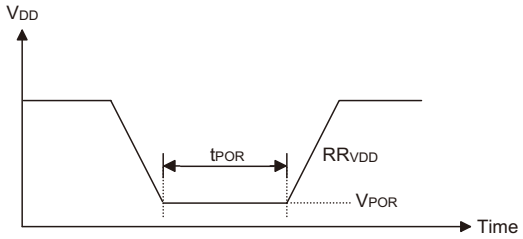
Symbol	Parameter	V_{DD}	Condition	Min.	Typ.	Max.	Unit
V_{CMP}	Comparator operating voltage	—	—	2.2	—	5.5	V
I_{CMP}	Comparator operating current	5V	—	—	—	200	μA
I_{CSTB}	Comparator power down current	5V	Comparator disable	—	—	0.1	μA
V_{CMPOS}	Comparator input offset voltage	5V	—	-10	—	+10	mV
V_{HYS}	Hysteresis width	5V		20	40	60	mV
V_{CM}	Comparator common mode voltage range	—	—	V_{SS}	—	V_{DD}-1.4V	V
A_{OL}	Comparator open loop gain	—	—	60	80	—	dB
t_{PD}	Comparator response time	3V	With 100mV overdrive(Note)	—	200	400	ns
		5V					

Note: Measured with comparator one input pin at $V_{CM}=(V_{DD}-1.4)/2$ while the other pin input transition from V_{SS} to (V_{CM}+100mV) or from V_{DD} to (V_{CM}-100mV).

Power on Reset (AC+DC) Electrical Characteristics

Ta=25°C

Symbol	Parameter	V_{DD}	Condition	Min.	Typ.	Max.	Unit
V_{POR}	V_{DD} Start Voltage to ensure Power-on Reset	—	—	—	—	100	mV
R_{POR_AC}	V_{DD} Rise Rate to ensure Power-on Reset	—	—	0.035	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} Stays at V_{POR} to Ensure Power-on Reset	—	—	1	—	—	ms



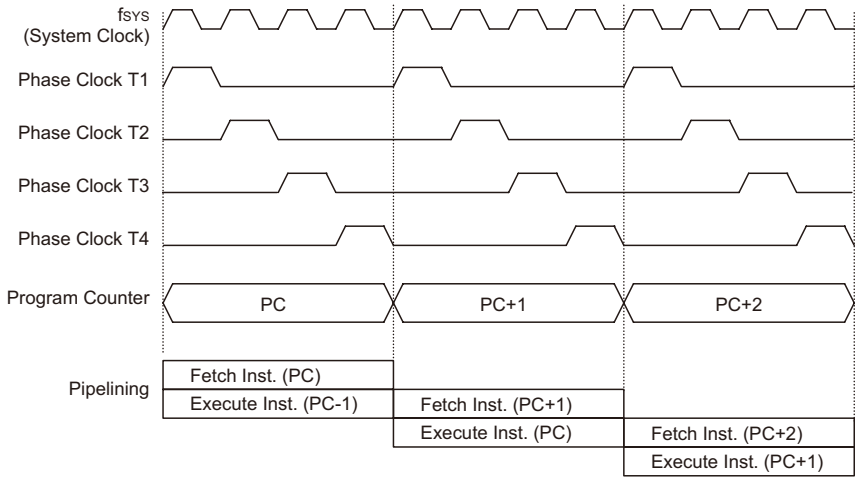
System Architecture

A key factor in the high-performance features of the Holtek range of microcontrollers is attributed to their internal system architecture. The range of devices take advantage of the usual features found within RISC microcontrollers providing increased speed of operation and enhanced performance. The pipelining scheme is implemented in such a way that instruction fetching and instruction execution are overlapped, hence instructions are effectively executed in one cycle, with the exception of branch or call instructions. An 8-bit wide ALU is used in practically all instruction set operations, which carries out arithmetic operations, logic operations, rotation, increment, decrement, branch decisions, etc. The internal data path is simplified by moving data through the Accumulator and the ALU. Certain internal registers are implemented in the Data Memory and can be directly or indirectly addressed. The simple addressing methods of these registers along with additional architectural features ensure that a minimum of external components is required to provide a functional I/O and A/D control system with maximum reliability and flexibility. This makes these devices suitable for low-cost, high-volume production for controller applications.

Clocking and Pipelining

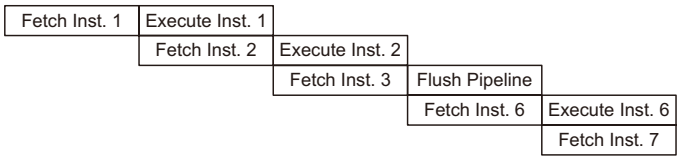
The main system clock, derived from either a HXT, LXT, HIRC or LIRC oscillator is subdivided into four internally generated non-overlapping clocks, T1~T4. The Program Counter is incremented at the beginning of the T1 clock during which time a new instruction is fetched. The remaining T2~T4 clocks carry out the decoding and execution functions. In this way, one T1~T4 clock cycle forms one instruction cycle. Although the fetching and execution of instructions takes place in consecutive instruction cycles, the pipelining structure of the microcontroller ensures that instructions are effectively executed in one instruction cycle. The exception to this are instructions where the contents of the Program Counter are changed, such as subroutine calls or jumps, in which case the instruction will take one more instruction cycle to execute.

For instructions involving branches, such as jump or call instructions, two machine cycles are required to complete instruction execution. An extra cycle is required as the program takes one cycle to first obtain the actual jump or call address and then another cycle to actually execute the branch. The requirement for this extra cycle should be taken into account by programmers in timing sensitive applications.



System Clocking and Pipelining

```
1          MOV A,[12H]
2          CALL DELAY
3          CPL [12H]
4          :
5          :
6  DELAY:  NOP
```



Instruction Fetching

Program Counter

During program execution, the Program Counter is used to keep track of the address of the next instruction to be executed. It is automatically incremented by one each time an instruction is executed except for instructions, such as "JMP" or "CALL" that demand a jump to a non-consecutive Program Memory address. Only the lower 8 bits, known as the Program Counter Low Register, are directly addressable by the application program.

When executing instructions requiring jumps to non-consecutive addresses such as a jump instruction, a subroutine call, interrupt or reset, etc., the microcontroller manages program control by loading the required address into the Program Counter. For conditional skip instructions, once the condition has been met, the next instruction, which has already been fetched during the present instruction execution, is discarded and a dummy cycle takes its place while the correct instruction is obtained.

Device	Program Counter	
	Program Counter High Byte	PCL Register
HT66FB540	PC11~PC8	PCL7~PCL0
HT66FB550	PC12~PC8	
HT66FB560	PC13~PC8	

Program Counter

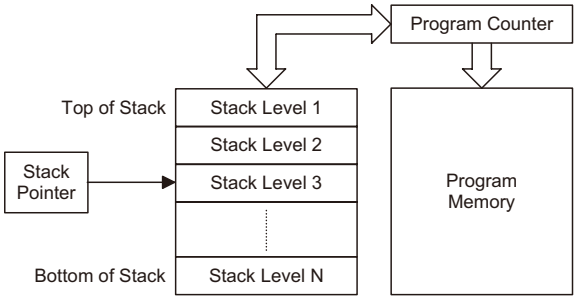
The lower byte of the Program Counter, known as the Program Counter Low register or PCL, is available for program control and is a readable and writeable register. By transferring data directly into this register, a short program jump can be executed directly; however, as only this low byte is available for manipulation, the jumps are limited to the present page of memory, which is 256 locations. When such program jumps are executed it should also be noted that a dummy cycle will be inserted. Manipulating the PCL register may cause program branching, so an extra cycle is needed to pre-fetch.

Stack

This is a special part of the memory which is used to save the contents of the Program Counter only. The stack has multiple levels depending upon these devices and is neither part of the data nor part of the program space, and is neither readable nor writeable. The activated level is indexed by the Stack Pointer, and is neither readable nor writeable. At a subroutine call or interrupt acknowledge signal, the contents of the Program Counter are pushed onto the stack. At the end of a subroutine or an interrupt routine, signaled by a return instruction, RET or RETI, the Program Counter is restored to its previous value from the stack. After a device reset, the Stack Pointer will point to the top of the stack.

If the stack is full and an enabled interrupt takes place, the interrupt request flag will be recorded but the acknowledge signal will be inhibited. When the Stack Pointer is decremented, by RET or RETI, the interrupt will be serviced. This feature prevents stack overflow allowing the programmer to use the structure more easily. However, when the stack is full, a CALL subroutine instruction can still be executed which will result in a stack overflow. Precautions should be taken to avoid such cases which might cause unpredictable program branching.

If the stack is overflow, the first Program Counter save in the stack will be lost.



Device	Stack Levels
HT66FB540/HT66FB550	8
HT66FB560	12

Arithmetic and Logic Unit – ALU

The arithmetic-logic unit or ALU is a critical area of the microcontroller that carries out arithmetic and logic operations of the instruction set. Connected to the main microcontroller data bus, the ALU receives related instruction codes and performs the required arithmetic or logical operations after which the result will be placed in the specified register. As these ALU calculation or operations may result in carry, borrow or other status changes, the status register will be correspondingly updated to reflect these changes. The ALU supports the following functions:

- Arithmetic operations: ADD, ADDM, ADC, ADCM, SUB, SUBM, SBC, SBCM, DAA
- Logic operations: AND, OR, XOR, ANDM, ORM, XORM, CPL, CPLA
- Rotation RRA, RR, RRCA, RRC, RLA, RL, RLCA, RLC
- Increment and Decrement INCA, INC, DECA, DEC
- Branch decision, JMP, SZ, SZA, SNZ, SIZ, SDZ, SIZA, SDZA, CALL, RET, RETI

Flash Program Memory

The Program Memory is the location where the user code or program is stored. For these devices series the Program Memory are Flash type, which means it can be programmed and re-programmed a large number of times, allowing the user the convenience of code modification on the same device. By using the appropriate programming tools, these Flash devices offer users the flexibility to conveniently debug and develop their applications while also offering a means of field programming and updating.

Structure

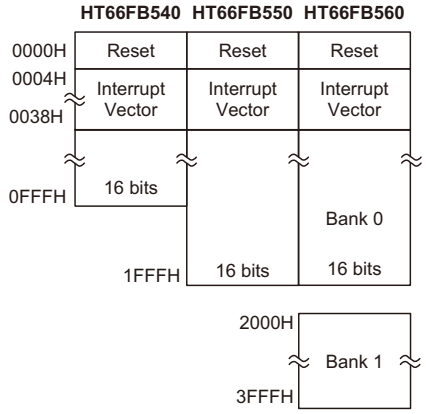
The Program Memory has a capacity of 4K×16 bits to 16K×16 bits. The Program Memory is addressed by the Program Counter and also contains data, table information and interrupt entries. Table data, which can be setup in any location within the Program Memory, is addressed by a separate table pointer register.

Device	Capacity	Banks
HT66FB540	4K×16	0
HT66FB550	8K×16	0
HT66FB560	16K×16	0, 1

The HT66FB560 has its Program Memory divided into two Banks, Bank 0 and Bank 1. The required Bank is selected using Bit 5 of the BP Register.

Special Vectors

Within the Program Memory, certain locations are reserved for the reset and interrupts. The location 000H is reserved for use by these devices reset for program initialisation. After a device reset is initiated, the program will jump to this location and begin execution.



Program Memory Structure

Look-up Table

Any location within the Program Memory can be defined as a look-up table where programmers can store fixed data. To use the look-up table, the table pointer must first be setup by placing the address of the look up data to be retrieved in the table pointer register, TBLP and TBHP. These registers define the total address of the look-up table.

After setting up the table pointer, the table data can be retrieved from the Program Memory using the "TABRD [m]" or "TABRDL [m]" instructions, respectively. When the instruction is executed, the lower order table byte from the Program Memory will be transferred to the user defined Data Memory register [m] as specified in the instruction. The higher order table data byte from the Program Memory will be transferred to the TBLH special register. Any unused bits in this transferred higher order byte will be read as “0”.

The accompanying diagram illustrates the addressing data flow of the look-up table.

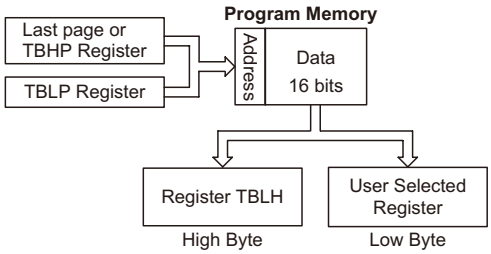


Table Program Example

The following example shows how the table pointer and table data is defined and retrieved from the microcontroller. This example uses raw table data located in the Program Memory which is stored there using the ORG statement. The value at this ORG statement is "1F00H" which refers to the start address of the last page within the 8K Program Memory of the HT66FB550. The table pointer is setup here to have an initial value of "06H". This will ensure that the first data read from the data table will be at the Program Memory address "1F06H" or 6 locations after the start of the last page. Note that the value for the table pointer is referenced to the first address of the present page if the "TABRD [m]" instruction is being used. The high byte of the table data which in this case is equal to zero will be transferred to the TBLH register automatically when the "TABRD [m]" instruction is executed.

Because the TBLH register is a read-only register and cannot be restored, care should be taken to ensure its protection if both the main routine and Interrupt Service Routine use table read instructions. If using the table read instructions, the Interrupt Service Routines may change the value of the TBLH and subsequently cause errors if used again by the main routine. As a rule it is recommended that simultaneous use of the table read instructions should be avoided. However, in situations where simultaneous use cannot be avoided, the interrupts should be disabled prior to the execution of any main routine table-read instructions. Note that all table related instructions require two instruction cycles to complete their operation.

Partial Lock

The flash program partial lock function is used to protect a block of Program Memory. The flash program memory is divided into several blocks according to the program size. Each block size is assigned by 512 words. The partial lock function is enabled by the partial lock configuration options. If the selected partial lock configuration option is selected, the corresponding partial lock function will be enabled and this block of program memory is unable to be accessed. Any read operations will result in a value of "0000h". In this way, the user can select which block of the flash memory is to be protected.

Precautions should be taken when using the Look-up table function in any locked blocks. The Look-up table pointer is implemented by the TBLP and TBHP registers. When the table pointer is setup to point to an address in an unlocked block, the table read instruction functions normally however when the pointer points to a locked block, there are two conditions:

1. If the table read instruction and the data table are located in the same block, then the table read instruction, TABRD [m], is valid.
2. If the table read instruction and the data table are located in different blocks, then the table read instruction is invalid. The read out data will be "0000h".

The following example illustrates the basic operation of the partial lock function using the HT66FB540 as an example.

If the last block is locked and if the table pointer address is setup to point to the last block, then if the table read instruction is executed in the last block, the data read back is valid. If the last block is locked, but the table pointer address points to the last page in other blocks, then when the table read instruction is executed, the read out data will be "0000h".

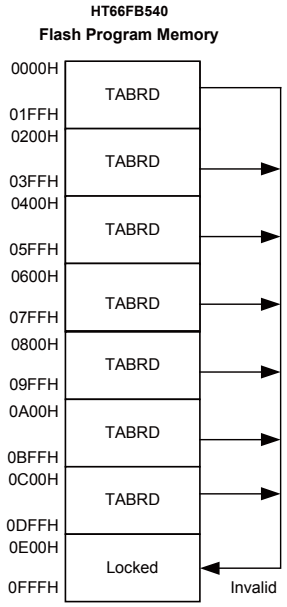


Table Read from different block

The above example has the following setups:

1. Enable the last page partial lock function via the configuration option.
2. Write data "0F00H" to the Table Pointer Registers, TBHP and TBLP.
3. Table read instruction not located in locked block.
4. Action: Table read is invalid – data read back as 000H.

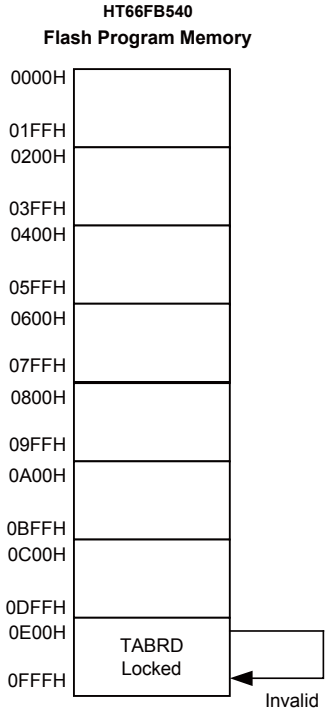


Table Read from same block

The above example has the following setups:

1. Enable the last page partial lock function via the configuration option.
2. Write data "0F00H" to the Table Pointer Registers, TBHP and TBLP.
3. Table read instruction is located in locked block.
4. Action: Table read instruction is valid.

In System Programming – ISP

The provision of Flash type Program Memory provides the user with a means of convenient and easy upgrades and modifications to their programs on the same device. As an additional convenience, Holtek has provided a means of programming the microcontroller in-system using a two-line USB interface. This provides manufacturers with the possibility of manufacturing their circuit boards complete with a programmed or un-programmed microcontroller, and then programming or upgrading the program at a later stage. This enables product manufacturers to easily keep their manufactured products supplied with the latest program releases without removal and re-insertion of the devices.

The Program Memory can be programmed serially in-system using the USB interface, namely using the UDN and UDP pins. The power is supplied by the UBUS pin. The technical details regarding the in-system programming of these devices are beyond the scope of this document and will be supplied in supplementary literature. The Flash Program Memory Read/Write function is implemented using a series of registers.

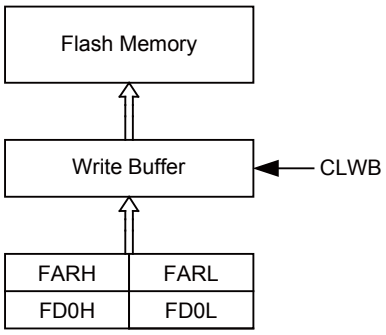
Flash Memory Read/Write Page Size

There are two page sizes, 32 words or 64 words, assigned for various Flash memory size. When the Flash memory, larger than 8K bytes, is selected, the 64 word page size is assigned per page and buffer. Otherwise, the page and buffer size are assigned as 32 words.

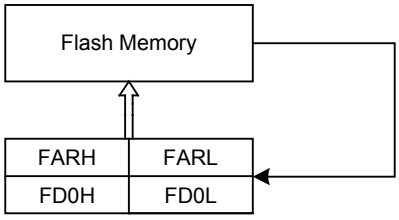
The following diagram illustrates the Read/Write page and buffer assignment. The write buffer is controlled by the CLWB bit in the FRCR register. The CLWB bit can be set high to enable the Clear Write Buffer procedure, as the procedure is finished, this bit will be cleared to low by hardware.

The Write Buffer is filled when the FWEN bit is set to high, when this bit is set high, the data in the Write buffer will be written to the Flash ROM, the FWT bit is used to indicate the writing procedure. Setting this bit high and check if the write procedure is finished, this bit will be cleared by hardware. The Read Byte can be assigned by the address. The FDEN is used to enable the read function and the FRD is used to indicate the reading procedure. When the reading procedure is finished, this bit will be cleared by hardware.

Device	Page size (words)	Write Buffer(Words)
HT66FB540(4K×16)	32	32
HT66FB550(8K×16)	32	32
HT66FB560(16K×16)	64	64



Write one word to FD0L/FD0H



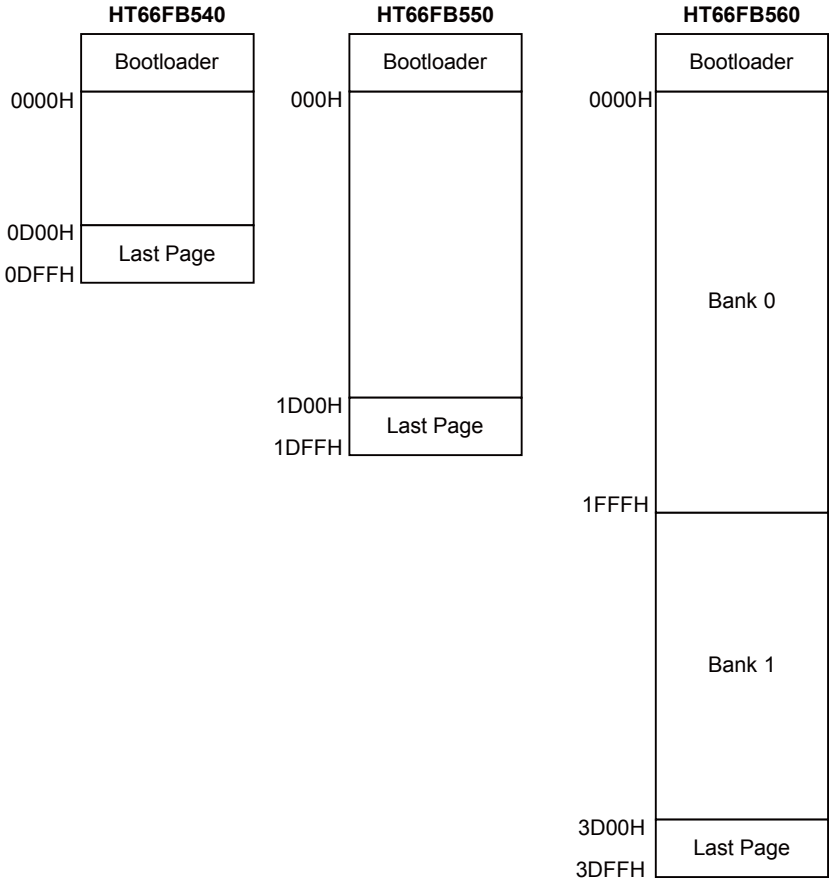
Read one word to FD0L/FD0H

Note: 1. Writing a data into high byte, which means the H/L Data is written into Write Buffer, will cause the Flash memory address increased by one automatically and the new address will be loaded to the FARH and FARL registers. However, the user can also fill the new address by filling the data into FARH and FARL registers in the same page, then the data will be written into the corresponding address.

2. If the address already reached the boundary of the flash memory, such as 11111b of the 32 words or 111111b of the 64 words. At this moment, the address will not be increased and the address will stop at the last address of that page and the writing data is invalid.
3. At this point, the user has to set a new address again to fill a new data.
4. If the data is writing using the write buffer, the write buffer will be cleared by hardware automatically after the write procedure is ready in 2ms.
5. Fisrt time use the Write buffer or renew the data in the Write buffer, the user can use to Clear buffer bit (CLWB) to clear write buffer.

ISP Bootloader

The devices provide the ISP Bootloader function to upgrade the software in the Flash memory. The user can select to use the ISP Bootloader application software provided by Holtek IDE tool or to create his own Bootloader software. When the Holtek Bootloader software is selected, that will occupy 0.5K words area in the Flash memory. The accompanyimg diagram illustrates the Flash memory structure with Holtek Bootloader software.



Flash Memory Structure with Bootloader Software

Flash Program Memory Registers

There are two address registers, four 16-bit data registers and one control register. The control register is located in Bank1 and the other registers are located in Bank 0. Read and Write operations to the Flash memory are carried out in 16-bit data operations using the address and data registers and the control register. Several registers control the overall operation of the internal Flash Program Memory. The address registers are named FARL and FARH, the data registers are named FDnL and FDnH, and the single control register is named FCR. As the FARL and FDnL registers are located in Bank 0, they can be directly accessed in the same was as any other Special Function Register. The FARH, FDnH and FCR registers however, being located in Bank1, cannot be addressed directly and can only be read from or written to indirectly using the MP1 Memory Pointer and Indirect Addressing Register, IAR1.

Program Memory Register List

- **HT66FB540**

Name	Bit							
	7	6	5	4	3	2	1	0
FARL	D7	D6	D5	D4	D3	D2	D1	D0
FARH	—	—	—	—	D11	D10	D9	D8
FD0L	D7	D6	D5	D4	D3	D2	D1	D0
FD0H	D15	D14	D13	D12	D11	D10	D9	D8
FD1L	D7	D6	D5	D4	D3	D2	D1	D0
FD1H	D15	D14	D13	D12	D11	D10	D9	D8
FD2L	D7	D6	D5	D4	D3	D2	D1	D0
FD2H	D15	D14	D13	D12	D11	D10	D9	D8
FD3L	D7	D6	D5	D4	D3	D2	D1	D0
FD3H	D15	D14	D13	D12	D11	D10	D9	D8
FCR	CFWEN	FMOD2	FMOD1	FMOD0	BWT	FWT	FDEN	FRD
FRCR	—	—	—	FSWRST	—	—	—	CLWB

- **HT66FB550**

Name	Bit							
	7	6	5	4	3	2	1	0
FARL	D7	D6	D5	D4	D3	D2	D1	D0
FARH	—	—	—	D12	D11	D10	D9	D8
FD0L	D7	D6	D5	D4	D3	D2	D1	D0
FD0H	D15	D14	D13	D12	D11	D10	D9	D8
FD1L	D7	D6	D5	D4	D3	D2	D1	D0
FD1H	D15	D14	D13	D12	D11	D10	D9	D8
FD2L	D7	D6	D5	D4	D3	D2	D1	D0
FD2H	D15	D14	D13	D12	D11	D10	D9	D8
FD3L	D7	D6	D5	D4	D3	D2	D1	D0
FD3H	D15	D14	D13	D12	D11	D10	D9	D8
FCR	CFWEN	FMOD2	FMOD1	FMOD0	BWT	FWT	FDEN	FRD
FRCR	—	—	—	FSWRST	—	—	—	CLWB

- **HT66FB560**

Name	Bit							
	7	6	5	4	3	2	1	0
FARL	D7	D6	D5	D4	D3	D2	D1	D0
FARH	—	—	D13	D12	D11	D10	D9	D8
FD0L	D7	D6	D5	D4	D3	D2	D1	D0
FD0H	D15	D14	D13	D12	D11	D10	D9	D8
FD1L	D7	D6	D5	D4	D3	D2	D1	D0
FD1H	D15	D14	D13	D12	D11	D10	D9	D8
FD2L	D7	D6	D5	D4	D3	D2	D1	D0
FD2H	D15	D14	D13	D12	D11	D10	D9	D8
FD3L	D7	D6	D5	D4	D3	D2	D1	D0
FD3H	D15	D14	D13	D12	D11	D10	D9	D8
FCR	CFWEN	FMOD2	FMOD1	FMOD0	BWT	FWT	FDEN	FRD
FRCR	—	—	—	FSWRST	—	—	—	CLWB

FARL Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x" unknown

Bit 7~0 Flash Program Memory address
Flash Program Memory address bit 7~bit 0

FARH Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	D11	D10	D9	D8
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	—	—	—	—	x	x	x	x

"x" unknown

Bit 7~4 Reserved, cannot be used

Bit 3~0 Flash Program Memory address
Flash Program Memory address bit 11~bit 8

- **HT66FB550**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	D12	D11	D10	D9	D8
R/W	—	—	—	R/W	R/W	R/W	R/W	R/W
POR	—	—	—	x	x	x	x	x

"x" unknown

Bit 7~5 Reserved, cannot be used

Bit 4~0 Flash Program Memory address
Flash Program Memory address bit 12~bit 8

- **HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	—	—	D13	D12	D11	D10	D9	D8
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	x	x	x	x	x	x

"x" unknown

Bit 7~6 Reserved, cannot be use

Bit 5~0 Flash Program Memory address
Flash Program Memory address bit 13~bit 8

FCR Register

Bit	7	6	5	4	3	2	1	0
Name	CFWEN	FMOD2	FMOD1	FMOD0	BWT	FWT	FRDEN	FRD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **CFWEN:** Flash ROM Write Enable bit, FWEN, control bit
0: Disable
1: Unimplemented
This bit is used to control the FWEN bit enable or disable. When this bit is cleared to low by software, the Flash memory write enable control bit, FWEN, will be cleared to low as well. It's ineffective to set this bit to high. The user can check this bit to confirm the FWEN status.

Bit 6~4 **FMOD2~FMOD0:** Flash Program memory, Configuration option memory operating mode control bits
000: write memory mode
001: Page erase mode
010: Reserved
011: Read memory mode
100: Reserved
101: Reserved
110: FWEN (Flash memory write enable) bit control mode
111: Reserved

Bit 3 **BWT:** Mode change control
0: Mode change cycle has finished
1: Activate a mode change cycle
This bit will be automatically reset to zero by the hardware after the mode change cycle has finished.

Bit 2 **FWT:** Flash memory Write Control
0: Write cycle has finished
1: Activate a write cycle
This is the Flash memory Write Control Bit and when set high by the application program will activate a write cycle. This bit will be automatically reset to zero by the hardware after the write cycle has finished.

Bit 1 **FRDEN:** Flash Memory Read Enable
0: Disable
1: Enable
This is the Flash memory Read Enable Bit which must be set high before Flash memory read operations are carried out. Clearing this bit to zero will inhibit Flash memory read operations.

Bit 0 **FRD:** Flash memory Read Control
0: Read cycle has finished
1: Activate a read cycle
This is the Flash memory Read Control Bit and when set high by the application program will activate a read cycle. This bit will be automatically reset to zero by the hardware after the read cycle has finished. Setting this bit high will have no effect if the RDEN has not first been set high.

Note: The FWT, FRDEN and FRD registers can not be set to "1" at the same time with a single instruction.

FRCR Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	FSWRST	—	—	—	CLWB
R/W	—	—	—	R/W	—	—	—	R/W
POR	—	—	—	0	—	—	—	0

Bit 7~5 Unimplemented

Bit 4 **FSWRST:** control bit
Must be to 0

Bit 3~1 Unimplemented

Bit 0 **CLWB:** Flash Program memory Write buffer clear control bit
0: Do not initiate clear Write Buffer or clear process
1: Initiate clear Write Buffer process
This bit is used to control the Flash Program memory clear Write buffer process. It will be set by software and cleared by hardware.

In Application Programming – IAP

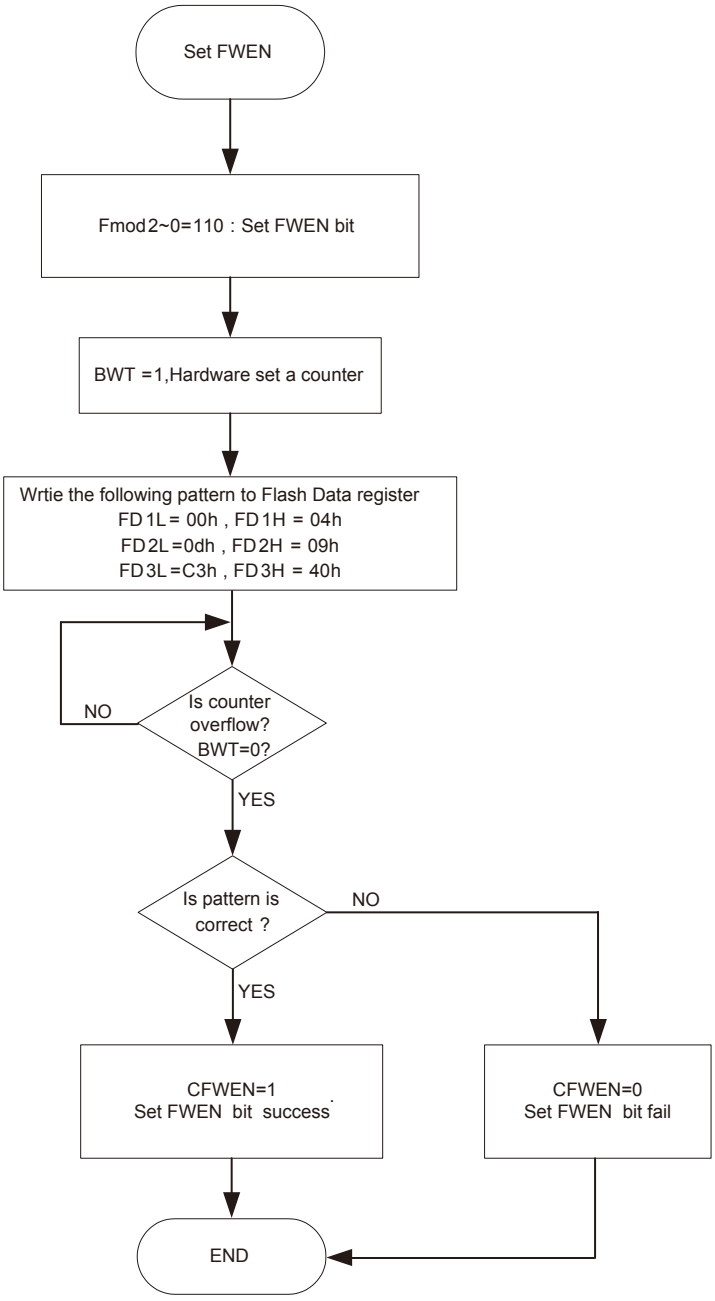
Offering users the convenience of Flash Memory multi-programming features, the HT66FB5x0 series of devices not only provide an ISP function, but also an additional IAP function. The convenience of the IAP function is that it can execute the updated program procedure using its internal firmware, without requiring an external Program Writer or PC. In addition, the IAP interface can also be any type of communication protocol, such as UART or USB, using I/O pins. Designers can assign I/O pins to communicate with the external memory device, including the updated program. Regarding the internal firmware, the user can select versions provided by HOLTEK or create their own. The following section illustrates the procedures regarding how to implement IAP firmware.

Enable Flash Write Control Procedure

The first procedure to implement the IAP firmware is to enable the Flash Write control which includes the following steps.

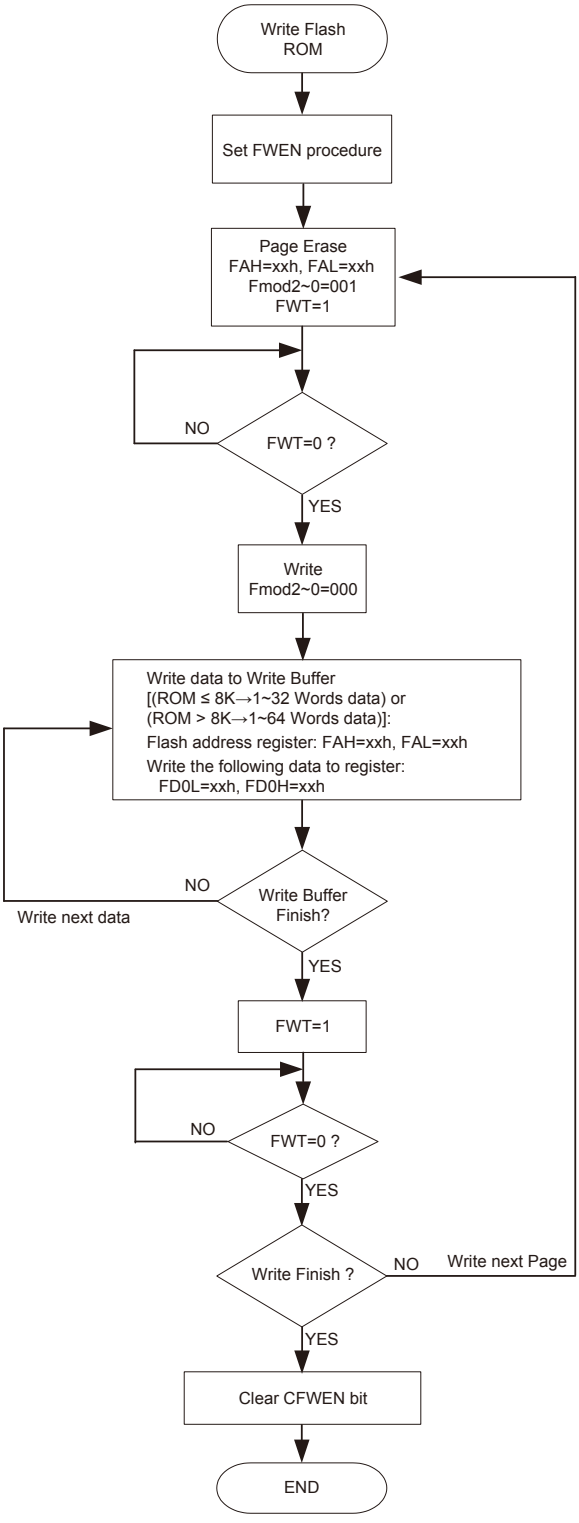
- Write data “110” to the Fmod [2:0] bits in the FCR register to enable the Flash write control bit, FWEN.
- Set the BWT bit in the FCR register to “1”.
- These devices will start a 300μs counter. The user should write the correct data pattern into the Flash data registers, namely FD1L~FD3L and FD1H~FD3H, during this period of time.
- Once the 300μs counter has overflowed or if the written pattern is incorrect, the enable Flash write control procedure will be invalid and the user should repeat the above procedure.
- No matter whether the procedure is valid or not, the devices will clear the BWT bit automatically.

- The enable Flash write pattern data is (00H, 04H, 0DH, 09H, C3H, 40H) and it should be written into the Flash data registers.
- Once the Flash write operation is enabled, the user can update the Flash memory using the Flash control registers.
- To disable the Flash write procedure, the user can only clear the CFWEN bit in the FCR register. There is no need to execute the above procedure.

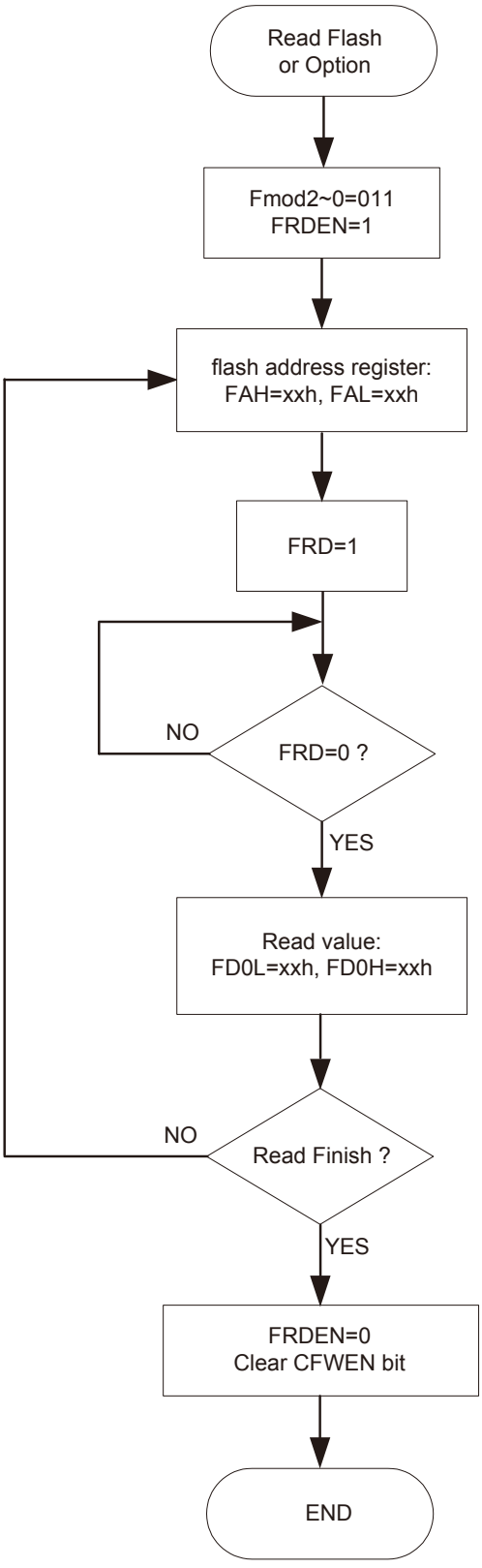


Flash Memory Write and Read Procedures

The following flow charts illustrate the Write and Read Flash memory procedures.



Write Flash Program ROM Procedure



Read Flash Program Procedure

In Circuit Programming – ICP

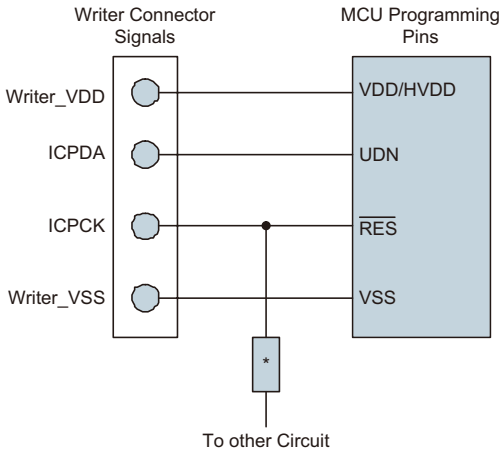
The provision of Flash type Program Memory provides the user with a means of convenient and easy upgrades and modifications to their programs on the same device.

As an additional convenience, Holtek has provided a means of programming the microcontroller in-circuit using a 4-pin interface. This provides manufacturers with the possibility of manufacturing their circuit boards complete with a programmed or un-programmed microcontroller, and then programming or upgrading the program at a later stage. This enables product manufacturers to easily keep their manufactured products supplied with the latest program releases without removal and re-insertion of the device.

Holtek Writer Pins	MCU Programming Pins	Pin Description
ICPDA	UDN	Programming Serial Data
ICPCK	$\overline{RES}$	Programming Clock
VDD	VDD/HVDD	Power Supply
VSS	VSS	Ground

The Program Memory can be programmed serially in-circuit using this 4-wire interface. Data is downloaded and uploaded serially on a single pin with an additional line for the clock. Two additional lines are required for the power supply and one line for the reset. The technical details regarding the in-circuit programming of the devices are beyond the scope of this document and will be supplied in supplementary literature.

During the programming process, taking control of the UDN and $\overline{RES}$ pins for data and clock programming purposes. The user must there take care to ensure that no other outputs are connected to these two pins.



Note: * may be resistor or capacitor. The resistance of * must be greater than 300Ω or the capacitance of * must be less than 1nF.

On-Chip Debug Support – OCDS

There is an EV chip named HT66VB540/HT66VB550/HT66VB560 which is used to emulate the HT66FB540/HT66FB550/HT66FB560 device. The HT66VB540/HT66VB550/HT66VB560 device also provides the "On-Chip Debug" function to debug the HT66FB540/HT66FB550/HT66FB560 device during development process. The two devices, HT66FB540/HT66FB550/HT66FB560 and HT66VB540/HT66VB550/HT66VB560, are almost functional compatible except the "On-Chip Debug" function. Users can use the HT66VB540/HT66VB550/HT66VB560 device to emulate the HT66FB540/HT66FB550/HT66FB560 device behaviors by connecting the OCDSDA and OCDSCK

pins to the Holtek HT-IDE development tools. The OCDSDA pin is the OCDS Data/Address input/output pin while the OCDSCK pin is the OCDS clock input pin. When users use the HT66VB540/HT66VB550/HT66VB560 EV chip for debugging, the corresponding pin functions shared with the OCDSDA and OCDSCK pins in the HT66FB540/HT66FB550/HT66FB560 device will have no effect in the HT66VB540/HT66VB550/HT66VB560 EV chip. For more detailed OCDS information, refer to the corresponding document named "Holtek e-Link for 8-bit MCU OCDS User's Guide".

Holtek e-Link Pins	EV Chip Pins	Pin Description
OCDSDA	OCDSDA	On-Chip Debug Support Data/Address input/output
OCDSCK	OCDSCK	On-Chip Debug Support Clock input
VDD	VDD/HVDD	Power Supply
GND	VSS	Ground

RAM Data Memory

The Data Memory is a volatile area of 8-bit wide RAM internal memory and is the location where temporary information is stored.

Structure

Divided into two sections, the first of these is an area of RAM, known as the Special Function Data Memory. Here are located registers which are necessary for correct operation of the devices. Many of these registers can be read from and written to directly under program control, however, some remain protected from user manipulation.

Device	Capacity	Banks
HT66FB540	512×8	0: 80H~FFH 1: 80H~FFH 2: 80H~FFH 3: 80H~FFH
HT66FB550	768×8	0: 80H~FFH 1: 80H~FFH 2: 80H~FFH 3: 80H~FFH 4: 80H~FFH 5: 80H~FFH
HT66FB560	1024×8	0: 80H~FFH 1: 80H~FFH 2: 80H~FFH 3: 80H~FFH 4: 80H~FFH 5: 80H~FFH 6: 80H~FFH 7: 80H~FFH

The second area of Data Memory is known as the General Purpose Data Memory, which is reserved for general purpose use. All locations within this area are read and write accessible under program control.

The overall Data Memory is subdivided into several banks, the structure of which depends upon these devices chosen. The Special Purpose Data Memory registers are accessible in all banks, with the exception of the , FCR, FARH and FDnH registers at address from 40H to 46H, which are only accessible in Bank 1. Switching between the different Data Memory banks is achieved by setting the Bank Pointer to the correct value. The start address of the Data Memory for all devices is the address 00H.

HT66FB540

	BANK0~3		BANK0, 2~3	BANK1
00H	IAR0	40H	Unused	FRCR
01H	MP0	41H	Unused	FCR
02H	IAR1	42H	FARL	FARH
03H	MP1	43H	FD0L	FD0H
04H	BP	44H	FD1L	FD1H
05H	ACC	45H	FD2L	FD2H
06H	PCL	46H	FD3L	FD3H
07H	TBLP	47H	TMPC0	
08H	TBLH	48H	TMPC1	
09H	TBHP	49H	TM0C0	
0AH	STATUS	4AH	TM0C1	
0BH	SMOD	4BH	Unused	
0CH	LVDC	4CH	TM0DL	
0DH	INTEG	4DH	TM0DH	
0EH	WDTC	4EH	TM0AL	
0FH	TBC	4FH	TM0AH	
10H	INTC0	50H	TM0RP	
11H	INTC1	51H	Unused	
12H	INTC2	52H	TM1C0	
13H	INTC3	53H	TM1C1	
14H	MFI0	54H	TM1DL	
15H	MFI1	55H	TM1DH	
16H	MFI2	56H	TM1AL	
17H	Unused	57H	TM1AH	
18H	PAWU	58H	TM2C0	
19H	PAPU	59H	TM2C1	
1AH	PA	5AH	TM2DL	
1BH	PAC	5BH	TM2DH	
1CH	PADIR	5CH	TM2AL	
1DH	PAOI	5DH	TM2AH	
1EH	PSLEW	5EH	TM3C0	
1FH	PXWU	5FH	TM3C1	
20H	PXPU	60H	TM3DL	
21H	PXOI	61H	TM3DH	
22H	PB	62H	TM3AL	
23H	PBC	63H	TM3AH	
24H	Unused	64H	USB_STAT	
25H	Unused	65H	UINT	
26H	PD	66H	USC	
27H	PDC	67H	USR	
28H	PE	68H	UCC	
29H	PEC	69H	AWR	
2AH	Unused	6AH	STLI	
2BH	Unused	6BH	STLO	
2CH	Unused	6CH	SIES	
2DH	Unused	6DH	MISC	
2EH	Unused	6EH	UFIEN	
2FH	ADRL	6FH	UFOEN	
30H	ADRH	70H	UFC0	
31H	ADCR0	71H	Unused	
32H	ADCR1	72H	FIFO0	
33H	ACER0	73H	FIFO1	
34H	Unused	74H	FIFO2	
35H	CP0C	75H	FIFO3	
36H	CP1C	76H	Unused	
37H	I2CTOC	77H	Unused	
38H	SIMC0	78H	Unused	
39H	SIMC1	79H	Unused	
3AH	SIMD	7AH	CTRL	
3BH	SIMA/SIMC2	7BH	LVRC	
3CH	SPIAC0	7CH	Unused	
3DH	SPIAC1	7DH	PAPS0	
3EH	SPIAD	7EH	PAPS1	
3FH	SBSC	7FH	SYSC	

HT66FB540 Special Purpose Data Memory

HT66FB550

	BANK0~5		BANK0, 2~5	BANK1
00H	IAR0	40H	Unused	FRCR
01H	MP0	41H	Unused	FCR
02H	IAR1	42H	FARL	FARH
03H	MP1	43H	FD0L	FD0H
04H	BP	44H	FD1L	FD1H
05H	ACC	45H	FD2L	FD2H
06H	PCL	46H	FD3L	FD3H
07H	TBLP	47H	TMPC0	
08H	TBLH	48H	TMPC1	
09H	TBHP	49H	TM0C0	
0AH	STATUS	4AH	TM0C1	
0BH	SMOD	4BH	Unused	
0CH	LVDC	4CH	TM0DL	
0DH	INTEG	4DH	TM0DH	
0EH	WDTC	4EH	TM0AL	
0FH	TBC	4FH	TM0AH	
10H	INTC0	50H	TM0RP	
11H	INTC1	51H	Unused	
12H	INTC2	52H	TM1C0	
13H	INTC3	53H	TM1C1	
14H	MFI0	54H	TM1DL	
15H	MFI1	55H	TM1DH	
16H	MFI2	56H	TM1AL	
17H	Unused	57H	TM1AH	
18H	PAWU	58H	TM2C0	
19H	PAPU	59H	TM2C1	
1AH	PA	5AH	TM2DL	
1BH	PAC	5BH	TM2DH	
1CH	PADIR	5CH	TM2AL	
1DH	PAOI	5DH	TM2AH	
1EH	PSLEW	5EH	TM3C0	
1FH	PXWU	5FH	TM3C1	
20H	PXPU	60H	TM3DL	
21H	PXOI	61H	TM3DH	
22H	PB	62H	TM3AL	
23H	PBC	63H	TM3AH	
24H	PC	64H	USB_STAT	
25H	PCC	65H	UINT	
26H	PD	66H	USC	
27H	PDC	67H	USR	
28H	PE	68H	UCC	
29H	PEC	69H	AWR	
2AH	Unused	6AH	STLI	
2BH	Unused	6BH	STLO	
2CH	Unused	6CH	SIES	
2DH	Unused	6DH	MISC	
2EH	Unused	6EH	UFIEN	
2FH	ADRL	6FH	UFOEN	
30H	ADRH	70H	UFC0	
31H	ADCR0	71H	UFC1	
32H	ADCR1	72H	FIFO0	
33H	ACER0	73H	FIFO1	
34H	ACER1	74H	FIFO2	
35H	CP0C	75H	FIFO3	
36H	CP1C	76H	FIFO4	
37H	I2CTOC	77H	FIFO5	
38H	SIMC0	78H	Unused	
39H	SIMC1	79H	Unused	
3AH	SIMD	7AH	CTRL	
3BH	SIMA/SIMC2	7BH	LVRC	
3CH	SPIAC0	7CH	Unused	
3DH	SPIAC1	7DH	PAPS0	
3EH	SPIAD	7EH	PAPS1	
3FH	SBSC	7FH	SYSC	

HT66FB550 Special Purpose Data Memory

HT66FB560

	BANK0~7		BANK0, 2~7	BANK1
00H	IAR0	40H	Unused	FRCR
01H	MP0	41H	Unused	FCR
02H	IAR1	42H	FARL	FARH
03H	MP1	43H	FD0L	FD0H
04H	BP	44H	FD1L	FD1H
05H	ACC	45H	FD2L	FD2H
06H	PCL	46H	FD3L	FD3H
07H	TBLP	47H	TMPC0	
08H	TBLH	48H	TMPC1	
09H	TBHP	49H	TM0C0	
0AH	STATUS	4AH	TM0C1	
0BH	SMOD	4BH	Unused	
0CH	LVDC	4CH	TM0DL	
0DH	INTEG	4DH	TM0DH	
0EH	WDTC	4EH	TM0AL	
0FH	TBC	4FH	TM0AH	
10H	INTC0	50H	TM0RP	
11H	INTC1	51H	Unused	
12H	INTC2	52H	TM1C0	
13H	INTC3	53H	TM1C1	
14H	MFI0	54H	TM1DL	
15H	MFI1	55H	TM1DH	
16H	MFI2	56H	TM1AL	
17H	Unused	57H	TM1AH	
18H	PAWU	58H	TM2C0	
19H	PAPU	59H	TM2C1	
1AH	PA	5AH	TM2DL	
1BH	PAC	5BH	TM2DH	
1CH	PADIR	5CH	TM2AL	
1DH	PAOI	5DH	TM2AH	
1EH	PSLEW	5EH	TM3C0	
1FH	PXWU	5FH	TM3C1	
20H	PXPU	60H	TM3DL	
21H	PXOI	61H	TM3DH	
22H	PB	62H	TM3AL	
23H	PBC	63H	TM3AH	
24H	PC	64H	USB_STAT	
25H	PCC	65H	UINT	
26H	PD	66H	USC	
27H	PDC	67H	USR	
28H	PE	68H	UCC	
29H	PEC	69H	AWR	
2AH	PF	6AH	STLI	
2BH	PFC	6BH	STLO	
2CH	PFPU	6CH	SIES	
2DH	PFWKUP	6DH	MISC	
2EH	Unused	6EH	UFIEN	
2FH	ADRL	6FH	UFOEN	
30H	ADRH	70H	UFC0	
31H	ADCR0	71H	UFC1	
32H	ADCR1	72H	FIFO0	
33H	ACER0	73H	FIFO1	
34H	ACER1	74H	FIFO2	
35H	CP0C	75H	FIFO3	
36H	CP1C	76H	FIFO4	
37H	I2CTOC	77H	FIFO5	
38H	SIMC0	78H	FIFO6	
39H	SIMC1	79H	FIFO7	
3AH	SIMD	7AH	CTRL	
3BH	SIMA/SIMC2	7BH	LVRC	
3CH	SPIAC0	7CH	Unused	
3DH	SPIAC1	7DH	PAPS0	
3EH	SPIAD	7EH	PAPS1	
3FH	SBSC	7FH	SYSC	

HT66FB560 Special Purpose Data Memory

Special Function Register Description

Most of the Special Function Register details will be described in the relevant functional section; however several registers require a separate description in this section.

Indirect Addressing Registers – IAR0, IAR1

The Indirect Addressing Registers, IAR0 and IAR1, although having their locations in normal RAM register space, do not actually physically exist as normal registers. The method of indirect addressing for RAM data manipulation uses these Indirect Addressing Registers and Memory Pointers, in contrast to direct memory addressing, where the actual memory address is specified. Actions on the IAR0 and IAR1 registers will result in no actual read or write operation to these registers but rather to the memory location specified by their corresponding Memory Pointers, MP0 or MP1. Acting as a pair, IAR0 and MP0 can together access data from Bank 0 while the IAR1 and MP1 register pair can access data from any bank. As the Indirect Addressing Registers are not physically implemented, reading the Indirect Addressing Registers indirectly will return a result of "00H" and writing to the registers indirectly will result in no operation.

Memory Pointers – MP0, MP1

Two Memory Pointers, known as MP0 and MP1 are provided. These Memory Pointers are physically implemented in the Data Memory and can be manipulated in the same way as normal registers providing a convenient way with which to address and track data. When any operation to the relevant Indirect Addressing Registers is carried out, the actual address that the microcontroller is directed to, is the address specified by the related Memory Pointer. MP0, together with Indirect Addressing Register, IAR0, are used to access data from Bank 0, while MP1 and IAR1 are used to access data from all banks according to BP register. Direct Addressing can only be used with Bank 0, all other Banks must be addressed indirectly using MP1 and IAR1.

The following example shows how to clear a section of four Data Memory locations already defined as locations adres1 to adres4.

Indirect Addressing Program Example

```
data .section data
adres1   db ?
adres2   db ?
adres3   db ?
adres4   db ?
block    db ?
code .section at 0 code
org  00h

start:
     mov a,04h              ; setup size of block
     mov block,a
     mov a,offset adres1    ; Accumulator loaded with first RAM address
     mov mp0,a              ; setup memory pointer with first RAM address
loop:
     clr IAR0               ; clear the data at address defined by MP0
     inc mp0                ; increment memory pointer
     sdz block              ; check if last memory location has been cleared
     jmp loop
continue:
```

The important point to note here is that in the example shown above, no reference is made to specific RAM addresses.

Bank Pointer – BP

Depending upon which devices are used, the Program and Data Memory are divided into several banks. Selecting the required Program and Data Memory area is achieved using the Bank Pointer. Bit 5 of the Bank Pointer is used to select Program Memory Bank 0 or 1, while bits 0~2 are used to select Data Memory Banks 0~6.

The Data Memory is initialised to Bank 0 after a reset, except for a WDT time-out reset in the Power Down Mode, in which case, the Data Memory bank remains unaffected. It should be noted that the Special Function Data Memory is not affected by the bank selection, which means that the Special Function Registers can be accessed from within any bank. Directly addressing the Data Memory will always result in Bank 0 being accessed irrespective of the value of the Bank Pointer. Accessing data from banks other than Bank 0 must be implemented using Indirect addressing.

As both the Program Memory and Data Memory share the same Bank Pointer Register, care must be taken during programming.

Device	Bit							
	7	6	5	4	3	2	1	0
HT66FB540	—	—	—	—	—	—	DMBP1	DMBP0
HT66FB550	—	—	—	—	—	DMBP2	DMBP1	DMBP0
HT66FB560	—	—	PMBP0	—	—	DMBP2	DMBP1	DMBP0

BP Registers List

BP Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	DMBP1	DMBP0
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	0

Bit 7~3 Unimplemented

Bit 1~0 **DMBP1, DMBP0:** Select Data Memory Banks
00: Bank 0
01: Bank 1
10: Bank 2
11: Bank 3

- **HT66FB550**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	DMBP2	DMBP1	DMBP0
R/W	—	—	—	—	—	R/W	R/W	R/W
POR	—	—	—	—	—	0	0	0

Bit 7~3 Unimplemented

Bit 1~0 **DMBP2, DMBP1, DMBP0:** Select Data Memory Banks
000: Bank 0
001: Bank 1
010: Bank 2
011: Bank 3
100: Bank 4
101: Bank 5
110~111: Undefined

• **HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	—	—	PMBP0	—	—	DMBP2	DMBP1	DMBP0
R/W	—	—	R/W	—	—	R/W	R/W	R/W
POR	—	—	0	—	—	0	0	0

Bit 7~6 Unimplemented

Bit 5 **PMBP0:** Select Program Memory Banks
0: Bank 0, Program Memory Address is from 0000H~1FFFH
1: Bank 1, Program Memory Address is from 2000H~3FFFH

Bit 4~3 Unimplemented

Bit 2~0 **DMBP2~DMBP0:** Select Data Memory Banks
000: Bank 0
001: Bank 1
010: Bank 2
011: Bank 3
100: Bank 4
101: Bank 5
110: Bank 6
111: Bank 7

Accumulator – ACC

The Accumulator is central to the operation of any microcontroller and is closely related with operations carried out by the ALU. The Accumulator is the place where all intermediate results from the ALU are stored. Without the Accumulator it would be necessary to write the result of each calculation or logical operation such as addition, subtraction, shift, etc., to the Data Memory resulting in higher programming and timing overheads. Data transfer operations usually involve the temporary storage function of the Accumulator; for example, when transferring data between one user defined register and another, it is necessary to do this by passing the data through the Accumulator as no direct transfer between two registers is permitted.

Program Counter Low Register – PCL

To provide additional program control functions, the low byte of the Program Counter is made accessible to programmers by locating it within the Special Purpose area of the Data Memory. By manipulating this register, direct jumps to other program locations are easily implemented. Loading a value directly into this PCL register will cause a jump to the specified Program Memory location, however, as the register is only 8-bit wide, only jumps within the current Program Memory page are permitted. When such operations are used, note that a dummy cycle will be inserted.

Look-up Table Registers – TBLP, TBHP, TBLH

These three special function registers are used to control operation of the look-up table which is stored in the Program Memory. TBLP and TBHP are the table pointer and indicates the location where the table data is located. Their value must be setup before any table read commands are executed. Their value can be changed, for example using the “INC” or “DEC” instructions, allowing for easy table data pointing and reading. TBLH is the location where the high order byte of the table data is stored after a table read data instruction has been executed. Note that the lower order table data byte is transferred to a user defined location.

Status Register – STATUS

This 8-bit register contains the zero flag (Z), carry flag (C), auxiliary carry flag (AC), overflow flag (OV), power down flag (PDF), and watchdog time-out flag (TO). These arithmetic/logical operation and system management flags are used to record the status and operation of the microcontroller.

With the exception of the TO and PDF flags, bits in the status register can be altered by instructions like most other registers. Any data written into the status register will not change the TO or PDF flag. In addition, operations related to the status register may give different results due to the different instruction operations. The TO flag can be affected only by a system power-up, a WDT time-out or by executing the "CLR WDT" or "HALT" instruction. The PDF flag is affected only by executing the "HALT" or "CLR WDT" instruction or during a system power-up.

The Z, OV, AC and C flags generally reflect the status of the latest operations.

- **C** is set if an operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation; otherwise C is cleared. C is also affected by a rotate through carry instruction.
- **AC** is set if an operation results in a carry out of the low nibbles in addition, or no borrow from the high nibble into the low nibble in subtraction; otherwise AC is cleared.
- **Z** is set if the result of an arithmetic or logical operation is zero; otherwise Z is cleared.
- **OV** is set if an operation results in a carry into the highest-order bit but not a carry out of the highest-order bit, or vice versa; otherwise OV is cleared.
- **PDF** is cleared by a system power-up or executing the “CLR WDT” instruction. PDF is set by executing the “HALT” instruction.
- **TO** is cleared by a system power-up or executing the “CLR WDT” or “HALT” instruction. TO is set by a WDT time-out.

In addition, on entering an interrupt sequence or executing a subroutine call, the status register will not be pushed onto the stack automatically. If the contents of the status registers are important and if the subroutine can corrupt the status register, precautions must be taken to correctly save it.

STATUS Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	TO	PDF	OV	Z	AC	C
R/W	—	—	R	R	R/W	R/W	R/W	R/W
POR	—	—	0	0	x	x	x	x

" x" unknown

Bit 7, 6 Unimplemented, read as “0”

Bit 5 **TO:** Watchdog Time-Out flag
0: After power up or executing the “CLR WDT” or “HALT” instruction
1: A watchdog time-out occurred.

Bit 4 **PDF:** Power down flag
0: After power up or executing the “CLR WDT” instruction
1: By executing the “HALT” instruction

Bit 3 **OV:** Overflow flag
0: No overflow
1: An operation results in a carry into the highest-order bit but not a carry out of the highest-order bit or vice versa.

Bit 2 **Z:** Zero flag
0: The result of an arithmetic or logical operation is not zero
1: The result of an arithmetic or logical operation is zero

Bit 1 **AC:** Auxiliary flag
0: No auxiliary carry
1: An operation results in a carry out of the low nibbles in addition, or no borrow from the high nibble into the low nibble in subtraction

Bit 0 **C:** Carry flag
0: No carry-out
1: An operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation

C is also affected by a rotate through carry instruction.

Oscillator

Various oscillator options offer the user a wide range of functions according to their various application requirements. The flexible features of the oscillator functions ensure that the best optimisation can be achieved in terms of speed and power saving. Oscillator selections and operation are selected through a combination of configuration options and registers.

Oscillator Overview

In addition to being the source of the main system clock the oscillators also provide clock sources for the Watchdog Timer and Time Base Interrupts. External oscillators requiring some external components as well as fully integrated internal oscillators, requiring no external components, are provided to form a wide range of both fast and slow system oscillators. All oscillator options are selected through the configuration options. The higher frequency oscillators provide higher performance but carry with it the disadvantage of higher power requirements, while the opposite is of course true for the lower frequency oscillators. With the capability of dynamically switching between fast and slow system clock, these devices have the flexibility to optimize the performance/power ratio, a feature especially important in power sensitive portable applications.

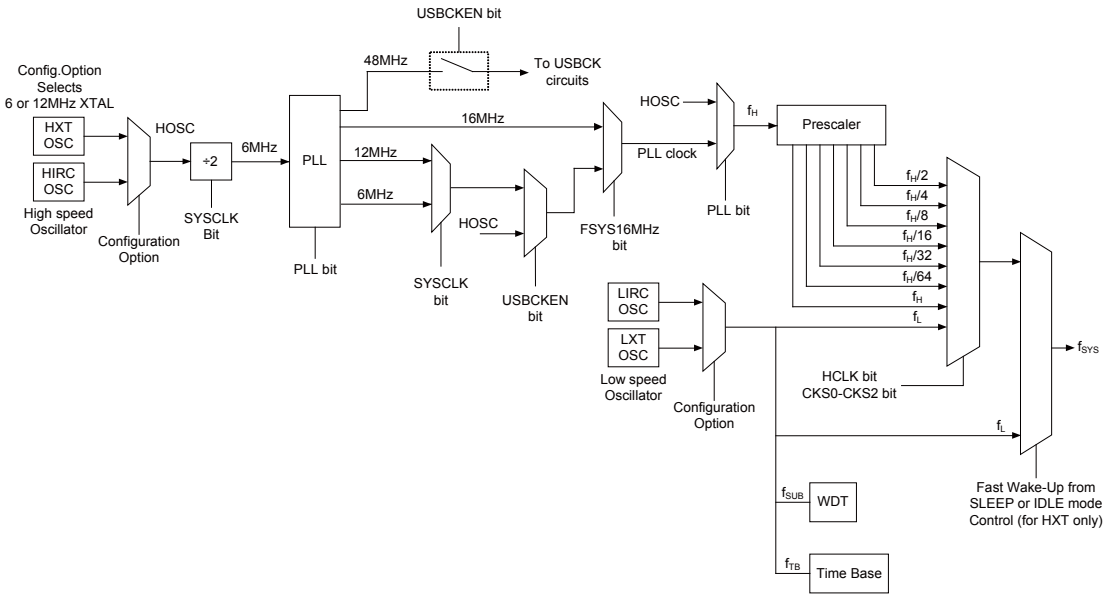
Type	Name	Frequency	Pins
External Crystal	HXT	6MHz or 12MHz	OSC1/OSC2
Internal High Speed RC	HIRC	12MHz	—
External Low Speed Crystal	LXT	32.768kHz	XT1/XT2
Internal Low Speed RC	LIRC	32kHz	—

Oscillator Types

Note: For USB applications, HXT must be connected a 6MHz or 12MHz crystal.

System Clock Configurations

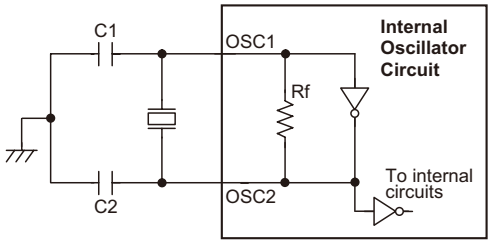
There are several oscillator sources, two high speed oscillators and two low speed oscillators. The high speed system clocks are sourced from the external crystal/ceramic oscillator, the PLL frequency generator and the internal 12MHz RC oscillator. The two low speed oscillators are the internal 32kHz RC oscillator and the external 32.768kHz crystal oscillator. Selecting whether the low or high speed oscillator is used as the system oscillator is implemented using the HLCLK bit and CKS2~CKS0 bits in the SMOD register and as the system clock can be dynamically selected. The actual source clock used for each of the high speed and low speed oscillators is chosen via configuration options. The frequency of the slow speed or high speed system clock is also determined using the HLCLK bit and CKS2~CKS0 bits in the SMOD register. Note that two oscillator selections must be made namely one high speed and one low speed system oscillators. It is not possible to choose a no-oscillator selection for either the high or low speed oscillator. In addition, the internal PLL frequency generator, whose clock source is supplied by an external crystal oscillator, can be enabled by a software control bit to generate various frequencies for the USB interface and system clock.



System Clock Configurations

External Crystal Oscillator – HXT

The External Crystal System Oscillator is one of the high frequency oscillator.



Note: 1. Rp is normally not required. C1 and C2 are required.
2. Although not shown OSC1/OSC2 pins have a parasitic capacitance of around 7pF.

Crystal Oscillator – HXT

Crystal Oscillator C1 and C2 Values		
Crystal Frequency	**C1**	**C2**
16MHz	0pF	0pF
12MHz	0pF	0pF
8MHz	0pF	0pF
6MHz	0pF	0pF
4MHz	0pF	0pF
1MHz	100pF	100pF
Note: 1. C1 and C2 values are for guidance only.		

Crystal Recommended Capacitor Values

Note: For USB applications, HXT must be connected a 6MHz or 12MHz crystal.

Internal PLL Frequency Generator

The internal PLL frequency generator is used to generate the frequency for the USB interface and the system clock. This PLL generator can be enabled or disabled by the PLL control bit in the USC register. After a power on reset, the PLL control bit will be set to “0” to turn on the PLL generator. The PLL generator will provide the fixed 48MHz frequency for the USB operating frequency and another frequency for the system clock source which can be either 6MHz, 12MHz or 16MHz. The selection of this system frequency is implemented using the SYSCLK, Fsys16MHZ and USBCKEN bits in the UCC register. In addition, the system clock can be selected as the HXT via these control bits. The CLK_ADJ bit is used to adjust the PLL clock automatically.

SYSC Register

Bit	7	6	5	4	3	2	1	0
Name	CLK_ADJ	USBdis	RUBUS	—	—	HFV	—	—
R/W	R/W	R/W	R/W	—	—	R/W	—	—
POR	0	0	0	—	—	0	—	—

Bit 7 **CLK_ADJ:** PLL Clock Automatic Adjustment function
0: Disable
1: Enable
Note that if the user selects the HIRC as the system clock, the CLK_ADJ bit must be set to “1” to adjust the PLL frequency automatically.

Bit 6 **USBdis:** USB SIE control bit
USB related control bit, described elsewhere

Bit 5 **RUBUS:** UBUS pin pull low resistor
USB related control bit, described elsewhere

Bit 4~3 "—": unimplemented, read as "0"

Bit 2 **HFV**: Non-USB mode high frequency voltage control
0: For USB mode - bit must be cleared to zero.
1: For non-USB mode - bit must be set high. Ensures that the higher frequency can work at lower voltages.
A higher frequency is >8MHz and is used for the system clock f_H.

Bit 1~0 "—": unimplemented, read as "0"

UCC Register

Bit	7	6	5	4	3	2	1	0
Name	Rctrl	SYSCLK	Fsys16MHz	SUSP2	USBCKEN	—	EPS1	EPS0
R/W	R/W	R/W	R/W	R/W	R/W	—	R/W	R/W
POR	0	0	0	0	0	—	0	0

Bit 7 **Rctrl:** 7.5kΩ resistor between UDP and Ubus control bit
USB related control bit, described elsewhere

Bit 6 **SYSCLK:** System clock frequency select bit
0: 12MHz
1: 6MHz
Note: If a 6MHz crystal or resonator is used for the MCU, this bit should be set to "1".
If a 12MHz crystal or resonator is used, then this bit should be set to "0".
If the 12MHz HIRC is selected, then this bit must be set to "0".

Bit 5 **Fsys16MHZ:** PLL 16MHz output control bit
0: HXT
1: PLL 16MHz

Bit 4 **SUSP2:** Reduce power consumption in suspend mode control bit
USB related control bit, described elsewhere

Bit 3 **USBCKEN:** USB clock control bit
0: Disable
1: Enable

Bit 2 Unimplemented

Bit 1~0 **EPS1, EPS0:** Accessing endpoint FIFO selection
USB related control bit, described elsewhere

USC Register

Bit	7	6	5	4	3	2	1	0
Name	URD	SELPS2	PLL	SELUSB	RESUME	URST	RMWK	SUSP
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R
POR	1	0	0	0	0	0	0	0

Bit 7 **URD:** USB reset signal control function definition
USB related control bit, described elsewhere

Bit 6 **SELPS2:** the chip works under PS2 mode indicator bit
USB related control bit, described elsewhere

Bit 5 **PLL:** PLL control bit
0: Turn-on PLL
1: Turn-off PLL

Bit 4 **SELUSB:** the chip works under USB mode indicator bit
USB related control bit, described elsewhere

Bit 3 **RESUME:** USB resume indication bit
USB related control bit, described elsewhere

Bit 2 **URST:** USB reset indication bit
USB related control bit, described elsewhere

Bit 1 **RMWK:** USB remote wake-up command
USB related control bit, described elsewhere

Bit 0 **SUSP:** USB suspend indication
USB related control bit, described elsewhere

The following table illustrates the PLL output frequency selected by the related control bits.

High frequency system clock f_H selection table:

PLL	USBCKEN	Fsys16MHz	f_H
0	0	0	HOSC (HXT or HIRC)
0	0	1	f_{PLL} – 16MHz
0	1	0	f_{PLL} – 6MHz or 12 MHz, depending on the “SYSCLK” bit in the UCC register selection
0	1	1	f_{PLL} – 16MHz
1	x	x	HOSC (HXT or HIRC)

x: stand for “don’t care”

Internal RC Oscillator – HIRC

The internal RC oscillator is a fully integrated system oscillator requiring no external components. The internal RC oscillator has a fixed frequency of 12MHz. Device trimming during the manufacturing process and the inclusion of internal frequency compensation circuits are used to ensure that the influence of the power supply voltage, temperature and process variations on the oscillation frequency are minimised. As a result, at a power supply of either 3.3V or 5V and at a temperature of 25°C degrees, the fixed oscillation frequency of 12MHz will have a tolerance within 3% (Non-USB mode). Note that if this internal system clock option is selected, as it requires no external pins for its operation, I/O pins PD0 and PD1 are free for use as normal I/O pins. The HIRC has its own power supply pin, HVDD. The HVDD pin must be connected to VDD and an 0.1μF capacitor to ground.

External 32.768kHz Crystal Oscillator – LXT

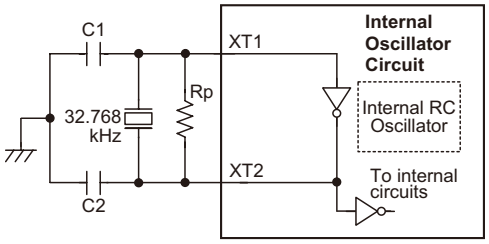
The External 32.768kHz Crystal System Oscillator is one of the low frequency oscillator choices, which is selected via configuration option. This clock source has a fixed frequency of 32.768kHz and requires a 32.768kHz crystal to be connected between pins XT1 and XT2. The external resistor and capacitor components connected to the 32.768kHz crystal are necessary to provide oscillation. For applications where precise frequencies are essential, these components may be required to provide frequency compensation due to different crystal manufacturing tolerances. During power-up there is a time delay associated with the LXT oscillator waiting for it to start-up.

When the microcontroller enters the SLEEP or IDLE Mode, the system clock is switched off to stop microcontroller activity and to conserve power. However, in many microcontroller applications it may be necessary to keep the internal timers operational even when the microcontroller is in the SLEEP or IDLE Mode. To do this, another clock, independent of the system clock, must be provided.

However, for some crystals, to ensure oscillation and accurate frequency generation, it is necessary to add two small value external capacitors, C1 and C2. The exact values of C1 and C2 should be selected in consultation with the crystal or resonator manufacturer’s specification. The external parallel feedback resistor, Rp, is required.

Some configuration options determine if the XT1/XT2 pins are used for the LXT oscillator or as I/O pins.

- If the LXT oscillator is not used for any clock source, the XT1/XT2 pins can be used as normal I/O pins.
- If the LXT oscillator is used for any clock source, the 32.768kHz crystal should be connected to the XT1/XT2 pins.



Note: 1. Rp, C1 and C2 are required.
2. Although not shown pins have a parasitic capacitance of around 7pF.

External LXT Oscillator

LXT Oscillator C1 and C2 Values		
Crystal Frequency	**C1**	**C2**
32.768kHz	10pF	10pF
Note: 1. C1 and C2 values are for guidance only. 2. R_P=5M~10M is recommended.		

32.768kHz Crystal Recommended Capacitor Values

LXT Oscillator Low Power Function

The LXT oscillator can function in one of two modes, the Quick Start Mode and the Low Power Mode. The mode selection is executed using the LXTLP bit in the TBC register.

LXTLP Bit	LXT Mode
0	Quick Start
1	Low-power

After power on the LXTLP bit will be automatically cleared to zero ensuring that the LXT oscillator is in the Quick Start operating mode. In the Quick Start Mode the LXT oscillator will power up and stabilise quickly. However, after the LXT oscillator has fully powered up it can be placed into the Low-power mode by setting the LXTLP bit high. The oscillator will continue to run but with reduced current consumption, as the higher current consumption is only required during the LXT oscillator start-up. In power sensitive applications, such as battery applications, where power consumption must be kept to a minimum, it is therefore recommended that the application program sets the LXTLP bit high about 2 seconds after power-on.

It should be noted that, no matter what condition the LXTLP bit is set to, the LXT oscillator will always function normally, the only difference is that it will take more time to start up if in the Low-power mode.

Internal 32kHz Oscillator – LIRC

The Internal 32kHz System Oscillator is one of the low frequency oscillator choices, which is selected via configuration option. It is a fully integrated RC oscillator with a typical frequency of 32kHz at 5V, requiring no external components for its implementation. Device trimming during the manufacturing process and the inclusion of internal frequency compensation circuits are used to ensure that the influence of the power supply voltage, temperature and process variations on the oscillation frequency are minimised. As a result, at a power supply of 5V and at a temperature of 25˚C degrees, the fixed oscillation frequency of 32kHz will have a tolerance within 10%.

Supplementary Internal Clocks

The low speed oscillators, in addition to providing a system clock source are also used to provide a clock source to two other devices functions. These are the Watchdog Timer and the Time Base Interrupts.

Operating Modes and System Clocks

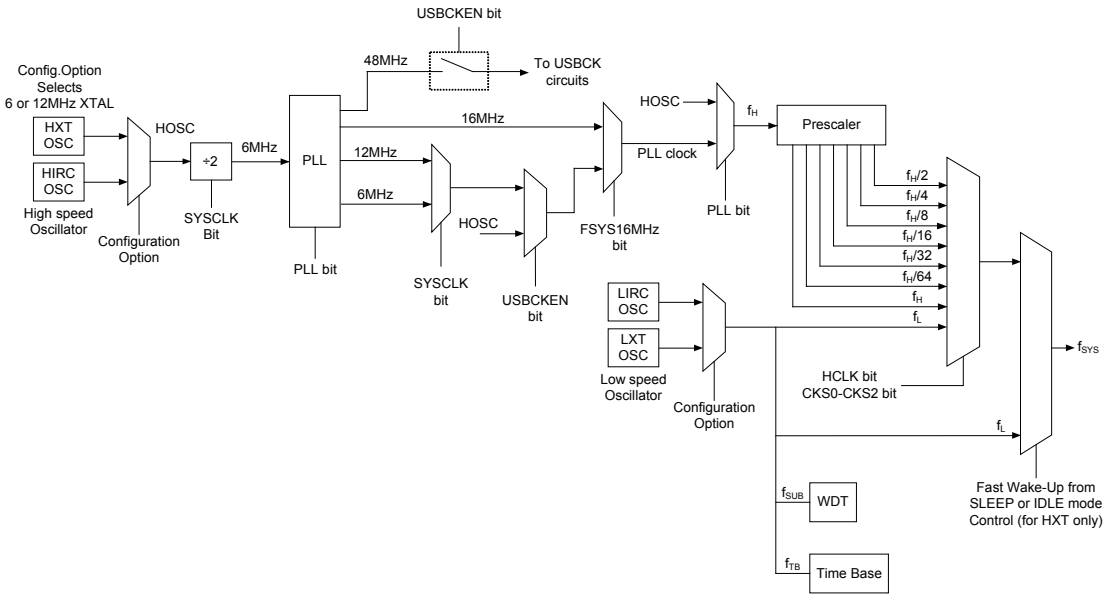
Present day applications require that their microcontrollers have high performance but often still demand that they consume as little power as possible, conflicting requirements that are especially true in battery powered portable applications. The fast clocks required for high performance will by their nature increase current consumption and of course vice versa, lower speed clocks reduce current consumption. As Holtek has provided these devices with both high and low speed clock sources and the means to switch between them dynamically, the user can optimise the operation of their microcontroller to achieve the best performance/power ratio.

System Clocks

The devices have many different clock sources for both the CPU and peripheral function operation. By providing the user with a wide range of clock options using configuration options and register programming, a clock system can be configured to obtain maximum application performance.

The main system clock, can come from either a high frequency, f_H, or low frequency, f_L, source, and is selected using the HLCLK bit and CKS2~CKS0 bits in the SMOD register. The high speed system clock can be sourced from either a HXT, PLL frequency generator or HIRC oscillator, selected via a configuration option. The low speed system clock source can be sourced from internal clock f_L. If f_L is selected then it can be sourced by either the LXT or LIRC oscillators, selected via a configuration option. The other choice, which is a divided version of the high speed system oscillator has a range of $f_H/2$~$f_H/64$.

There are two additional internal clocks for the peripheral circuits, the substitute clock, f_{SUB}, and the Time Base clock, f_{TBC}. Each of these internal clocks is sourced by either the LXT or LIRC oscillators, selected via configuration options. The f_{SUB} clock is used to provide a substitute clock for the microcontroller just after a wake-up has occurred to enable faster wake-up times.



System Clock Configurations

Note: When the system clock source f_{SYS} is switched to f_L from f_H, the high speed oscillation will stop to conserve the power. Thus there is no f_H~f_H/64 for peripheral circuit to use.

The f_{SUB} clock is used as one of the clock sources for the Watchdog timer. The f_{TBC} clock is used as a source for the Time Base interrupt functions and for the TMs.

System Operation Modes

There are six different modes of operation for the microcontroller, each one with its own special characteristics and which can be chosen according to the specific performance and power requirements of the application. There are two modes allowing normal operation of the microcontroller, the NORMAL Mode and SLOW Mode. The remaining four modes, the SLEEP0, SLEEP1, IDLE0 and IDLE1 Mode are used when the microcontroller CPU is switched off to conserve power.

Operation Mode	Description			
	CPU	f_{SYS}	f_{SUB}	f_{TBC}
NORMAL Mode	On	f_H~f_H/64	On	On
SLOW Mode	On	f_L	On	On
IDLE0 Mode	Off	Off	On	On
IDLE1 Mode	Off	On	On	On
SLEEP0 Mode	Off	Off	Off	Off
SLEEP1 Mode	Off	Off	On	Off

- NORMAL Mode
  As the name suggests this is one of the main operating modes where the microcontroller has all of its functions operational and where the system clock is provided by one of the high speed oscillators. This mode operates allowing the microcontroller to operate normally with a clock source will come from one of the high speed oscillators, either the PLL frequency generator, HXTor HIRC oscillators. The high speed oscillator will however first be divided by a ratio ranging from 1 to 64, the actual ratio being selected by the CKS2~CKS0 and HLCLK bits in the SMOD register. Although a high speed oscillator is used, running the microcontroller at a divided clock ratio reduces the operating current.
- SLOW Mode
  This is also a mode where the microcontroller operates normally although now with a slower speed clock source. The clock source used will be from one of the low speed oscillators, either the LXT or the LIRC. Running the microcontroller in this mode allows it to run with much lower operating currents. In the SLOW Mode, the f_H is off.
- SLEEP0 Mode
  The SLEEP0 Mode is entered when an HALT instruction is executed and when the IDLEN bit in the SMOD register is low. In the SLEEP0 mode the CPU will be stopped, and the f_{SUB} clock will be stopped too, and the Watchdog Timer function is disabled. In this mode, the LVDEN is must set to "0". If the LVDEN is set to "1", it won't enter the SLEEP0 Mode.
- SLEEP1 Mode
  The SLEEP1 Mode is entered when an HALT instruction is executed and when the IDLEN bit in the SMOD register is low. In the SLEEP1 mode the CPU will be stopped. However, the f_{SUB} clock will continue to operate if the LVDEN is "1" or the Watchdog Timer function is enabled.
- IDLE0 Mode
  The IDLE0 Mode is entered when a HALT instruction is executed and when the IDLEN bit in the SMOD register is high and the FSYSON bit in the CTRL register is low. In the IDLE0 Mode the system oscillator will be inhibited from driving the CPU but some peripheral functions will remain operational such as the Watchdog Timer, TMs and SIM. In the IDLE0 Mode, the system oscillator will be stopped. In the IDLE0 Mode the Watchdog Timer clock, f_{SUB}, will be on.
- IDLE1 Mode
  The IDLE1 Mode is entered when an HALT instruction is executed and when the IDLEN bit in the SMOD register is high and the FSYSON bit in the CTRL register is high. In the IDLE1 Mode the system oscillator will be inhibited from driving the CPU but may continue to provide a clock source to keep some peripheral functions operational such as the Watchdog Timer, TMs and SIM. In the IDLE1 Mode, the system oscillator will continue to run, and this system oscillator may be high speed or low speed system oscillator. In the IDLE1 Mode the Watchdog Timer clock, f_{SUB}, will be on.

Control Register

A single register, SMOD, is used for overall control of the internal clocks within these devices.

SMOD Register

Bit	7	6	5	4	3	2	1	0
Name	CKS2	CKS1	CKS0	FSTEN	LTO	HTO	IDLEN	HLCLK
R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W
POR	0	0	0	0	0	0	1	1

Bit 7~5 **CKS2~CKS0:** The system clock selection when HLCLK is "0"
000: f_L (f_{LXT} or f_{LIRC})
001: f_L (f_{LXT} or f_{LIRC})
010: $f_H/64$
011: $f_H/32$
100: $f_H/16$
101: $f_H/8$
110: $f_H/4$
111: $f_H/2$
These three bits are used to select which clock is used as the system clock source. In addition to the system clock source, which can be either the LXT or LIRC, a divided version of the high speed system oscillator can also be chosen as the system clock source.

Bit 4 **FSTEN:** Fast Wake-up Control (only for HXT)
0: Disable
1: Enable
This is the Fast Wake-up Control bit which determines if the f_{SUB} clock source is initially used after these devices wakes up. When the bit is high, the f_{SUB} clock source can be used as a temporary system clock to provide a faster wake up time as the f_{SUB} clock is available.

Bit 3 **LTO:** Low speed system oscillator ready flag
0: Not ready
1: Ready
This is the low speed system oscillator ready flag which indicates when the low speed system oscillator is stable after power on reset or a wake-up has occurred. The flag will be low when in the SLEEP0 Mode but after a wake-up has occurred, the flag will change to a high level after 1024 clock cycles if the LXT oscillator is used and 1~2 clock cycles if the LIRC oscillator is used.

Bit 2 **HTO:** High speed system oscillator ready flag
0: Not ready
1: Ready
This is the high speed system oscillator ready flag which indicates when the high speed system oscillator is stable. This flag is cleared to "0" by hardware when these devices are powered on and then changes to a high level after the high speed system oscillator is stable. Therefore this flag will always be read as "1" by the application program after devices power-on. The flag will be low when in the SLEEP or IDLE0 Mode but after a wake-up has occurred, the flag will change to a high level after 1024 clock cycles if the HXT oscillator is used and after 1024 clock cycles if the HIRC oscillator is used.

Bit 1 **IDLEN:** IDLE Mode control
0: Disable
1: Enable

This is the IDLE Mode Control bit and determines what happens when the HALT instruction is executed. If this bit is high, when a HALT instruction is executed these devices will enter the IDLE Mode. In the IDLE1 Mode the CPU will stop running but the system clock will continue to keep the peripheral functions operational, if FSYSON bit is high. If FSYSON bit is low, the CPU and the system clock will all stop in IDLE0 mode. If the bit is low these devices will enter the SLEEP Mode when a HALT instruction is executed.

Bit 0 **HLCLK:** System clock selection
0: $f_H/2$~$f_H/64$ or f_L
1: f_H

This bit is used to select if the f_H clock or the $f_H/2$~$f_H/64$ or f_L clock is used as the system clock. When the bit is high the f_H clock will be selected and if low the $f_H/2$~$f_H/64$ or f_L clock will be selected. When system clock switches from the f_H clock to the f_L clock and the f_H clock will be automatically switched off to conserve power.

Fast Wake-up

To minimise power consumption these devices can enter the SLEEP or IDLE0 Mode, where the system clock source to these devices will be stopped. However when these devices are woken up again, it can take a considerable time for the original system oscillator to restart, stabilise and allow normal operation to resume. To ensure the device is up and running as fast as possible a Fast Wake-up function is provided, which allows f_{SUB}, namely either the LXT or LIRC oscillator, to act as a temporary clock to first drive the system until the original system oscillator has stabilised. As the clock source for the Fast Wake-up function is f_{SUB}, the Fast Wake-up function is only available in the SLEEP1 and IDLE0 modes. When these devices are woken up from the SLEEP0 mode, the Fast Wake-up function has no effect because the f_{SUB} clock is stopped. The Fast Wake-up enable/disable function is controlled using the FSTEN bit in the SMOD register.

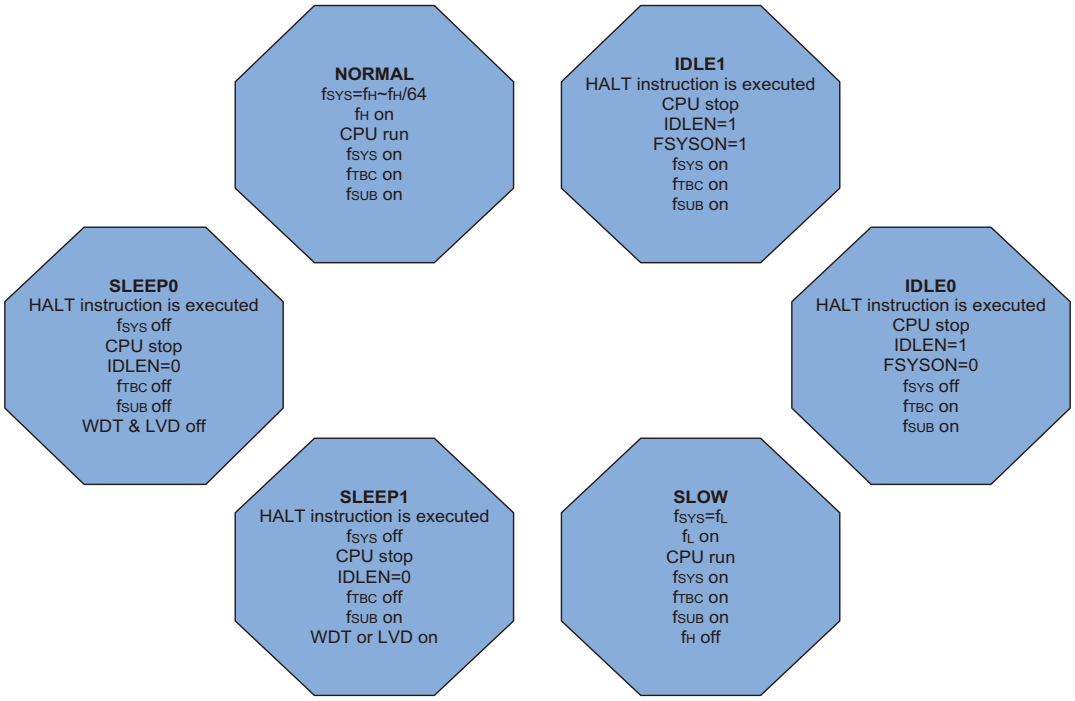
If the HXT oscillator is selected as the NORMAL Mode system clock, and if the Fast Wake-up function is enabled, then it will take one to two t_{SUB} clock cycles of the LIRC or LXT oscillator for the system to wake-up. The system will then initially run under the f_{SUB} clock source until 1024 HXT clock cycles have elapsed, at which point the HTO flag will switch high and the system will switch over to operating from the HXT oscillator.

If the HIRC oscillator or LIRC oscillator is used as the system oscillator then it will take 1024 clock cycles of the HIRC or 1~2 cycles of the LIRC to wake up the system from the SLEEP or IDLE0 Mode. The Fast Wake-up bit, FSTEN will have no effect in these cases.

System Oscillator	FSTEN Bit	Wake-up Time (SLEEP0 Mode)	Wake-up Time (SLEEP1 Mode)	Wake-up Time (IDLE0 Mode)	Wake-up Time (IDLE1 Mode)
HXT	0	1024 HXT cycles	1024 HXT cycles		1~2 HXT cycles
	1	1024 HXT cycles	1~2 f_{SUB} cycles (System runs with f_{SUB} first for 1024 HXT cycles and then switches over to run with the HXT clock)		1~2 HXT cycles
HIRC	X	1024 HIRC cycles	1024 HIRC cycles		1~2 HIRC cycles
LIRC	X	1~2 LIRC cycles	1~2 LIRC cycles		1~2 LIRC cycles
LXT	X	1024 LTX cycles	1024 LXT cycles		1~2 LXT cycles

Wake-Up Times

Note that if the Watchdog Timer is disabled, which means that the LXT and LIRC are all both off, then there will be no Fast Wake-up function available when these devices wake-up from the SLEEP0 Mode.



Operating Mode Switching and Wake-up

These devices can switch between operating modes dynamically allowing the user to select the best performance/power ratio for the present task in hand. In this way microcontroller operations that do not require high performance can be executed using slower clocks thus requiring less operating current and prolonging battery life in portable applications.

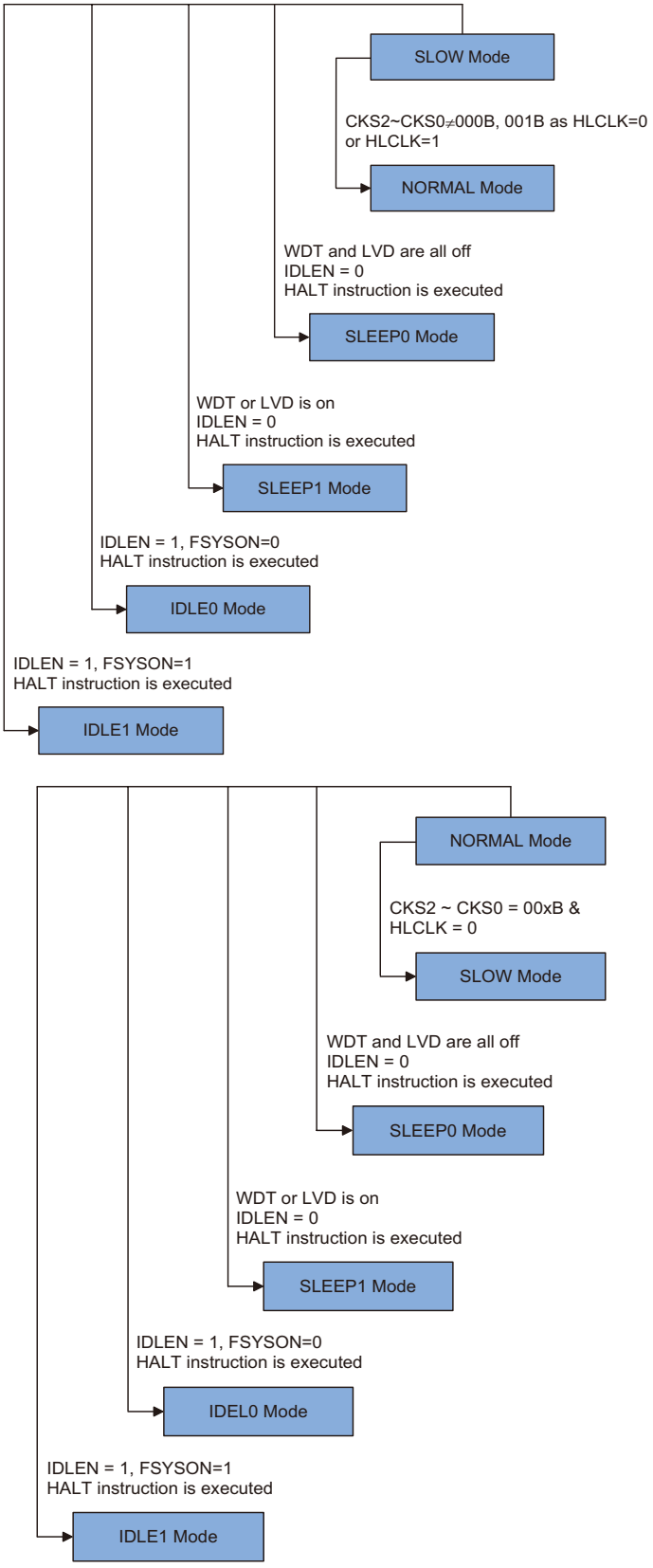
In simple terms, Mode Switching between the NORMAL Mode and SLOW Mode is executed using the HLCLK bit and CKS2~CKS0 bits in the SMOD register while Mode Switching from the NORMAL/SLOW Modes to the SLEEP/IDLE Modes is executed via the HALT instruction. When a HALT instruction is executed, whether these devices enter the IDLE Mode or the SLEEP Mode is determined by the condition of the IDLEN bit in the SMOD register and FSYSON in the CTRL register.

When the HLCLK bit switches to a low level, which implies that clock source is switched from the high speed clock source, f_H, to the clock source, $f_H/2$~$f_H/64$ or f_L. If the clock is from the f_L, the high speed clock source will stop running to conserve power. When this happens it must be noted that the $f_H/16$ and $f_H/64$ internal clock sources will also stop running, which may affect the operation of other internal functions such as the TMs and the SIM. The accompanying flowchart shows what happens when these devices move between the various operating modes.

NORMAL Mode to SLOW Mode Switching

When running in the NORMAL Mode, which uses the high speed system oscillator, and therefore consumes more power, the system clock can switch to run in the SLOW Mode by set the HLCLK bit to “0” and set the CKS2~CKS0 bits to “000” or “001” in the SMOD register. This will then use the low speed system oscillator which will consume less power. Users may decide to do this for certain operations which do not require high performance and can subsequently reduce power consumption.

The SLOW Mode is sourced from the LXT or the LIRC oscillators and therefore requires these oscillators to be stable before full mode switching occurs. This is monitored using the LTO bit in the SMOD register.


SLOW Mode
CKS2~CKS0≠000B, 001B as HLCLK=0
or HLCLK=1
NORMAL Mode
WDT and LVD are all off
IDLEN = 0
HALT instruction is executed
SLEEP0 Mode
WDT or LVD is on
IDLEN = 0
HALT instruction is executed
SLEEP1 Mode
IDLEN = 1, FSYSON=0
HALT instruction is executed
IDLE0 Mode
IDLEN = 1, FSYSON=1
HALT instruction is executed
IDLE1 Mode
NORMAL Mode
CKS2 ~ CKS0 = 00xB &
HLCLK = 0
SLOW Mode
WDT and LVD are all off
IDLEN = 0
HALT instruction is executed
SLEEP0 Mode
WDT or LVD is on
IDLEN = 0
HALT instruction is executed
SLEEP1 Mode
IDLEN = 1, FSYSON=0
HALT instruction is executed
IDEL0 Mode
IDLEN = 1, FSYSON=1
HALT instruction is executed
IDLE1 Mode

SLOW Mode to NORMAL Mode Switching

In SLOW Mode the system uses either the LXT or LIRC low speed system oscillator. To switch back to the NORMAL Mode, where the high speed system oscillator is used, the HLCLK bit should be set to "1" or HLCLK bit is "0", but CKS2~CKS0 is set to "010", "011", "100", "101", "110" or "111". As a certain amount of time will be required for the high frequency clock to stabilise, the status of the HTO bit is checked. The amount of time required for high speed system oscillator stabilization depends upon which high speed system oscillator type is used.

Entering the SLEEP0 Mode

There is only one way for these devices to enter the SLEEP0 Mode and that is to execute the "HALT" instruction in the application program with the IDLEN bit in SMOD register equal to "0" and the WDT and LVD both off. When this instruction is executed under the conditions described above, the following will occur:

- The system clock, WDT clock and Time Base clock will be stopped and the application program will stop at the "HALT" instruction.
- The Data Memory contents and registers will maintain their present condition.
- The WDT will be cleared and stopped no matter if the WDT clock source originates from the f_{SUB} clock or from the system clock.
- The I/O ports will maintain their present conditions.
- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

Entering the SLEEP1 Mode

There is only one way for these devices to enter the SLEEP1 Mode and that is to execute the "HALT" instruction in the application program with the IDLEN bit in SMOD register equal to "0" and the WDT or LVD on. When this instruction is executed under the conditions described above, the following will occur:

- The system clock and Time Base clock will be stopped and the application program will stop at the "HALT" instruction, but the WDT or LVD will remain with the clock source coming from the f_{SUB} clock.
- The Data Memory contents and registers will maintain their present condition.
- The WDT will be cleared and resume counting if the WDT clock source is selected to come from the f_{SUB} clock as the WDT is enabled.
- The I/O ports will maintain their present conditions.
- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

Entering the IDLE0 Mode

There is only one way for these devices to enter the IDLE0 Mode and that is to execute the "HALT" instruction in the application program with the IDLEN bit in SMOD register equal to "1" and the FSYSON bit in CTRL register equal to "0". When this instruction is executed under the conditions described above, the following will occur:

- The system clock will be stopped and the application program will stop at the "HALT" instruction, but the Time Base clock and f_{SUB} clock will be on.
- The Data Memory contents and registers will maintain their present condition.
- The WDT will be cleared and resume counting if the WDT clock source is selected to come from the f_{SUB} clock and the WDT is enabled. The WDT will stop if its clock source originates from the system clock.
- The I/O ports will maintain their present conditions.
- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

Entering the IDLE1 Mode

There is only one way for these devices to enter the IDLE1 Mode and that is to execute the "HALT" instruction in the application program with the IDLEN bit in SMOD register equal to "1" and the FSYSON bit in CTRL register equal to "1". When this instruction is executed under the conditions described above, the following will occur:

- The system clock and Time Base clock and f_{SUB} clock will be on and the application program will stop at the "HALT" instruction.
- The Data Memory contents and registers will maintain their present condition.
- The WDT will be cleared and resume counting if the WDT is enabled regardless of the WDT clock source which originates from the f_{SUB} clock or from the system clock.
- The I/O ports will maintain their present conditions.
- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

Standby Current Considerations

As the main reason for entering the SLEEP or IDLE Mode is to keep the current consumption of these devices to as low a value as possible, perhaps only in the order of several micro-amps except in the IDLE1 Mode, there are other considerations which must also be taken into account by the circuit designer if the power consumption is to be minimised. Special attention must be made to the I/O pins on these devices. All high-impedance input pins must be connected to either a fixed high or low level as any floating input pins could create internal oscillations and result in increased current consumption. This also applies to devices which have different package types, as there may be unbonded pins. These must either be setup as outputs or if setup as inputs must have pull-high resistors connected.

Care must also be taken with the loads, which are connected to I/O pins, which are setup as outputs. These should be placed in a condition in which minimum current is drawn or connected only to external circuits that do not draw current, such as other CMOS inputs. Also note that additional standby current will also be required if the configuration options have enabled the LXT or LIRC oscillator.

In the IDLE1 Mode the system oscillator is on, if the system oscillator is from the high speed system oscillator, the additional standby current will also be perhaps in the order of several hundred micro-amps.

Wake-up

After the system enters the SLEEP or IDLE Mode, it can be woken up from one of various sources listed as follows:

- An external or USB reset
- An external rising or falling edge on Port
- A system interrupt
- A WDT overflow

If the system is woken up by an external or USB reset, these devices will experience a full system reset, however, if these devices are woken up by a WDT overflow, a Watchdog Timer reset will be initiated. Although both of these wake-up methods will initiate a reset operation, the actual source of the wake-up can be determined by examining the TO and PDF flags. The PDF flag is cleared by a system power-up or executing the clear Watchdog Timer instructions and is set when executing the "HALT" instruction. The TO flag is set if a WDT time-out occurs, and causes a wake-up that only resets the Program Counter and Stack Pointer, the other flags remain in their original status.

Each pin on Port can be setup using the PAWU or PXWU register to permit a negative transition on the pin to wake-up the system. When a pin wake-up occurs, the program will resume execution at the instruction following the "HALT" instruction. If the system is woken up by an interrupt, then two possible situations may occur. The first is where the related interrupt is disabled or the interrupt is enabled but the stack is full, in which case the program will resume execution at the instruction following the "HALT" instruction. In this situation, the interrupt which woke-up these devices will not be immediately serviced, but will rather be serviced later when the related interrupt is finally enabled or when a stack level becomes free. The other situation is where the related interrupt is enabled and the stack is not full, in which case the regular interrupt response takes place. If an interrupt request flag is set high before entering the SLEEP or IDLE Mode, the wake-up function of the related interrupt will be disabled.

Programming Considerations

The HXT and LXT oscillators both use the same SST counter. For example, if the system is woken up from the SLEEP0 Mode and both the HXT and LXT oscillators need to start-up from an off state. The LXT oscillator uses the SST counter after HXT oscillator has finished its SST period.

- If these devices are woken up from the SLEEP0 Mode to the NORMAL Mode, the high speed system oscillator needs an SST period. These devices will execute first instruction after HTO is "1". At this time, the LXT oscillator may not be stability if f_{SUB} is from LXT oscillator. The same situation occurs in the power-on state. The LXT oscillator is not ready yet when the first instruction is executed.
- If these devices are woken up from the SLEEP1 Mode to NORMAL Mode, and the system clock source is from HXT oscillator and FSTEN is "1", the system clock can be switched to the LXT or LIRC oscillator after wake up.
- There are peripheral functions, such as WDT, TMs and SIM, for which the f_{SYS} is used. If the system clock source is switched from f_H to f_L, the clock source to the peripheral functions mentioned above will change accordingly.
- The on/off condition of f_{SUB} depends upon whether the WDT is enabled or disabled as the WDT clock source is selected from f_{SUB}.

Watchdog Timer

The Watchdog Timer is provided to prevent program malfunctions or sequences from jumping to unknown locations, due to certain uncontrollable external events such as electrical noise.

Watchdog Timer Clock Source

The Watchdog Timer clock source is provided by the internal clock, f_{SUB}, which can be sourced from either the LXT or LIRC oscillators, chosen via a configuration option. The Watchdog Timer source clock is then subdivided by a ratio of 2^8 to 2^{18} to give longer timeouts, the actual value being chosen using the WS2~WS0 bits in the WDTC register. The LIRC internal oscillator has an approximate period of 32kHz at a supply voltage of 5V.

However, it should be noted that this specified internal clock period can vary with V_{DD}, temperature and process variations. The WDT function is allowed to enable or disable by setting the WDTC register data.

Watchdog Timer Control Register

A single register, WDTC, controls the required timeout period as well as the enable/disable operation. The WRF software reset flag will be indicated in the CTRL register.

WDTC Register

Bit	7	6	5	4	3	2	1	0
Name	WE4	WE3	WE2	WE1	WE0	WS2	WS1	WS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	1	0	1	0	0	1	1

Bit 7~3 **WE4~WE0:** WDT function software control
10101: WDT Disabled
01010: WDT Enabled
Other values: Reset MCU
When these bits are changed to any other values due to environmental noise the microcontroller will be reset; this reset operation will be activated after 2~3 LIRC clock cycles and the WRF bit in the CTRL register will be set to 1 to indicate the reset source.

Bit 2~0 **WS2, WS1, WS0**: WDT time-out period selection
000: $2^8/f_{SUB}$
001: $2^{10}/f_{SUB}$
010: $2^{12}/f_{SUB}$
011: $2^{14}/f_{SUB}$
100: $2^{15}/f_{SUB}$
101: $2^{16}/f_{SUB}$
110: $2^{17}/f_{SUB}$
111: $2^{18}/f_{SUB}$
These three bits determine the division ratio of the Watchdog Timer source clock, which in turn determines the timeout period.

CTRL Register

Bit	7	6	5	4	3	2	1	0
Name	FSYSON	—	—	—	—	LVRF	LRF	WRF
R/W	R/W	—	—	—	—	R/W	R/W	R/W
POR	0	—	—	—	—	x	0	0

Bit 7 **FSYSON:** f_{SYS} Control in IDLE Mode
Described elsewhere.

Bit 6~3 Unimplemented, read as "0"

Bit 2 **LVRF:** LVR function reset flag
Described elsewhere.

Bit 1 **LRF:** LVR Control register software reset flag
Described elsewhere.

Bit 0 **WRF:** WDT Control register software reset flag
0: Not occurred
1: Occurred
This bit is set to 1 by the WDT Control register software reset and cleared by the application program. Note that this bit can only be cleared to 0 by the application program.

Watchdog Timer Operation

The Watchdog Timer operates by providing a device reset when its timer overflows. This means that in the application program and during normal operation the user has to strategically clear the Watchdog Timer before it overflows to prevent the Watchdog Timer from executing a reset. This is done using the clear watchdog instructions. If the program malfunctions for whatever reason, jumps to an unknown location, or enters an endless loop, these clear instructions will not be executed in the correct manner, in which case the Watchdog Timer will overflow and reset these devices. With regard to the Watchdog Timer enable/disable function, there are also five bits, WE4~WE0, in the WDTC register to offer additional enable/disable and reset control of the Watchdog Timer.

WDT Enable/Disabled using the WDT Control Register

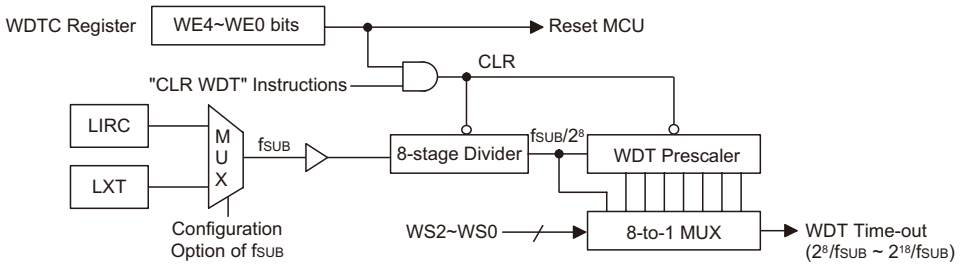
The WDT is enabled/disabled using the WDT control register, the WE4~WE0 values can determine which mode the WDT operates in. The WDT will be disabled when the WE4~WE0 bits are set to a value of 10101B. The WDT function will be enabled if the WE4~WE0 bit value is equal to 01010B. If the WE4~WE0 bits are set to any other values other than 01010B and 10101B, it will reset these devices after 2~3 LIRC clock cycles. After power on these bits will have the value of 01010B.

WDT	WE4~WE0 Bits	WDT Function
Controlled by WDT Control Register	10101B	Disable
	01010B	Enable
	Any other value	Reset MCU

Watchdog Timer Enable/Disable Control

Under normal program operation, a Watchdog Timer time-out will initialise a device reset and set the status bit TO. However, if the system is in the SLEEP or IDLE Mode, when a Watchdog Timer time-out occurs, the TO bit in the status register will be set and only the Program Counter and Stack Pointer will be reset. Three methods can be adopted to clear the Watchdog Timer contents. The first is a WDT reset, which means a value other than 01010B or 10101B is written into the WE4~WE0 bit locations, the second is to use the Watchdog Timer software clear instructions and the third is via a HALT instruction. There is only one method of using software instruction to clear the Watchdog Timer and that is to use the single "CLR WDT" instruction to clear the WDT.

The maximum time out period is when the 2^{18} division ratio is selected. As an example, with a 32kHz LIRC oscillator as its source clock, this will give a maximum watchdog period of around 8 seconds for the 2^{18} division ratio, and a minimum timeout of 7.8ms for the 2^8 division ration.



Watchdog Timer

Reset and Initialisation

A reset function is a fundamental part of any microcontroller ensuring that these devices can be set to some predetermined condition irrespective of outside parameters. A hardware reset will of course be automatically implemented after these devices are powered-on, however there are a number of other hardware and software reset sources that can be implemented dynamically when these devices are running.

Reset Overview

The most important reset condition is after power is first applied to the microcontroller. In this case, internal circuitry will ensure that the microcontroller, after a short delay, will be in a well defined state and ready to execute the first program instruction. After this power-on reset, certain important internal registers will be set to defined states before the program instructions commence execution. One of these registers is the Program Counter, which will be reset to zero forcing the microcontroller to begin program execution from the lowest Program Memory address.

These devices provide several reset sources to generate the internal reset signal, providing extended MCU protection. The different types of resets are listed in the accompanying table.

No.	Reset Name	Abbreviation	Indication Bit	Register	Notes
1	Power-On Reset	POR	—	—	Auto generated at power on
2	Reset Pin	$\overline{\text{RES}}$	—	—	Hardware Reset
3	Low-Voltage Reset	LVR	LRF	CTRL	Low V_{DD} voltage
4	Watchdog Reset	WDT	TO	STATUS	—
5	WDTC Register Setting Software Reset	—	WRF	CTRL	Write to WDTC register

Reset Source Summary

In addition to the power-on reset, situations may arise where it is necessary to forcefully apply a reset condition when the microcontroller is running. One example of this is where after power has been applied and the microcontroller is already running, the $\overline{\text{RES}}$ line is forcefully pulled low. In such a case, known as a normal operation reset, some of the registers remain unchanged allowing the microcontroller to proceed with normal operation after the reset line is allowed to return high.

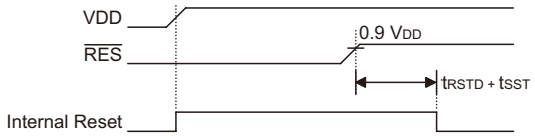
Another type of reset is when the Watchdog Timer overflows and resets the microcontroller. All types of reset operations result in different register conditions being setup. Another reset exists in the form of a Low Voltage Reset, LVR, where a full reset, similar to the $\overline{\text{RES}}$ reset is implemented in situations where the power supply voltage falls below a certain threshold.

Reset Functions

There are several ways in which a microcontroller reset can occur, through events occurring both internally and externally:

- Power-on Reset

  The most fundamental and unavoidable reset is the one that occurs after power is first applied to the microcontroller. As well as ensuring that the Program Memory begins execution from the first memory address, a power-on reset also ensures that certain other registers are preset to known conditions. All the I/O port and port control registers will power up in a high condition ensuring that all pins will be first set to inputs.



Power-on Reset Timing Chart

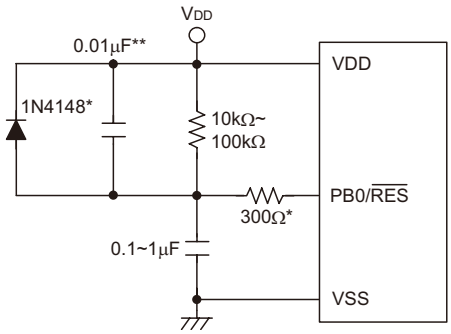
Note: t_{RSTD} is power-on delay, typical time=50ms

- $\overline{RES}$ Pin

  Although the microcontroller has an internal RC reset function, if the V_{DD} power supply rise time is not fast enough or does not stabilise quickly at power-on, the internal reset function may be incapable of providing proper reset operation. For this reason it is recommended that an external RC network is connected to the $\overline{RES}$ pin, whose additional time delay will ensure that the $\overline{RES}$ pin remains low for an extended period to allow the power supply to stabilise. During this time delay, normal operation of the microcontroller will be inhibited. After the $\overline{RES}$ line reaches a certain voltage value, the reset delay time t_{RSTD} is invoked to provide an extra delay time after which the microcontroller will begin normal operation. The abbreviation SST in the figures stands for System Start-up Timer.

  For most applications a resistor connected between VDD and the $\overline{RES}$ pin and a capacitor connected between VSS and the $\overline{RES}$ pin will provide a suitable external reset circuit. Any wiring connected to the $\overline{RES}$ pin should be kept as short as possible to minimise any stray noise interference.

  For applications that operate within an environment where more noise is present the Enhanced Reset Circuit shown is recommended.



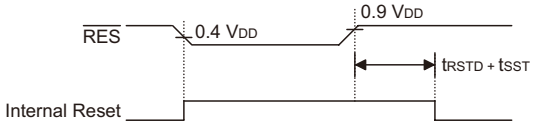
Note: * It is recommended that this component is added for added ESD protection.

** It is recommended that this component is added in environments where power line noise is significant.

Extern $\overline{RES}$ Circuit

More information regarding external reset circuits is located in Application Note HA0075E on the Holtek website.

Pulling the $\overline{RES}$ Pin low using external hardware will also execute a device reset. In this case, as in the case of other resets, the Program Counter will reset to zero and program execution initiated from this point.



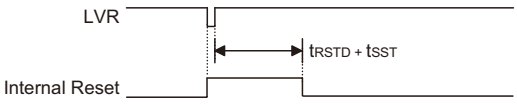
$\overline{RES}$ Reset Timing Chart

Note: t_{RSTD} is power-on delay, typical time=16.7ms

- Low Voltage Reset – LVR

  The microcontroller contains a low voltage reset circuit in order to monitor the supply voltage of the devices and provide an MCU reset should the value fall below a certain predefined level.

  The LVR function is always enabled with a specific LVR voltage V_{LVR}. If the supply voltage of the devices drops to within a range of 0.9V~V_{LVR} such as might occur when changing the battery in battery powered applications, the LVR will automatically reset the devices internally and the LVRF bit in the CTRL register will also be set to 1. For a valid LVR signal, a low supply voltage, i.e., a voltage in the range between 0.9V~V_{LVR} must exist for a time greater than that specified by t_{LVR} in the A.C. characteristics. If the low supply voltage state does not exceed this value, the LVR will ignore the low supply voltage and will not perform a reset function. The actual V_{LVR} value can be selected by the LVS bits in the LVRC register. If the LVS7~LVS0 bits are changed to some different values by environmental noise, the LVR will reset the devices after 2~3 LIRC clock cycles. When this happens, the LRF bit in the CTRL register will be set to 1. After power on the register will have the value of 01010101B. Note that the LVR function will be automatically disabled when the devices enters the power down mode.



Low Voltage Reset Timing Chart

Note: t_{RSTD} is power-on delay, typical time=16.7ms

LVRC Register

Bit	7	6	5	4	3	2	1	0
Name	LVS7	LVS6	LVS5	LVS4	LVS3	LVS2	LVS1	LVS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	1	0	1	0	1	0	1

Bit 7~0 **LVS7~LVS0:** LVR Voltage Select control
01010101: 2.1V
00110011: 2.55V
10011001: 3.15V
10101010: 3.8V
Any other value: Generates MCU reset – register is reset to POR value

When an actual low voltage condition occurs, as specified by one of the four defined LVR voltage values above, an MCU reset will be generated. The reset operation will be activated after 2~3 LIRC clock cycles. In this situation the register contents will remain the same after such a reset occurs.

Any register value, other than the four defined LVR values above, will also result in the generation of an MCU reset. The reset operation will be activated after 2~3 LIRC clock cycles. However in this situation the register contents will be reset to the POR value.

CTRL Register

Bit	7	6	5	4	3	2	1	0
Name	FSYSON	—	—	—	—	LVRF	LRF	WRF
R/W	R/W	—	—	—	—	R/W	R/W	R/W
POR	0	—	—	—	—	x	0	0

Bit 7 **FSYSON:** f_{SYS} Control in IDLE Mode
Describe elsewhere.

Bit 6~3 Unimplemented, read as 0

Bit 2 **LVRF:** LVR function reset flag
0: Not occur
1: Occurred

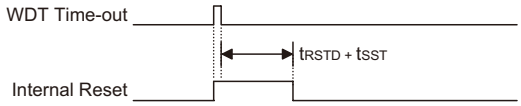
This bit is set to 1 when a specific Low Voltage Reset situation condition occurs. This bit can only be cleared to 0 by the application program.

Bit 1 **LRF:** LVR Control register software reset flag
0: Not occur
1: Occurred

This bit is set to 1 if the LVRC register contains any non defined LVR voltage register values. This in effect acts like a software reset function. This bit can only be cleared to 0 by the application program.

Bit 0 **WRF:** WDT Control register software reset flag
Describe elsewhere.

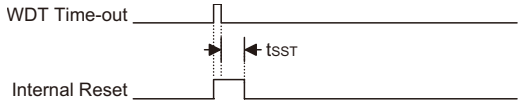
- Watchdog Time-out Reset during Normal Operation
  The Watchdog time-out Reset during normal operation is the same as a hardware $\overline{RES}$ pin reset except that the Watchdog time-out flag TO will be set to "1".



WDT Time-out Reset during Normal Operation Timing Chart

Note: t_{RSTD} is power-on delay, typical time=16.7ms

- Watchdog Time-out Reset during SLEEP or IDLE Mode
  The Watchdog time-out Reset during SLEEP or IDLE Mode is a little different from other kinds of reset. Most of the conditions remain unchanged except that the Program Counter and the Stack Pointer will be cleared to "0" and the TO flag will be set to "1". Refer to the A.C. Characteristics for t_{SST} details.



WDT Time-out Reset during SLEEP or IDLE Timing Chart

Note: The t_{SST} is 15~16 clock cycles if the system clock source is provided by HIRC.
The t_{SST} is 1024 clock for HXT or LXT. The t_{SST} is 1~2 clock for LIRC.

WDTC Register Software Reset

A WDTC software reset will be generated when a value other than "10101" or "01010", exist in the highest five bits of the WDTC register. The WRF bit in the CTRL register will be set high when this occurs, thus indicating the generation of a WDTC software reset.

WDTC Register

Bit	7	6	5	4	3	2	1	0
Name	WE4	WE3	WE2	WE1	WE0	WS2	WS1	WS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	1	0	1	0	0	1	1

Bit 7~3 **WE4, WE3, WE2, WE1, WE0:** WDT Software Control
10101: WDT Disable
01010: WDT Enable (default)
Other: MCU reset

Bit 2~0 **WS2, WS1, WS0 :** WDT time-out period selection
Described elsewhere

Reset Initial Conditions

The different types of reset described affect the reset flags in different ways. These flags, known as PDF and TO are located in the status register and are controlled by various microcontroller operations, such as the SLEEP or IDLE Mode function or Watchdog Timer. The reset flags are shown in the table:

TO	PDF	RESET Conditions
0	0	Power-on reset
u	u	$\overline{RES}$, LVR or USB reset during NORMAL or SLOW Mode operation
1	u	WDT time-out reset during NORMAL or SLOW Mode operation
1	1	WDT time-out reset during IDLE or SLEEP Mode operation

"u" stands for unchanged

The following table indicates the way in which the various components of the microcontroller are affected after a power-on reset occurs.

Item	Condition After RESET
Program Counter	Reset to zero
Interrupts	All interrupts will be disabled
WDT	Clear after reset, WDT begins counting
Timer/Event Counter	Timer Counter will be turned off
Input/Output Ports	I/O ports will be setup as inputs, and AN0~ANn is as A/D input pin.
Stack Pointer	Stack Pointer will point to the top of the stack

The different kinds of resets all affect the internal registers of the microcontroller in different ways. To ensure reliable continuation of normal program execution after a reset occurs, it is important to know what condition the microcontroller is in after a particular reset occurs. The following table describes how each type of reset affects each of the microcontroller internal registers. Note that where more than one package type exists the table will reflect the situation for the larger package type.

The HT66FB540 register states are summarized below:

Register	Reset (Power On)	WDT Time-out/ WDTC Software Reset (Normal Operation)	$\overline{RES}$ Reset/ LVRC Software Reset (Normal Operation)	$\overline{RES}$ Reset (HALT)	WDT Time-out (HALT)*	USB-reset (Normal)	USB-reset (HALT)
MP0	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
MP1	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
ACC	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PCL	0000 0000	0000 0000	0000 0000	0000 0000	0000 0000	0000 0000	0000 0000
TBLP	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBLH	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBHP	---- xxxx	---- uuuu	---- uuuu	---- uuuu	---- uuuu	---- uuuu	---- uuuu
STATUS	--00 xxxx	--1u uuuu	--uu uuuu	--01 uuuu	--11 uuuu	--uu uuuu	--uu uuuu
BP	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00
SMOD	0000 0011	0000 0011	0000 0011	0000 0011	uuuu uuuu	0000 0011	0000 0011
INTEG	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
LVDC	--00 -000	--00 -000	--00 -000	--00 -000	--uu -uuu	--00 -000	--00 -000
INTC0	-000 0000	-000 0000	-000 0000	-000 0000	-uuu uuuu	-000 0000	-000 0000
INTC1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
INTC2	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
INTC3	-000 -000	-000 -000	-000 -000	-000 -000	-uuu -uuu	-000 -000	-000 -000
MFI0	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
MFI1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
MFI2	-0-0 -0-0	-0-0 -0-0	-0-0 -0-0	-0-0 -0-0	-u-u -u-u	-0-0 -0-0	-0-0 -0-0
PA	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PAC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PB	-111 1111	-111 1111	-111 1111	-111 1111	-uuu uuuu	-111 1111	-111 1111
PBC	-111 1111	-111 1111	-111 1111	-111 1111	-uuu uuuu	-111 1111	-111 1111
PD	--11 1111	--11 1111	--11 1111	--11 1111	--uu uuuu	--11 1111	--11 1111
PDC	--11 1111	--11 1111	--11 1111	--11 1111	--uu uuuu	--11 1111	--11 1111
PE	---1 1101	---1 1101	---1 1101	---1 1101	---u uuuu	---1 1101	---1 1101
PEC	---1 1111	---1 1111	---1 1111	---1 1111	---u uuuu	---1 1111	---1 1111
ADRL (ADRFS=0)	xxxx ----	xxxx ----	xxxx ----	xxxx ----	uuuu ----	xxxx ----	xxxx ----
ADRL (ADRFS=1)	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
ADRH (ADRFS=0)	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
ADRH (ADRFS=1)	---- xxxx	---- xxxx	---- xxxx	---- xxxx	---- uuuu	---- xxxx	---- xxxx
ADCR0	0110 -000	0110 -000	0110 -000	0110 -000	uuuu -uuu	0110 -000	0110 -000
ADCR1	00-0 -000	00-0 -000	00-0 -000	00-0 -000	uu-u -uuu	00-0 -000	00-0 -000
ACER0	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
WDTC	0101 0011	0101 0011	0101 0011	0101 0011	uuuu uuuu	0101 0011	0101 0011
TBC	0011 0111	0011 0111	0011 0111	0011 0111	uuuu uuuu	0011 0111	0011 0111
FRCR	---0 ---0	---0 ---0	---0 ---0	---0 ---0	---u ---u	---0 ---0	---0 ---0
FCR	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
FARL	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FARH	---- xxxx	---- xxxx	---- xxxx	---- xxxx	---- uuuu	---- xxxx	---- xxxx
FD0L	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD0H	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx

Register	Reset (Power On)	WDT Time-out/ WDTC Software Reset (Normal Operation)	$\overline{RES}$ Reset/ LVRC Software Reset (Normal Operation)	$\overline{RES}$ Reset (HALT)	WDT Time-out (HALT)*	USB-reset (Normal)	USB-reset (HALT)
FD1L	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD1H	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD2L	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD2H	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD3L	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD3H	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
I2CTOC	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
SIMC0	1110 000-	1110 000-	1110 000-	1110 000-	uuuu uuu-	1110 000-	1110 000-
SIMC1	1000 0001	1000 0001	1000 0001	1000 0001	uuuu uuuu	1000 0001	1000 0001
SIMD	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
SIMA/SIMC2	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
SPIAC0	111- --0-	111- --0-	111- --0-	111- --0-	uuu- --u-	111- --0-	111- --0-
SPIAC1	--00 0000	--00 0000	--00 0000	--00 0000	--uu uuuu	--00 0000	--00 0000
SPIAD	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
SBSC	0-00 ---0	0-00 ---0	0-00 ---0	0-00 ---0	u-uu ---u	0-00 ---0	0-00 ---0
PAWU	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PADIR	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PAPU	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PXPU	0000 --00	0000 --00	0000 --00	0000 --00	uuuu --uu	0000 --00	0000 --00
PAOI	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PSLEW	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PXWU	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PXOI	0000 --00	0000 --00	0000 --00	0000 --00	uuuu --uu	0000 --00	0000 --00
CP0C	1000 0--1	1000 0--1	1000 0--1	1000 0--1	uuuu u--u	1000 0--1	1000 0--1
CP1C	1000 0--1	1000 0--1	1000 0--1	1000 0--1	uuuu u--u	1000 0--1	1000 0--1
TMPC0	--01 --01	--01 --01	--01 --01	--01 --01	--uu --uu	--01 --01	--01 --01
TMPC1	--0- --0-	--0- --0-	--0- --0-	--0- --0-	--u- --u-	--0- --0-	--0- --0-
TM0C0	0000 0---	0000 0---	0000 0---	0000 0---	uuuu u---	0000 0---	0000 0---
TM0C1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM0DL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM0DH	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM0AL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM0AH	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM0RP	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM1C0	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM1C1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM1DL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM1DH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00
TM1AL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM1AH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00
TM2C0	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM2C1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM2DL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM2DH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00
TM2AL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM2AH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00

Register	Reset (Power On)	WDT Time-out/ WDTC Software Reset (Normal Operation)	$\overline{RES}$ Reset/ LVRC Software Reset (Normal Operation)	$\overline{RES}$ Reset (HALT)	WDT Time-out (HALT)*	USB-reset (Normal)	USB-reset (HALT)
TM3C0	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM3C1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM3DL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM3DH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00
TM3AL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM3AH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00
USB_STAT	11xx 000-	11xx 000-	11xx 000-	11xx 000-	11xx 000-	11xx 000-	11xx 000-
UINT	---- 0000	---- uuuu	---- 0000	---- 0000	---- uuuu	---- 0000	---- 0000
USC	1000 0000	uuuu xuux	1000 0000	1000 0000	uuuu xuux	1uuu 0100	1uuu 0100
USR	---- 0000	---- uuuu	---- 0000	---- 0000	---- uuuu	---- 0000	---- 0000
UCC	0000 0-00	uuuu u-uu	0000 0-00	0000 0-00	uuuu u-uu	0uu0 u-00	0uu0 u-00
AWR	0000 0000	uuuu uuuu	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
STLI	---- 0000	---- uuuu	---- 0000	---- 0000	---- uuuu	---- 0000	---- 0000
STLO	---- 0000	---- uuuu	---- 0000	---- 0000	---- uuuu	---- 0000	---- 0000
SIES	00-0 0000	uu-x xuuu	00-0 0000	00-0 0000	uu-x xuuu	00-0 0000	00-0 0000
MISC	000- 0000	xxu- uuuu	000- 0000	000- 0000	xxu- uuuu	000- 0000	000- 0000
UFIEN	---- 0000	---- uuuu	---- 0000	---- 0000	---- uuuu	---- 0000	---- 0000
FIFO0	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
FIFO1	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
FIFO2	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
FIFO3	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
UFOEN	---- 0000	---- uuuu	---- 0000	---- 0000	---- uuuu	---- 0000	---- 0000
UFC0	0000 00--	uuuu uu--	0000 00--	0000 00--	uuuu uu--	0000 00--	0000 00--
PAPS0	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PAPS1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
SYSC	000- -0--	000- -0--	000- -0--	000- -0--	uuu- -u--	000- -0--	000- -0--
CTRL	0--- -x00	0--- -x00	0--- -x00	0--- -x00	u--- -xuu	0--- -x00	0--- -x00
LVRC	0101 0101	0101 0101	0101 0101	0101 0101	uuuu uuuu	0101 0101	0101 0101

Note: "*" stands for "warm reset"
"-" not implement
"u" stands for "unchanged"
"x" stands for "unknown"

The HT66FB550 register states are summarized below:

Register	Reset (Power On)	WDT Time-out/ WDTC Software Reset (Normal Operation)	$\overline{RES}$ Reset/ LVRC Software Reset (Normal Operation)	$\overline{RES}$ Reset (HALT)	WDT Time-out (HALT)*	USB-reset (Normal)	USB-reset (HALT)
MP0	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
MP1	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
ACC	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PCL	0000 0000	0000 0000	0000 0000	0000 0000	0000 0000	0000 0000	0000 0000
TBLP	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBLH	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBHP	---x xxxx	---u uuuu	---u uuuu	---u uuuu	---u uuuu	---u uuuu	---u uuuu
STATUS	--00 xxxx	--1u uuuu	--uu uuuu	--01 uuuu	--11 uuuu	--uu uuuu	--uu uuuu
BP	---- -000	---- --000	---- -000	---- -000	---- -uuu	---- -000	---- -000
SMOD	0000 0011	0000 0011	0000 0011	0000 0011	uuuu uuuu	0000 0011	0000 0011
INTEG	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
LVDC	--00 -000	--00 -000	--00 -000	--00 -000	--uu -uuu	--00 -000	--00 -000
INTC0	-000 0000	-000 0000	-000 0000	-000 0000	-uuu uuuu	-000 0000	-000 0000
INTC1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
INTC2	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
INTC3	-000 -000	-000 -000	-000 -000	-000 -000	-uuu -uuu	-000 -000	-000 -000
MFI0	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
MFI1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
MFI2	-0-0 -0-0	-0-0 -0-0	-0-0 -0-0	-0-0 -0-0	-u-u -u-u	-0-0 -0-0	-0-0 -0-0
PA	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PAC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PB	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PBC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PCC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PD	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PDC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PE	--11 1101	--11 1101	--11 1101	--11 1101	--uu uuuu	--11 1101	--11 1101
PEC	--11 1111	--11 1111	--11 1111	--11 1111	--uu uuuu	--11 1111	--11 1111
ADRL (ADRFS=0)	xxxx ----	xxxx ----	xxxx ----	xxxx ----	uuuu ----	xxxx ----	xxxx ----
ADRL (ADRFS=1)	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
ADRH (ADRFS=0)	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
ADRH (ADRFS=1)	---- xxxx	---- xxxx	---- xxxx	---- xxxx	---- uuuu	---- xxxx	---- xxxx
ADCR0	0110 0000	0110 0000	0110 0000	0110 0000	uuuu uuuu	0110 0000	0110 0000
ADCR1	00-0 -000	00-0 -000	00-0 -000	00-0 -000	uu-u -uuu	00-0 -000	00-0 -000
ACER0	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
ACER1	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
WDTC	0101 0011	0101 0011	0101 0011	0101 0011	uuuu uuuu	0101 0011	0101 0011
TBC	0011 0111	0011 0111	0011 0111	0011 0111	uuuu uuuu	0011 0111	0011 0111
FRCR	---0 ---0	---0 ---0	---0 ---0	---0 ---0	---u ---u	---0 ---0	---0 ---0
FCR	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
FARL	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx

Register	Reset (Power On)	WDT Time-out/ WDTC Software Reset (Normal Operation)	$\overline{RES}$ Reset/ LVRC Software Reset (Normal Operation)	$\overline{RES}$ Reset (HALT)	WDT Time-out (HALT)*	USB-reset (Normal)	USB-reset (HALT)
FARH	---x xxxx	---x xxxx	---x xxxx	---x xxxx	---u uuuu	---x xxxx	---x xxxx
FD0L	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD0H	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD1L	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD1H	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD2L	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD2H	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD3L	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD3H	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
I2CTOC	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
SIMC0	1110 000-	1110 000-	1110 000-	1110 000-	uuuu uuu-	1110 000-	1110 000-
SIMC1	1000 0001	1000 0001	1000 0001	1000 0001	uuuu uuuu	1000 0001	1000 0001
SIMD	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
SIMA/SIMC2	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
SPIAC0	111- --0-	111- --0-	111- --0-	111- --0-	uuu- --u-	111- --0-	111- --0-
SPIAC1	--00 0000	--00 0000	--00 0000	--00 0000	--uu uuuu	--00 0000	--00 0000
SPIAD	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
SBSC	0-00 ---0	0-00 ---0	0-00 ---0	0-00 ---0	u-uu ---u	0-00 ---0	0-00 ---0
PAWU	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PADIR	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PAPU	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PXPU	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PAOI	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PSLEW	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PXWU	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PXOI	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
CP0C	1000 0--1	1000 0--1	1000 0--1	1000 0--1	uuuu u--u	1000 0--1	1000 0--1
CP1C	1000 0--1	1000 0--1	1000 0--1	1000 0--1	uuuu u--u	1000 0--1	1000 0--1
TMPC0	--01 --01	--01 --01	--01 --01	--01 --01	--uu --uu	--01 --01	--01 --01
TMPC1	--01 --01	--01 --01	--01 --01	--01 --01	--uu --uu	--01 --01	--01 --01
TM0C0	0000 0---	0000 0---	0000 0---	0000 0---	uuuu u---	0000 0---	0000 0---
TM0C1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM0DL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM0DH	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM0AL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM0AH	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM0RP	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM1C0	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM1C1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM1DL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM1DH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00
TM1AL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM1AH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00
TM2C0	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM2C1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM2DL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000

Register	Reset (Power On)	WDT Time-out/ WDTC Software Reset (Normal Operation)	$\overline{RES}$ Reset/ LVRC Software Reset (Normal Operation)	$\overline{RES}$ Reset (HALT)	WDT Time-out (HALT)*	USB-reset (Normal)	USB-reset (HALT)
TM2DH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00
TM2AL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM2AH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00
TM3C0	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM3C1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM3DL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM3DH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00
TM3AL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM3AH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00
USB_STAT	11xx 000-	11xx 000-	11xx 000-	11xx 000-	11xx 000-	11xx 000-	11xx 000-
UINT	--00 0000	--uu uuuu	--00 0000	--00 0000	--uu uuuu	--00 0000	--00 0000
USC	1000 0000	uuuu xuux	1000 0000	1000 0000	uuuu xuux	1uuu 0100	1uuu 0100
USR	--00 0000	--uu uuuu	--00 0000	--00 0000	--uu uuuu	--00 0000	--00 0000
UCC	0000 0000	uuuu uuuu	0000 0000	0000 0000	uuuu uuuu	0uu0 u000	0uu0 u000
AWR	0000 0000	uuuu uuuu	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
STLI	--00 0000	--uu uuuu	--00 0000	--00 0000	--uu uuuu	--00 0000	--00 0000
STLO	--00 0000	--uu uuuu	--00 0000	--00 0000	--uu uuuu	--00 0000	--00 0000
SIES	00-0 0000	uu-x xuuu	00-0 0000	00-0 0000	uu-x xuuu	00-0 0000	00-0 0000
MISC	0000 0000	xxuu uuuu	0000 0000	0000 0000	xxuu uuuu	0000 0000	0000 0000
UFIEN	--00 0000	--uu uuuu	--00 0000	--00 0000	--uu uuuu	--00 0000	--00 0000
FIFO0	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
FIFO1	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
FIFO2	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
FIFO3	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
FIFO4	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
FIFO5	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
UFOEN	--00 0000	--uu uuuu	--00 0000	--00 0000	--uu uuuu	--00 0000	--00 0000
UFC0	0000 00--	uuuu uu--	0000 00--	0000 00--	uuuu uu--	0000 00--	0000 00--
UFC1	---- 0000	---- uuuu	---- 0000	---- 0000	---- uuuu	---- 0000	---- 0000
PAPS0	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PAPS1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
SYSC	000- -0--	000- -0--	000- -0--	000- -0--	uuu- -u--	000- -0--	000- -0--
CTRL	0--- -x00	0--- -x00	0--- -x00	0--- -x00	u--- -xuu	0--- -x00	0--- -x00
LVRC	0101 0101	0101 0101	0101 0101	0101 0101	uuuu uuuu	0101 0101	0101 0101

Note: "*" stands for "warm reset"
"-" not implement
"u" stands for "unchanged"
"x" stands for "unknown"

The HT66FB560 register states are summarized below:

Register	Reset (Power On)	WDT Time-out/ WDTC Software Reset (Normal Operation)	$\overline{RES}$ Reset/ LVRC Software Reset (Normal Operation)	$\overline{RES}$ Reset (HALT)	WDT Time-out (HALT)*	USB-reset (Normal)	USB-reset (HALT)
MP0	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
MP1	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
ACC	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PCL	0000 0000	0000 0000	0000 0000	0000 0000	0000 0000	0000 0000	0000 0000
TBLP	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBLH	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBHP	--xx xxxx	--uu uuuu	--uu uuuu	--uu uuuu	--uu uuuu	--uu uuuu	--uu uuuu
STATUS	--00 xxxx	--1u uuuu	--uu uuuu	--01 uuuu	--11 uuuu	--uu uuuu	--uu uuuu
BP	--0- -000	--0- --000	--0- -000	--0- -000	--u- -uuu	--0- -000	--0- -000
SMOD	0000 0011	0000 0011	0000 0011	0000 0011	uuuu uuuu	0000 0011	0000 0011
INTEG	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
LVDC	--00 -000	--00 -000	--00 -000	--00 -000	--uu -uuu	--00 -000	--00 -000
INTC0	-000 0000	-000 0000	-000 0000	-000 0000	-uuu uuuu	-000 0000	-000 0000
INTC1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
INTC2	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
INTC3	-000 -000	-000 -000	-000 -000	-000 -000	-uuu -uuu	-000 -000	-000 -000
MFI0	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
MFI1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
MFI2	-0-0 -0-0	-0-0 -0-0	-0-0 -0-0	-0-0 -0-0	-u-u -u-u	-0-0 -0-0	-0-0 -0-0
PA	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PAC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PB	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PBC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PCC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PD	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PDC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PE	--11 1101	--11 1101	--11 1101	--11 1101	--uu uuuu	--11 1101	--11 1101
PEC	--11 1111	--11 1111	--11 1111	--11 1111	--uu uuuu	--11 1111	--11 1111
PF	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PFC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
ADRL (ADRFS=0)	xxxx ----	xxxx ----	xxxx ----	xxxx ----	uuuu ----	xxxx ----	xxxx ----
ADRL (ADRFS=1)	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
ADRH (ADRFS=0)	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
ADRH (ADRFS=1)	---- xxxx	---- xxxx	---- xxxx	---- xxxx	---- uuuu	---- xxxx	---- xxxx
ADCR0	0110 0000	0110 0000	0110 0000	0110 0000	uuuu uuuu	0110 0000	0110 0000
ADCR1	00-0 -000	00-0 -000	00-0 -000	00-0 -000	uu-u -uuu	00-0 -000	00-0 -000
ACER0	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
ACER1	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
WDTC	0101 0011	0101 0011	0101 0011	0101 0011	uuuu uuuu	0101 0011	0101 0011
TBC	0011 0111	0011 0111	0011 0111	0011 0111	uuuu uuuu	0011 0111	0011 0111
FRCR	---0 ---0	---0 ---0	---0 ---0	---0 ---0	---u ---u	---0 ---0	---0 ---0

Register	Reset (Power On)	WDT Time-out/ WDTC Software Reset (Normal Operation)	$\overline{RES}$ Reset/ LVRC Software Reset (Normal Operation)	$\overline{RES}$ Reset (HALT)	WDT Time-out (HALT)*	USB-reset (Normal)	USB-reset (HALT)
FCR	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
FARL	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FARH	--xx xxxx	--xx xxxx	--xx xxxx	--xx xxxx	--uu uuuu	--xx xxxx	--xx xxxx
FD0L	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD0H	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD1L	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD1H	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD2L	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD2H	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD3L	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
FD3H	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
I2CTOC	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
SIMC0	1110 000-	1110 000-	1110 000-	1110 000-	uuuu uuu-	1110 000-	1110 000-
SIMC1	1000 0001	1000 0001	1000 0001	1000 0001	uuuu uuuu	1000 0001	1000 0001
SIMD	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
SIMA/SIMC2	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
SPIAC0	111- --0-	111- --0-	111- --0-	111- --0-	uuu- --u-	111- --0-	111- --0-
SPIAC1	--00 0000	--00 0000	--00 0000	--00 0000	--uu uuuu	--00 0000	--00 0000
SPIAD	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
SBSC	0-00 ---0	0-00 ---0	0-00 ---0	0-00 ---0	u-uu ---u	0-00 ---0	0-00 ---0
PAWU	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PADIR	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PAPU	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PXPU	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PAOI	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PSLEW	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PXWU	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PXOI	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PFPU	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PFWU	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
CP0C	1000 0--1	1000 0--1	1000 0--1	1000 0--1	uuuu u--u	1000 0--1	1000 0--1
CP1C	1000 0--1	1000 0--1	1000 0--1	1000 0--1	uuuu u--u	1000 0--1	1000 0--1
TMPC0	--01 --01	--01 --01	--01 --01	--01 --01	--uu --uu	--01 --01	--01 --01
TMPC1	--01 --01	--01 --01	--01 --01	--01 --01	--uu --uu	--01 --01	--01 --01
TM0C0	0000 0---	0000 0---	0000 0---	0000 0---	uuuu u---	0000 0---	0000 0---
TM0C1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM0DL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM0DH	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM0AL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM0AH	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM1C0	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM1C1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM1DL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM1DH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00
TM1AL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM1AH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00

Register	Reset (Power On)	WDT Time-out/ WDTC Software Reset (Normal Operation)	$\overline{RES}$ Reset/ LVRC Software Reset (Normal Operation)	$\overline{RES}$ Reset (HALT)	WDT Time-out (HALT)*	USB-reset (Normal)	USB-reset (HALT)
TM2C0	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM2C1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM2DL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM2DH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00
TM2AL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM2AH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00
TM3C0	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM3C1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM3DL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM3DH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00
TM3AL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TM3AH	---- --00	---- --00	---- --00	---- --00	---- --uu	---- --00	---- --00
USB_STAT	11xx 000-	11xx 000-	11xx 000-	11xx 000-	11xx 000-	11xx 000-	11xx 000-
UINT	0000 0000	uuuu uuuu	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
USC	1000 0000	uuuu xuux	1000 0000	1000 0000	uuuu xuux	1uuu 0100	1uuu 0100
USR	0000 0000	uuuu uuuu	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
UCC	0000 0000	uuuu uuuu	0000 0000	0000 0000	uuuu uuuu	0uu0 u000	0uu0 u000
AWR	0000 0000	uuuu uuuu	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
STLI	0000 0000	uuuu uuuu	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
STLO	0000 0000	uuuu uuuu	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
SIES	00-0 0000	uu-x xuuu	00-0 0000	00-0 0000	uu-x xuuu	00-0 0000	00-0 0000
MISC	0000 0000	xxuu uuuu	0000 0000	0000 0000	xxuu uuuu	0000 0000	0000 0000
UFIEN	0000 0000	00uu uuuu	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
FIFO0	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
FIFO1	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
FIFO2	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
FIFO3	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
FIFO4	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
FIFO5	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
FIFO6	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
FIFO7	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
UFOEN	0000 0000	00uu uuuu	-0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
UFC0	0000 00--	uuuu uu--	0000 00--	0000 00--	uuuu uu--	0000 00--	0000 00--
UFC1	0000 0000	uuuu uuuu	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PAPS0	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PAPS1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
SYSC	000- -0--	000- -0--	000- -0--	000- -0--	uuu- -u--	000- -0--	000- -0--
CTRL	0--- -x00	0--- -x00	0--- -x00	0--- -x00	u--- -xuu	0--- -x00	0--- -x00
LVRC	0101 0101	0101 0101	0101 0101	0101 0101	uuuu uuuu	0101 0101	0101 0101

Note: "*" stands for "warm reset"
"-" not implement
"u" stands for "unchanged"
"x" stands for "unknown"

Input/Output Ports

Holtek microcontrollers offer considerable flexibility on their I/O ports. With the input or output designation of every pin fully under user program control, pull-high selections for all ports and wake-up selections on certain pins, the user is provided with an I/O structure to meet the needs of a wide range of application possibilities.

The devices provides bidirectional input/output lines labeled with port names PA~PF These I/O ports are mapped to the RAM Data Memory with specific addresses as shown in the Special Purpose Data Memory table. All of these I/O ports can be used for input and output operations. For input operation, these ports are non-latching, which means the inputs must be ready at the T2 rising edge of instruction "MOV A, [m]", where m denotes the port address. For output operation, all the data is latched and remains unchanged until the output latch is rewritten.

I/O Register List

- **HT66FB540**

Register Name	Bit							
	7	6	5	4	3	2	1	0
PAWU	D7	D6	D5	D4	D3	D2	D1	D0
PAPU	D7	D6	D5	D4	D3	D2	D1	D0
PA	D7	D6	D5	D4	D3	D2	D1	D0
PAC	D7	D6	D5	D4	D3	D2	D1	D0
PADIR	D7	D6	D5	D4	D3	D2	D1	D0
PAOI	D7	D6	D5	D4	D3	D2	D1	D0
PSLEW	PDSLEW1	PDSLEW0	—	—	PBSLEW1	PBSLEW0	PASLEW1	PASLEW0
PXWU	PEHWU	PELWU	PDHWU	PDLWU	—	—	PBHWU	PBLWU
PXPU	PEHPU	PELPU	PDHPU	PDLPU	—	—	PBHPU	PBLPU
PXOI	PEHI	PELI	PDHI	PDLI	—	—	PBHI	PBLI
PAPS0	PA3S1	PA3S0	PA2S1	PA2S0	PA1S1	PA1S0	PA0S1	PA0S0
PAPS1	PA7S1	PA7S0	PA6S1	PA6S0	PA5S1	PA5S0	PA4S1	PA4S0
PB	—	D6	D5	D4	D3	D2	D1	D0
PBC	—	D6	D5	D4	D3	D2	D1	D0
PD	—	—	D5	D4	D3	D2	D1	D0
PDC	—	—	D5	D4	D3	D2	D1	D0
PE	—	—	—	D4	D3	D2	D1	D0
PEC	—	—	—	D4	D3	D2	D1	D0

- **HT66FB550**

Register Name	Bit							
	7	6	5	4	3	2	1	0
PAWU	D7	D6	D5	D4	D3	D2	D1	D0
PAPU	D7	D6	D5	D4	D3	D2	D1	D0
PA	D7	D6	D5	D4	D3	D2	D1	D0
PAC	D7	D6	D5	D4	D3	D2	D1	D0
PADIR	D7	D6	D5	D4	D3	D2	D1	D0
PAOI	D7	D6	D5	D4	D3	D2	D1	D0
PSLEW	PDSLEW1	PDSLEW0	PCSLEW1	PCSLEW0	PBSLEW1	PBSLEW0	PASLEW1	PASLEW0
PXWU	PEHWU	PELWU	PDHWU	PDLWU	PCHWU	PCLWU	PBHWU	PBLWU
PXPU	PEHPU	PELPU	PDHPU	PDLPU	PCHPU	PCLPU	PBHPU	PBLPU
PXOI	PEHI	PELI	PDHI	PDLI	PCHI	PCLI	PBHI	PBLI
PAPS0	PA3S1	PA3S0	PA2S1	PA2S0	PA1S1	PA1S0	PA0S1	PA0S0
PAPS1	PA7S1	PA7S0	PA6S1	PA6S0	PA5S1	PA5S0	PA4S1	PA4S0
PB	D7	D6	D5	D4	D3	D2	D1	D0
PBC	D7	D6	D5	D4	D3	D2	D1	D0
PC	D7	D6	D5	D4	D3	D2	D1	D0
PCC	D7	D6	D5	D4	D3	D2	D1	D0
PD	D7	D6	D5	D4	D3	D2	D1	D0
PDC	D7	D6	D5	D4	D3	D2	D1	D0
PE	—	—	D5	D4	D3	D2	D1	D0
PEC	—	—	D5	D4	D3	D2	D1	D0

- **HT66FB560**

Register Name	Bit							
	7	6	5	4	3	2	1	0
PAWU	D7	D6	D5	D4	D3	D2	D1	D0
PAPU	D7	D6	D5	D4	D3	D2	D1	D0
PA	D7	D6	D5	D4	D3	D2	D1	D0
PAC	D7	D6	D5	D4	D3	D2	D1	D0
PADIR	D7	D6	D5	D4	D3	D2	D1	D0
PAOI	D7	D6	D5	D4	D3	D2	D1	D0
PSLEW	PDSLEW1	PDSLEW0	PCSLEW1	PCSLEW0	PBSLEW1	PBSLEW0	PASLEW1	PASLEW0
PXWU	PEHWU	PELWU	PDHWU	PDLWU	PCHWU	PCLWU	PBHWU	PBLWU
PXPU	PEHPU	PELPU	PDHPU	PDLPU	PCHPU	PCLPU	PBHPU	PBLPU
PXOI	PEHI	PELI	PDHI	PDLI	PCHI	PCLI	PBHI	PBLI
PAPS0	PA3S1	PA3S0	PA2S1	PA2S0	PA1S1	PA1S0	PA0S1	PA0S0
PAPS1	PA7S1	PA7S0	PA6S1	PA6S0	PA5S1	PA5S0	PA4S1	PA4S0
PB	D7	D6	D5	D4	D3	D2	D1	D0
PBC	D7	D6	D5	D4	D3	D2	D1	D0
PC	D7	D6	D5	D4	D3	D2	D1	D0
PCC	D7	D6	D5	D4	D3	D2	D1	D0
PD	D7	D6	D5	D4	D3	D2	D1	D0
PDC	D7	D6	D5	D4	D3	D2	D1	D0
PE	—	—	D5	D4	D3	D2	D1	D0
PEC	—	—	D5	D4	D3	D2	D1	D0
PFWU	D7	D6	D5	D4	D3	D2	D1	D0
PFPU	D7	D6	D5	D4	D3	D2	D1	D0
PF	D7	D6	D5	D4	D3	D2	D1	D0
PFC	D7	D6	D5	D4	D3	D2	D1	D0

Pull-high Resistors

Many product applications require pull-high resistors for their switch inputs usually requiring the use of an external resistor. To eliminate the need for these external resistors, all I/O pins, when configured as an input have the capability of being connected to an internal pull-high resistor. These pull-high resistors are selected using registers, namely PAPU, PXPU and PFPU, and are implemented using weak PMOS transistors. Note that the PA and PF pull-high resistors are controlled by bits in the PAPU and PFPU registers, other than the PB, PC, PD, PE pull-high resistors are controlled by nibble in the PXPU register.

PAPU Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 I/O PA bit 7~bit 0 Pull-High Control
0: Disable
1: Enable

PXPU Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	PEHPU	PELPU	PDHPU	PDLPU	—	—	PBHPU	PBLPU
R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **PEHPU:** PE4 pins Pull-High control
0: Disable
1: Enable

Bit 6 **PELPU:** PE3, PE2 and PE0 pins Pull-High control
0: Disable
1: Enable
Note that the PE1 pin has no pull-up resistor.

Bit 5 **PDHPU:** PD7~PD4 pins Pull-High control
0: Disable
1: Enable

Bit 4 **PDLPU:** PD3~PD0 pins Pull-High control
0: Disable
1: Enable

Bit 3~2 Unimplemented

Bit 1 **PBHPU:** PB6~PB4 pins Pull-High control
0: Disable
1: Enable

Bit 0 **PBLPU:** PB3~PB0 pins Pull-High control
0: Disable
1: Enable

- **HT66FB550/HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	PEHPU	PELPU	PDHPU	PDLPU	PCHPU	PCLPU	PBHPU	PBLPU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **PEHPU:** PE5~PE4 pins Pull-High control
0: Disable
1: Enable

Bit 6 **PELPU:** PE3, PE2 and PE0 pins Pull-High control
0: Disable
1: Enable
Note that the PE1 pin has no pull-up resistor.

Bit 5 **PDHPU:** PD7~PD4 pins Pull-High control
0: Disable
1: Enable

Bit 4 **PDLPU:** PD3~PD0 pins Pull-High control
0: Disable
1: Enable

Bit 3 **PCHPU:** PC7~PC4 pins Pull-High control
0: Disable
1: Enable

Bit 2 **PCLPU:** PC3~PC0 pins Pull-High control
0: Disable
1: Enable

Bit 1 **PBHPU:** PB7~PB4 pins Pull-High control
0: Disable
1: Enable

Bit 0 **PBLPU:** PB3~PB0 pins Pull-High control
0: Disable
1: Enable

PFPU Register

- **HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 I/O Port F bit 7~bit 0 Pull-High Control
0: Disable
1: Enable

Port Wake-up

The HALT instruction forces the microcontroller into the SLEEP or IDLE Mode which preserves power, a feature that is important for battery and other low-power applications. Various methods exist to wake-up the microcontroller, one of which is to change the logic condition on one of the Port A~Port F pins from high to low. This function is especially suitable for applications that can be woken up via external switches. Each pin on Port A~PortF can be selected by bits or nibble to have this wake-up feature using the PAWU, PXWU and PFWU registers.

PAWU Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PAWU:** Port A bit 7~bit 0 Wake-up Control
0: Disable
1: Enable

PXWU Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	PEHWU	PELWU	PDHWU	PDLWU	—	—	PBHWU	PBLWU
R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **PEHWU:** PE4 pins Wake-up control
0: Disable
1: Enable

Bit 6 **PELWU:** PE3, PE2,PE0 pins Wake-up control
0: Disable
1: Enable
Note that the PE1 pin has no wake-up function.

Bit 5 **PDHWU:** PD7~PD4 pins Wake-up control
0: Disable
1: Enable

Bit 4 **PDLWU:** PD3~PD0 pins Wake-up control
0: Disable
1: Enable

Bit3~2 Unimplemented

Bit 1 **PBHWU:** PB6~PB4 pins Wake-up control
0: Disable
1: Enable

Bit 0 **PBLWU:** PB3~PB0 pins Wake-up control
0: Disable
1: Enable

- **HT66FB550/HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	PEHWU	PELWU	PDHWU	PDLWU	PCHWU	PCLWU	PBHWU	PBLWU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **PEHWU:** PE5, PE4 pins Wake-up control
0: Disable
1: Enable

Bit 6 **PELWU:** PE3~PE2, PE0 pins Wake-up control
0: Disable
1: Enable
Note that the PE1 pin has no wake-up function.

Bit 5 **PDHWU:** PD7~PD4 pins Wake-up control
0: Disable
1: Enable

Bit 4 **PDLWU:** PD3~PD0 pins Wake-up control
0: Disable
1: Enable

Bit 3 **PCHWU:** PC7~PC4 pins Wake-up control
0: Disable
1: Enable

Bit 2 **PCLWU:** PC3~PC0 pins Wake-up control
0: Disable
1: Enable

Bit 1 **PBHWU:** PB7~PB4 pins Wake-up control
0: Disable
1: Enable

Bit 0 **PBLWU:** PB3~PB0 pins Wake-up control
0: Disable
1: Enable

PFWU Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PFWU:** Port A bit 7~bit 0 Wake-up Control
0: Disable
1: Enable

Port A Wake-up Polarity Control Register

The I/O port, PA, can be setup to have a choice of wake-up polarity using specific register. Each pin on Port A can be selected individually to have this Wake-up polarity feature using the PADIR register.

PADIR Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PADIR:** PA7~PA0 pins Wake-up edge control
0: Rising edge
1: Falling edge

I/O Port Control Registers

Each I/O port has its own control register known as PAC~PFC, to control the input/output configuration. With this control register, each CMOS output or input can be reconfigured dynamically under software control. Each pin of the I/O ports is directly mapped to a bit in its associated port control register. For the I/O pin to function as an input, the corresponding bit of the control register must be written as a "1". This will then allow the logic state of the input pin to be directly read by instructions. When the corresponding bit of the control register is written as a "0", the I/O pin will be setup as a CMOS output. If the pin is currently setup as an output, instructions can still be used to read the output register. However, it should be noted that the program will in fact only read the status of the output data latch and not the actual logic status of the output pin.

PAC Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

PBC Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	—	D6	D5	D4	D3	D2	D1	D0
R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	1	1	1	1	1	1	1

- **HT66FB550/HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

PCC Register

- **HT66FB550/HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

PDC Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	—	—	D5	D4	D3	D2	D1	D0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	1	1	1	1	1	1

- **HT66FB550/HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

PEC Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	D4	D3	D2	D1	D0
R/W	—	—	—	R/W	R/W	R/W	R/W	R/W
POR	—	—	—	1	1	1	1	1

- **HT66FB550/HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	—	—	D5	D4	D3	D2	D1	D0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	1	1	1	1	1	1

PFC Register

- **HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

Bit 7~0 I/O Port bit 7~bit 0 Input/Output Control
0: Output
1: Input

I/O Output Current Control Registers

The I/O ports, PA~PE, can be setup to have a choice of high or low drive currents using specific registers. Each pin on Port A can be selected individually to have this high output current feature using the PAOI register. As for PB~PE, the output current must be selected by nibble using the PXOI register. Note that the Port F is defaulted to have a low output current, the I_{OL} is 4mA and I_{OH} is -4mA at V_{DD}=5V.

PAOI Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PAOI:** PA7~PA0 pins output current control (typical value, at V_{DD}=5V)
0: I_{OL}/I_{OH} Low Current Drive
1: I_{OL}/I_{OH} High Current Drive

PXOI Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	PEHI	PELI	PDHI	PDLI	—	—	PBHI	PBLI
R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **PEHI:** PE4 pin output current control (typical value, at V_{DD}=5V)
0: I_{OL}/I_{OH} Low Current Drive
1: I_{OL}/I_{OH} High Current Drive

Bit 6 **PELI:** PE3~PE0 pins output current control (typical value, at V_{DD}=5V)
0: I_{OL}/I_{OH} Low Current Drive
1: I_{OL}/I_{OH} High Current Drive

Bit 5 **PDHI:** PD5~PD4 pins output current control (typical value, at V_{DD}=5V)
0: I_{OL}/I_{OH} Low Current Drive
1: I_{OL}/I_{OH} High Current Drive

Bit 4 **PDLI:** PD3~PD0 pins output current control (typical value, at V_{DD}=5V)
0: I_{OL}/I_{OH} Low Current Drive
1: I_{OL}/I_{OH} High Current Drive

Bit 3, 2 Unimplemented

Bit 1 **PBHI:** PB6~PB4 pins output current control (typical value, at V_{DD}=5V)
0: I_{OL}/I_{OH} Low Current Drive
1: I_{OL}/I_{OH} High Current Drive

Bit 0 **PBLI:** PB3~PB0 pins output current control (typical value, at V_{DD}=5V)
0: I_{OL}/I_{OH} Low Current Drive
1: I_{OL}/I_{OH} High Current Drive

- **HT66FB550/HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	PEHI	PELI	PDHI	PDLI	PCHI	PCLI	PBHI	PBLI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **PEHI:** PE5~PE4 pins output current control (typical value, at V_{DD}=5V)
0: I_{OL}/I_{OH} Low Current Drive
1: I_{OL}/I_{OH} High Current Drive

Bit 6 **PELI:** PE3~PE0 pins output current control (typical value, at V_{DD}=5V)
0: I_{OL}/I_{OH} Low Current Drive
1: I_{OL}/I_{OH} High Current Drive

Bit 5 **PDHI:** PD7~PD4 pins output current control (typical value, at V_{DD}=5V)
0: I_{OL}/I_{OH} Low Current Drive
1: I_{OL}/I_{OH} High Current Drive

Bit 4 **PDLI:** PD3~PD0 pins output current control (typical value, at V_{DD}=5V)
0: I_{OL}/I_{OH} Low Current Drive
1: I_{OL}/I_{OH} High Current Drive

Bit 3 **PCHI:** PC7~PC4 pins output current control (typical value, at V_{DD}=5V)
0: I_{OL}/I_{OH} Low Current Drive
1: I_{OL}/I_{OH} High Current Drive

Bit 2 **PCLI:** PC3~PC0 pins output current control (typical value, at V_{DD}=5V)
0: I_{OL}/I_{OH} Low Current Drive
1: I_{OL}/I_{OH} High Current Drive

Bit 1 **PBHI:** PB7~PB4 pins output current control (typical value, at V_{DD}=5V)
0: I_{OL}/I_{OH} Low Current Drive
1: I_{OL}/I_{OH} High Current Drive

Bit 0 **PBLI:** PB3~PB0 pins output current control (typical value, at V_{DD}=5V)
0: I_{OL}/I_{OH} Low Current Drive
1: I_{OL}/I_{OH} High Current Drive

I/O Output Slew Rate Control Registers

The I/O ports, PA~PD, can be setup to have a choice of various slew rate using specific registers. The slew rate must be selected by nibble using the PSLEW register. Note that the Port E and the Port F are defaulted to have a fixed slew rate at 200ns.

PSLEW Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	PDSLEW1	PDSLEW0	—	—	PBSLEW1	PBSLEW0	PASLEW1	PASLEW0
R/W	R/W	R/W	0	0	R/W	R/W	R/W	R/W
POR	0	0	R	R	0	0	0	0

Bit 7, 6 **PDSLEW1, PDSLEW0:** Port D output slew rate control
00: 200ns
01: 100ns
10: 50ns
11: No slew rate

Bit 5, 4 Unimplemented

Bit 3, 2 **PBSLEW1, PBSLEW0:** Port B output slew rate control
00: 200ns
01: 100ns
10: 50ns
11: No slew rate

Bit 1, 0 **PASLEW1, PASLEW0:** Port A output slew rate control
00: 200ns
01: 100ns
10: 50ns
11: No slew rate

- **HT66FB550/HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	PDSLEW1	PDSLEW0	PCSLEW1	PCSLEW0	PBSLEW1	PBSLEW0	PASLEW1	PASLEW0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7, 6 **PDSLEW1, PDSLEW0:** Port D output slew rate control
00: 200ns
01: 100ns
10: 50ns
11: No slew rate

Bit 5, 4 **PCSLEW1, PCSLEW0:** Port C output slew rate control
00: 200ns
01: 100ns
10: 50ns
11: No slew rate

Bit 3, 2 **PBSLEW1, PBSLEW0:** Port B output slew rate control
00: 200ns
01: 100ns
10: 50ns
11: No slew rate

Bit 1, 0 **PASLEW1, PASLEW0:** Port A output slew rate control
00: 200ns
01: 100ns
10: 50ns
11: No slew rate

Port A Power Source Control Registers

Port A can be setup to have a choice of various power source using specific registers. Each pin on Port A can be selected individually to have various power sources using the PAPS0 and PAPS1 registers.

PAPS0 Register

Bit	7	6	5	4	3	2	1	0
Name	PA3S1	PA3S0	PA2S1	PA2S0	PA1S1	PA1S0	PA0S1	PA0S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7, 6 **PA3S1, PA3S0:** PA3 power supply control
00: VDD
01: VDD
10: VDDIO
11: V33O, 3.3V regulator output

Bit 5, 4 **PA2S1, PA2S0:** PA2 power supply control
00: VDD
01: VDD
10: VDDIO
11: V33O, 3.3V regulator output

Bit 3, 2 **PA1S1, PA1S0:** PA1 power supply control
00: VDD
01: VDD
10: VDDIO
11: V33O, 3.3V regulator output

Bit 1, 0 **PA0S1, PA0S0:** PA0 power supply control
00: VDD
01: VDD
10: VDDIO
11: V33O, 3.3V regulator output

PAPS1 Register

Bit	7	6	5	4	3	2	1	0
Name	PA7S1	PA7S0	PA6S1	PA6S0	PA5S1	PA5S0	PA4S1	PA4S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7, 6 **PA7S1, PA7S0:** PA7 power supply control
00: VDD
01: VDD
10: VDDIO
11: V33O, 3.3V regulator output

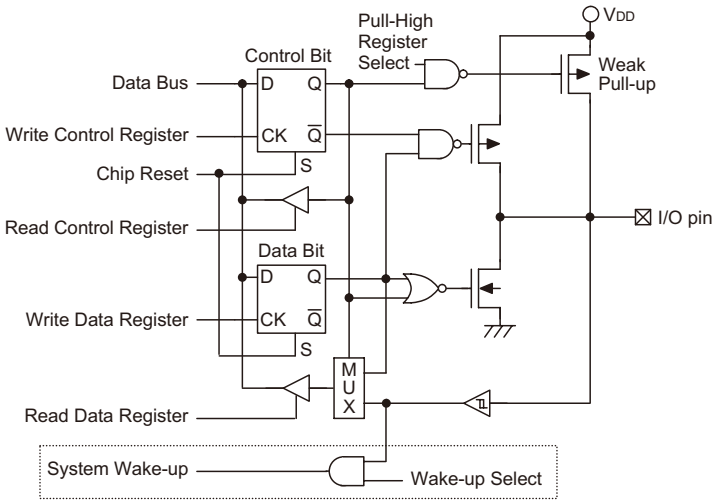
Bit 5, 4 **PA6S1, PA6S0:** PA6 power supply control
00: VDD
01: VDD
10: VDDIO
11: V33O, 3.3V regulator output

Bit 3, 2 **PA5S1, PA5S0:** PA5 power supply control
00: VDD
01: VDD
10: VDDIO
11: V33O, 3.3V regulator output

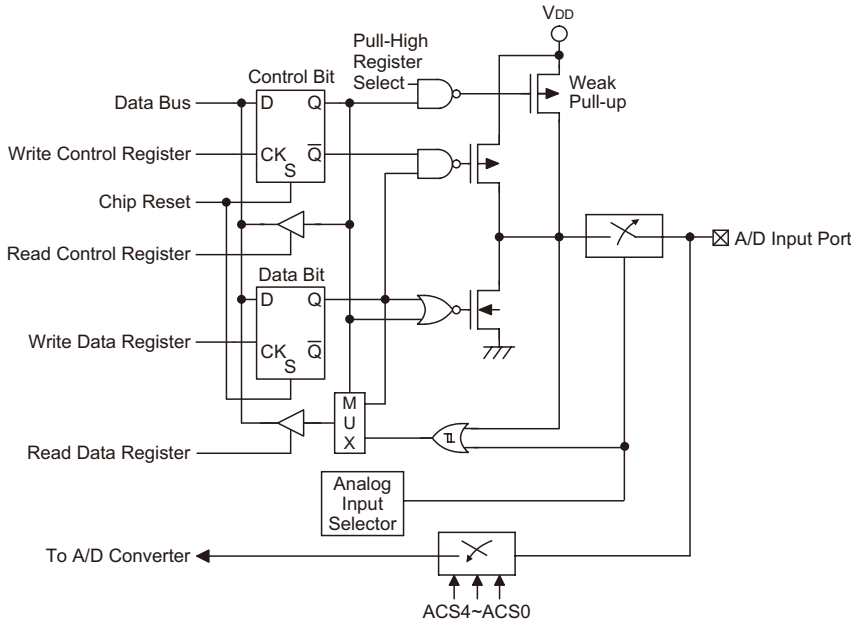
Bit 1, 0 **PA4S1, PA4S0:** PA4 power supply control
00: VDD
01: VDD
10: VDDIO
11: V33O, 3.3V regulator output

I/O Pin Structures

The accompanying diagrams illustrate the internal structures of some generic I/O pin types. As the exact logical construction of the I/O pin will differ from these drawings, they are supplied as a guide only to assist with the functional understanding of the I/O pins. The wide range of pin-shared structures does not permit all types to be shown.



Generic Input/Output Structure



A/D Input/Output Structure

Programming Considerations

Within the user program, one of the first things to consider is port initialisation. After a reset, all of the I/O data and port control registers will be set high. This means that all I/O pins will default to an input state, the level of which depends on the other connected circuitry and whether pull-high selections have been chosen. If the port control registers, PAC~PFC, are then programmed to setup some pins as outputs, these output pins will have an initial high output value unless the associated port data registers, PA~PF, are first programmed. Selecting which pins are inputs and which are outputs can be achieved byte-wide by loading the correct values into the appropriate port control register or by programming individual bits in the port control register using the "SET [m].i" and "CLR [m].i" instructions. Note that when using these bit control instructions, a read-modify-write operation takes place. The microcontroller must first read in the data on the entire port, modify it to the required new bit values and then rewrite this data back to the output ports.

All Ports provide the wake-up function which can be set by individual pin in the Port A and Port F while it has to be set by nibble pins in the Port B, Port C, Port D and Port E. When the devices are in the SLEEP or IDLE Mode, various methods are available to wake the devices up. One of these is a high to low transition of any of the Port pins. Single or multiple pins on Ports can be setup to have this function.

Timer Modules – TM

One of the most fundamental functions in any microcontroller devices are the ability to control and measure time. To implement time related functions each device includes several Timer Modules, abbreviated to the name TM. The TMs are multi-purpose timing units and serve to provide operations such as Timer/Counter, Input Capture, Compare Match Output and Single Pulse Output as well as being the functional unit for the generation of PWM signals. Each of the TMs has either two or three individual interrupts. The addition of input and output pins for each TM ensures that users are provided with timing units with a wide and flexible range of features.

The common features of the different TM types are described here with more detailed information provided in the individual Compact and Standard TM sections.

Introduction

The devices contain four TMs having a reference name of TM0, TM1, TM2 and TM3. Each individual TM can be categorised as a certain type, namely Compact Type TM or Standard Type TM. Although similar in nature, the different TM types vary in their feature complexity. The common features to all of the Compact and Standard TMs will be described in this section. The detailed operation regarding each of the TM types will be described in separate sections. The main features and differences between the two types of TMs are summarised in the accompanying table.

Function	CTM	STM
Timer/Counter	√	√
I/P Capture	—	√
Compare Match Output	√	√
PWM Channels	1	1
Single Pulse Output	—	1
PWM Alignment	Edge	Edge
PWM Adjustment Period & Duty	Duty or Period	Duty or Period

TM Function Summary

Each device in the series contains a specific number of either Compact Type and Standard Type TM units which are shown in the table together with their individual reference name, TM0~TM3.

Device	TM0	TM1	TM2	TM3
HT66FB540/HT66FB550/ HT66FB560	16-bit STM	10-bit STM	10-bit CTM	10-bit CTM

TM Name/Type Reference

TM Operation

The different types of TM offer a diverse range of functions, from simple timing operations to PWM signal generation. The key to understanding how the TM operates is to see it in terms of a free running counter whose value is then compared with the value of pre-programmed internal comparators. When the free running counter has the same value as the pre-programmed comparator, known as a compare match situation, a TM interrupt signal will be generated which can clear the counter and perhaps also change the condition of the TM output pin. The internal TM counter is driven by a user selectable clock source, which can be an internal clock or an external pin.

TM Clock Source

The clock source which drives the main counter in each TM can originate from various sources. The selection of the required clock source is implemented using the TnCK2~TnCK0 bits in the TM control registers. The clock source can be a ratio of either the system clock f_{SYS} or the internal high clock f_H, the f_{TBC} clock source or the external TCKn pin. Note that setting these bits to the value 101 will select an undefined clock input, in effect disconnecting the TM clock source. The TCKn pin clock source is used to allow an external signal to drive the TM as an external clock source or for event counting.

TM Interrupts

The Compact and Standard type TMs each have two internal interrupts, one for each of the internal comparator A or comparator P, which generate a TM interrupt when a compare match condition occurs. When a TM interrupt is generated it can be used to clear the counter and also to change the state of the TM output pin.

TM External Pins

Each of the TMs, irrespective of what type, has one TM input pin, with the label TCKn. The TM input pin, is essentially a clock source for the TM and is selected using the TnCK2~TnCK0 bits in the TMnC0 register. This external TM input pin allows an external clock source to drive the internal TM. This external TM input pin is shared with other functions but will be connected to the internal TM if selected using the TnCK2~TnCK0 bits. The TM input pin can be chosen to have either a rising or falling active edge.

The TMs each have one or more output pins with the label TPn. When the TM is in the Compare Match Output Mode, these pins can be controlled by the TM to switch to a high or low level or to toggle when a compare match situation occurs. The external TPn output pin is also the pin where the TM generates the PWM output waveform. As the TM output pins are pin-shared with other function, the TM output function must first be setup using registers. A single bit in one of the registers determines if its associated pin is to be used as an external TM output pin or if it is to have another function. The number of output pins for each TM type and devices are different, the details are provided in the accompanying table.

All TM output pin names have a "_n" suffix. Pin names that include a "_0" or "_1" suffix indicate that they are from a TM with multiple output pins. This allows the TM to generate a complimentary output pair, selected using the I/O register data bits.

Device	CTM	STM	Registers
HT66FB540	TP2_1, TP3_1	TP0_0, TP0_1 TP1_0, TP1_1	TMPC0, TMPC1
HT66FB550, HT66FB560	TP2_0, TP3_0 TP2_1, TP3_1		

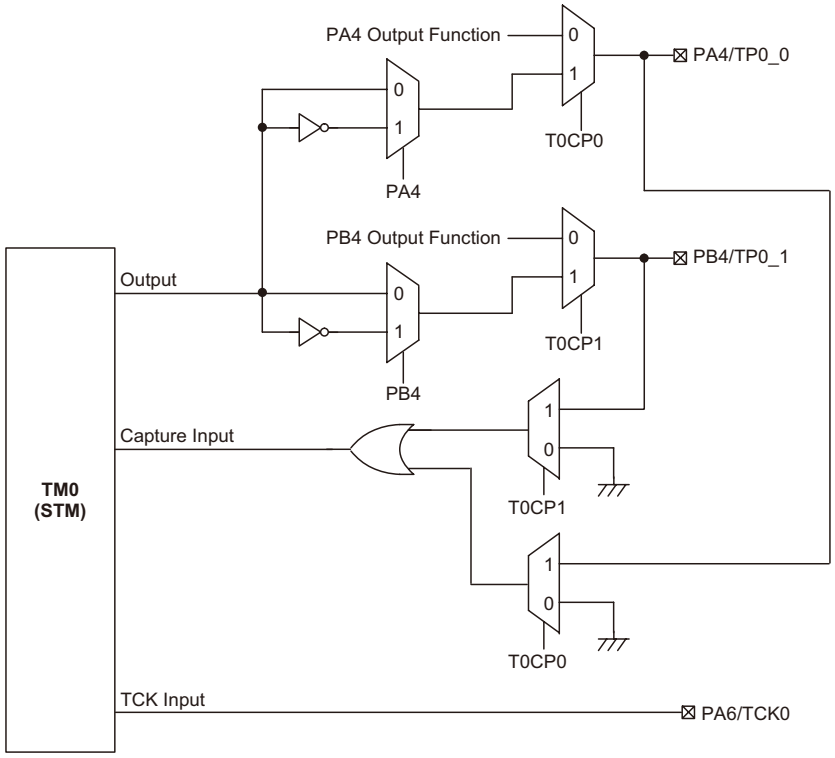
TM Output Pins

TM Input/Output Pin Control Registers

Selecting to have a TM input/output or whether to retain its other shared function, is implemented using one or two registers, with a single bit in each register corresponding to a TM input/output pin. Setting the bit high will setup the corresponding pin as a TM input/output, if reset to zero the pin will retain its original other function.

Registers	Device	Bit							
		7	6	5	4	3	2	1	0
TMPC0	HT66FB540 HT66FB550 HT66FB560	—	—	T1CP1	T1CP0	—	—	T0CP1	T0CP0
TMPC1	HT66FB540	—	—	T3CP1	—	—	—	T2CP1	—
TMPC1	HT66FB550 HT66FB560	—	—	T3CP1	T3CP0	—	—	T2CP1	T2CP0

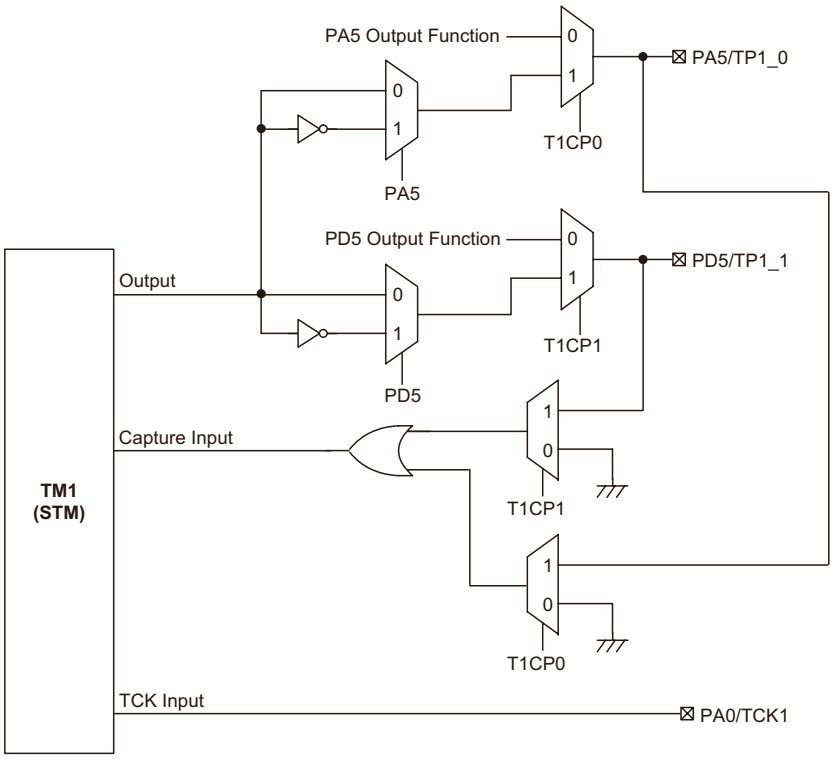
TM Input/Output Pin Control Registers List



HT66FB540/HT66FB550/HT66FB560 TM0 Function Pin Control Block Diagram

Note: (1) The I/O register data bits shown are used for TM output inversion control.

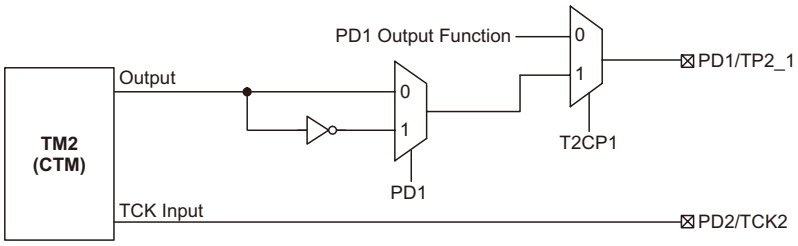
(2) In the Capture Input Mode, the TM pin control register must never enable more than one TM input.



HT66FB540/HT66FB550/HT66FB560 TM1 Function Pin Control Block Diagram

Note: (1) The I/O register data bits shown are used for TM output inversion control.

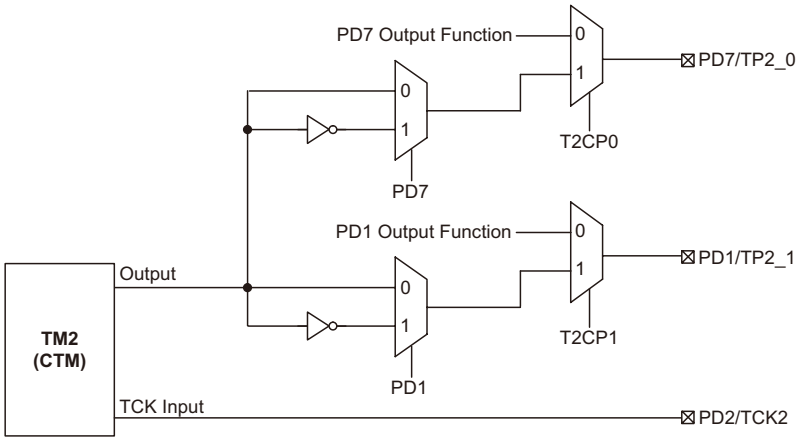
(2) In the Capture Input Mode, the TM pin control register must never enable more than one TM input.



HT66FB540 TM2 Function Pin Control Block Diagram

Note: (1) The I/O register data bits shown are used for TM output inversion control.

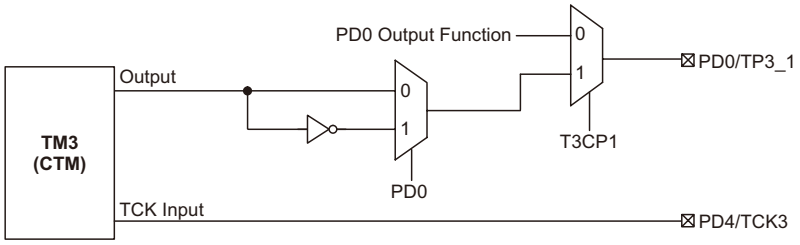
(2) In the Capture Input Mode, the TM pin control register must never enable more than one TM input.



HT66FB550/HT66FB560 TM2 Function Pin Control Block Diagram

Note: (1) The I/O register data bits shown are used for TM output inversion control.

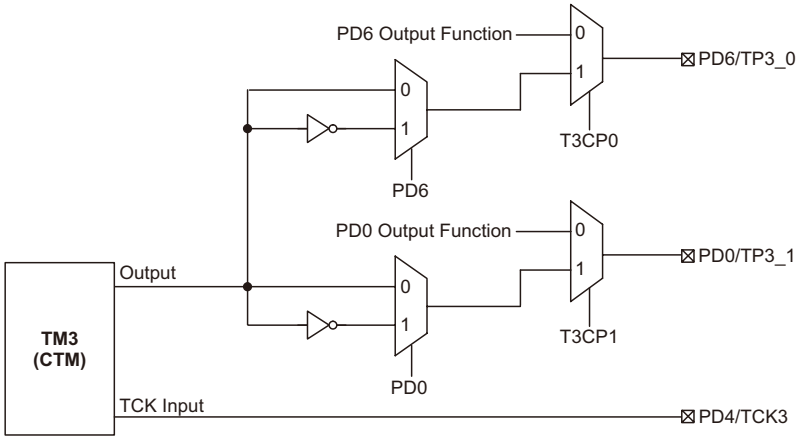
(2) In the Capture Input Mode, the TM pin control register must never enable more than one TM input.



HT66FB540 TM3 Function Pin Control Block Diagram

Note: (1) The I/O register data bits shown are used for TM output inversion control.

(2) In the Capture Input Mode, the TM pin control register must never enable more than one TM input.



HT66FB550/HT66FB560 TM3 Function Pin Control Block Diagram

Note: (1) The I/O register data bits shown are used for TM output inversion control.

(2) In the Capture Input Mode, the TM pin control register must never enable more than one TM input.

TMPC0 Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	T1CP1	T1CP0	—	—	T0CP1	T0CP0
R/W	R	R	R/W	R/W	R	R	R/W	R/W
POR	0	0	0	1	0	0	0	1

Bit 7~6 Unimplemented

Bit 5 **T1CP1:** TP1_1 pin Control
0: Disable
1: Enable

Bit 4 **T1CP0:** TP1_0 pin Control
0: Disable
1: Enable

Bit 3~2 Unimplemented

Bit 1 **T0CP1:** TP0_1 pin Control
0: Disable
1: Enable

Bit 0 **T0CP0:** TP0_0 pin Control
0: Disable
1: Enable

TMPC1 Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	—	—	T3CP1	—	—	—	T2CP1	—
R/W	R	R	R/W	R	R	R	R/W	R
POR	0	0	0	0	0	0	0	0

Bit 7~6 Unimplemented

Bit 5 **T3CP1:** TP3_1 pin Control
0: Disable
1: Enable

Bit 4~2 Unimplemented

Bit 1 **T2CP1:** TP2_1 pin Control
0: Disable
1: Enable

Bit 0 Unimplemented

- **HT66FB550/HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	—	—	T3CP1	T3CP0	—	—	T2CP1	T2CP0
R/W	R	R	R/W	R/W	R	R	R/W	R/W
POR	0	0	0	1	0	0	0	1

Bit 7~6 Unimplemented

Bit 5 **T3CP1:** TP3_1 pin Control
0: Disable
1: Enable

Bit 4 **T3CP0:** TP3_0 pin Control
0: Disable
1: Enable

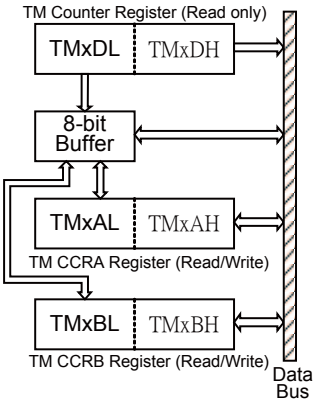
Bit 3~2 Unimplemented

Bit 1 **T2CP1:** TP2_1 pin Control
0: Disable
1: Enable

Bit 0 **T2CP0:** TP2_0 pin Control
0: Disable
1: Enable

Programming Considerations

The TM Counter Registers and the Capture/Compare CCRA register, being either 10-bit or 16-bit, all have a low and high byte structure. The high bytes can be directly accessed, but as the low bytes can only be accessed via an internal 8-bit buffer, reading or writing to these register pairs must be carried out in a specific way. The important point to note is that data transfer to and from the 8-bit buffer and its related low byte only takes place when a write or read operation to its corresponding high byte is executed.



The following steps show the read and write procedures:

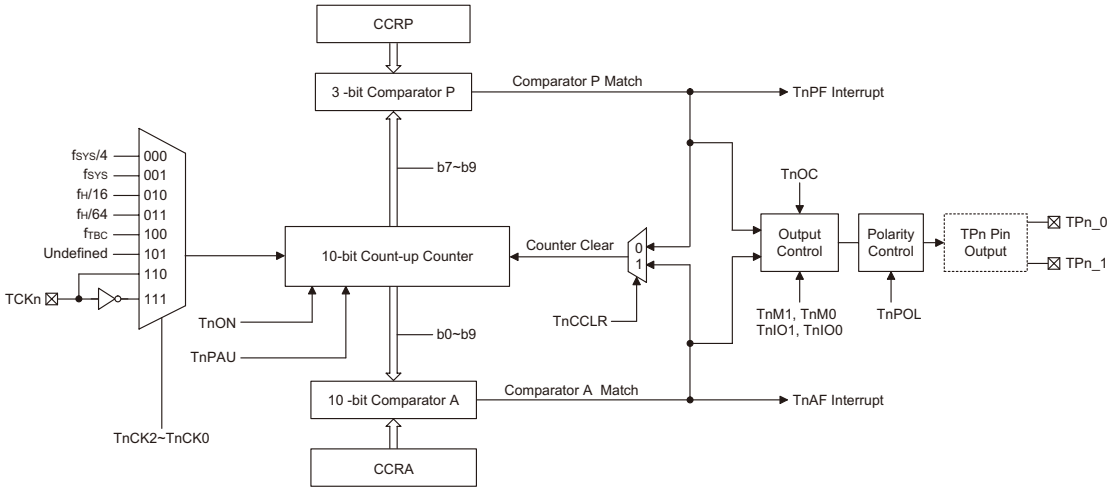
- Writing Data to CCRA
  - Step 1. Write data to Low Byte TMxAL
    – note that here data is only written to the 8-bit buffer.
  - Step 2. Write data to High Byte TMxAH
    – here data is written directly to the high byte registers and simultaneously data is latched from the 8-bit buffer to the Low Byte registers.
- Reading Data from the Counter Registers and or CCRA
  - Step 1. Read data from the High Byte TMxDH, TMxAH
    – here data is read directly from the High Byte registers and simultaneously data is latched from the Low Byte register into the 8-bit buffer.
  - Step 2. Read data from the Low Byte TMxDL, TMxAL
    – this step reads data from the 8-bit buffer.

As the CCRA register is implemented in the way shown in the following diagram and accessing the register pair is carried out in a specific way described above, it is recommended to use the "MOV" instruction to access the CCRA low byte register, named TMxAL, using the following access procedures. Accessing the CCRA low byte register without following these access procedures will result in unpredictable values.

Compact Type TM – CTM

Although the simplest form of the two TM types, the Compact TM type still contains three operating modes, which are Compare Match Output, Timer/Event Counter and PWM Output modes. The Compact TM can also be controlled with an external input pin and can drive two external output pins. These two external output pins can be the same signal or the inverse signal.

CTM	Name	TM No.	TM Input Pin	TM Output Pin
HT66FB540	10-bit CTM	2, 3	TCK2, TCK3	TP2_1, TP3_1,
HT66FB550/ HT66FB560	10-bit CTM	2, 3	TCK2, TCK3	TP2_0, TP2_1, TP3_0, TP3_1,



Compact Type TM Block Diagram

Compact TM Operation

At its core is a 10-bit count-up counter which is driven by a user selectable internal or external clock source. There are also two internal comparators with the names, Comparator A and Comparator P. These comparators will compare the value in the counter with CCRP and CCRA registers. The CCRP is three bits wide whose value is compared with the highest three bits in the counter while the CCRA is the ten bits and therefore compares with all counter bits.

The only way of changing the value of the 10-bit counter using the application program, is to clear the counter by changing the TnON bit from low to high. The counter will also be cleared automatically by a counter overflow or a compare match with one of its associated comparators. When these conditions occur, a TM interrupt signal will also usually be generated. The Compact Type TM can operate in a number of different operational modes, can be driven by different clock sources including an input pin and can also control an output pin. All operating setup conditions are selected using relevant internal registers.

Compact Type TM Register Description

Overall operation of the Compact TM is controlled using six registers. A read only register pair exists to store the internal counter 10-bit value, while a read/write register pair exists to store the internal 10-bit CCRA value. The remaining two registers are control registers which setup the different operating and control modes as well as the three CCRP bits.

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TMnC0	TnPAU	TnCK2	TnCK1	TnCK0	TnON	TnRP2	TnRP1	TnRP0
TMnC1	TnM1	TnM0	TnIO1	TnIO0	TnOC	TnPOL	TnDPX	TnCCLR
TMnDL	D7	D6	D5	D4	D3	D2	D1	D0
TMnDH	—	—	—	—	—	—	D9	D8
TMnAL	D7	D6	D5	D4	D3	D2	D1	D0
TMnAH	—	—	—	—	—	—	D9	D8

Compact TM Register List (n=2, 3)

TMnDL Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	0	0	0	0

Bit 7~0 **TMnDL:** TMn Counter Low Byte Register bit 7~bit 0
TMn 10-bit Counter bit 7~bit 0

TMnDH Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R	R
POR	—	—	—	—	—	—	0	0

Bit 7~2 Unimplemented

Bit 1~0 **TMnDH:** TMn Counter High Byte Register bit 1~bit 0
TMn 10-bit Counter bit 9~bit 8

TMnAL Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **TMnAL:** TMn CCRA Low Byte Register bit 7~bit 0
TMn 10-bit CCRA bit 7~bit 0

TMnAH Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	0

Bit 7~2 Unimplemented

Bit 1~0 **TMnAH:** TMn CCRA High Byte Register bit 1~bit 0
TMn 10-bit CCRA bit 9~bit 8

TMnC0 Register

Bit	7	6	5	4	3	2	1	0
Name	TnPAU	TnCK2	TnCK1	TnCK0	TnON	TnRP2	TnRP1	TnRP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **TnPAU:** TMn Counter Pause Control
0: Run
1: Pause

The counter can be paused by setting this bit high. Clearing the bit to zero restores normal counter operation. When in a Pause condition the TM will remain powered up and continue to consume power. The counter will retain its residual value when this bit changes from low to high and resume counting from this value when the bit changes to a low value again.

Bit 6~4 **TnCK2~TnCK0:** Select TMn Counter clock
000: $f_{SYS}/4$
001: f_{SYS}
010: $f_H/16$
011: $f_H/64$
100: f_{TBC}
101: Undefined
110: TCKn rising edge clock
111: TCKn falling edge clock

These three bits are used to select the clock source for the TMn. Selecting the Reserved clock input will effectively disable the internal counter. The external pin clock source can be chosen to be active on the rising or falling edge. The clock source f_{SYS} is the system clock, while f_H and f_{TBC} are other internal clocks, the details of which can be found in the oscillator section.

Bit 3 **TnON:** TMn Counter On/Off Control
0: Off
1: On
This bit controls the overall on/off function of the TMn. Setting the bit high enables the counter to run, clearing the bit disables the TMn. Clearing this bit to zero will stop the counter from counting and turn off the TMn which will reduce its power consumption. When the bit changes state from low to high the internal counter value will be reset to zero, however when the bit changes from high to low, the internal counter will retain its residual value. If the TMn is in the Compare Match Output Mode then the TMn output pin will be reset to its initial condition, as specified by the TnOC bit, when the TnON bit changes from low to high.

Bit 2~0 **TnRP2~TnRP0:** TMn CCRP 3-bit register, compared with the TMn Counter bit 9~bit 7 Comparator P Match Period
000: 1024 TMn clocks
001: 128 TMn clocks
010: 256 TMn clocks
011: 384 TMn clocks
100: 512 TMn clocks
101: 640 TMn clocks
110: 768 TMn clocks
111: 896 TMn clocks
These three bits are used to setup the value on the internal CCRP 3-bit register, which are then compared with the internal counter's highest three bits. The result of this comparison can be selected to clear the internal counter if the TnCCLR bit is set to zero. Setting the TnCCLR bit to zero ensures that a compare match with the CCRP values will reset the internal counter. As the CCRP bits are only compared with the highest three counter bits, the compare values exist in 128 clock cycle multiples. Clearing all three bits to zero is in effect allowing the counter to overflow at its maximum value.

TMnC1 Register

Bit	7	6	5	4	3	2	1	0
Name	TnM1	TnM0	TnIO1	TnIO0	TnOC	TnPOL	TnDPX	TnCCLR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 **TnM1~TnM0:** Select TMn Operating Mode
00: Compare Match Output Mode
01: Undefined
10: PWM Mode
11: Timer/Counter Mode

These bits setup the required operating mode for the TM. To ensure reliable operation the TM should be switched off before any changes are made to the TnM1 and TnM0 bits. In the Timer/Counter Mode, the TM output pin control must be disabled.

Bit 5~4 **TnIO1~TnIO0:** Select TPn_0, TPn_1 output function
Compare Match Output Mode
00: No change
01: Output low
10: Output high
11: Toggle output
PWM Mode
00: PWM Output inactive state
01: PWM Output active state
10: PWM output
11: Undefined
Timer/counter Mode
unused

These two bits are used to determine how the TMn output pin changes state when a certain condition is reached. The function that these bits select depends upon in which mode the TMn is running. In the Compare Match Output Mode, the TnIO1 and TnIO0 bits determine how the TMn output pin changes state when a compare match occurs from the Comparator A. The TMn output pin can be setup to switch high, switch low or to toggle its present state when a compare match occurs from the Comparator A. When the bits are both zero, then no change will take place on the output. The initial value of the TMn output pin should be setup using the TnOC bit in the TMnC1 register. Note that the output level requested by the TnIO1 and TnIO0 bits must be different from the initial value setup using the TnOC bit otherwise no change will occur on the TMn output pin when a compare match occurs. After the TMn output pin changes state it can be reset to its initial level by changing the level of the TnON bit from low to high.

In the PWM Mode, the TnIO1 and TnIO0 bits determine how the TM output pin changes state when a certain compare match condition occurs. The PWM output function is modified by changing these two bits. It is necessary to only change the values of the TnIO1 and TnIO0 bits only after the TMn has been switched off. Unpredictable PWM outputs will occur if the TnIO1 and TnIO0 bits are changed when the TM is running.

Bit 3 **TnOC:** TPn_0, TPn_1 Output control bit
Compare Match Output Mode
0: Initial low
1: Initial high
PWM Mode
0: Active low
1: Active high
This is the output control bit for the TMn output pin. Its operation depends upon whether TMn is being used in the Compare Match Output Mode or in the PWM Mode. It has no effect if the TMn is in the Timer/Counter Mode. In the Compare Match Output Mode it determines the logic level of he TMn output pin before a compare match occurs. In the PWM Mode it determines if the PWM signal is active high or active low.

Bit 2 **TnPOL:** TPn_0, TPn_1 Output polarity Control
0: Non-invert
1: Invert
This bit controls the polarity of the TPn_0 or TPn_1 output pin. When the bit is set high the TMn output pin will be inverted and not inverted when the bit is zero. It has no effect if the TMn is in the Timer/Counter Mode.

Bit 1 **TnDPX:** TMn PWM period/duty Control
0: CCRP - period; CCRA - duty
1: CCRP - duty; CCRA - period
This bit, determines which of the CCRA and CCRP registers are used for period and duty control of the PWM waveform.

Bit 0 **TnCCLR:** Select TMn Counter clear condition
0: TMn Comparator P match
1: TMn Comparator A match
This bit is used to select the method which clears the counter. Remember that the Compact TMn contains two comparators, Comparator A and Comparator P, either of which can be selected to clear the internal counter. With the TnCCLR bit set high, the counter will be cleared when a compare match occurs from the Comparator A. When the bit is low, the counter will be cleared when a compare match occurs from the Comparator P or with a counter overflow. A counter overflow clearing method can only be implemented if the CCRP bits are all cleared to zero. The TnCCLR bit is not used in the PWM Mode.

Compact Type TM Operating Modes

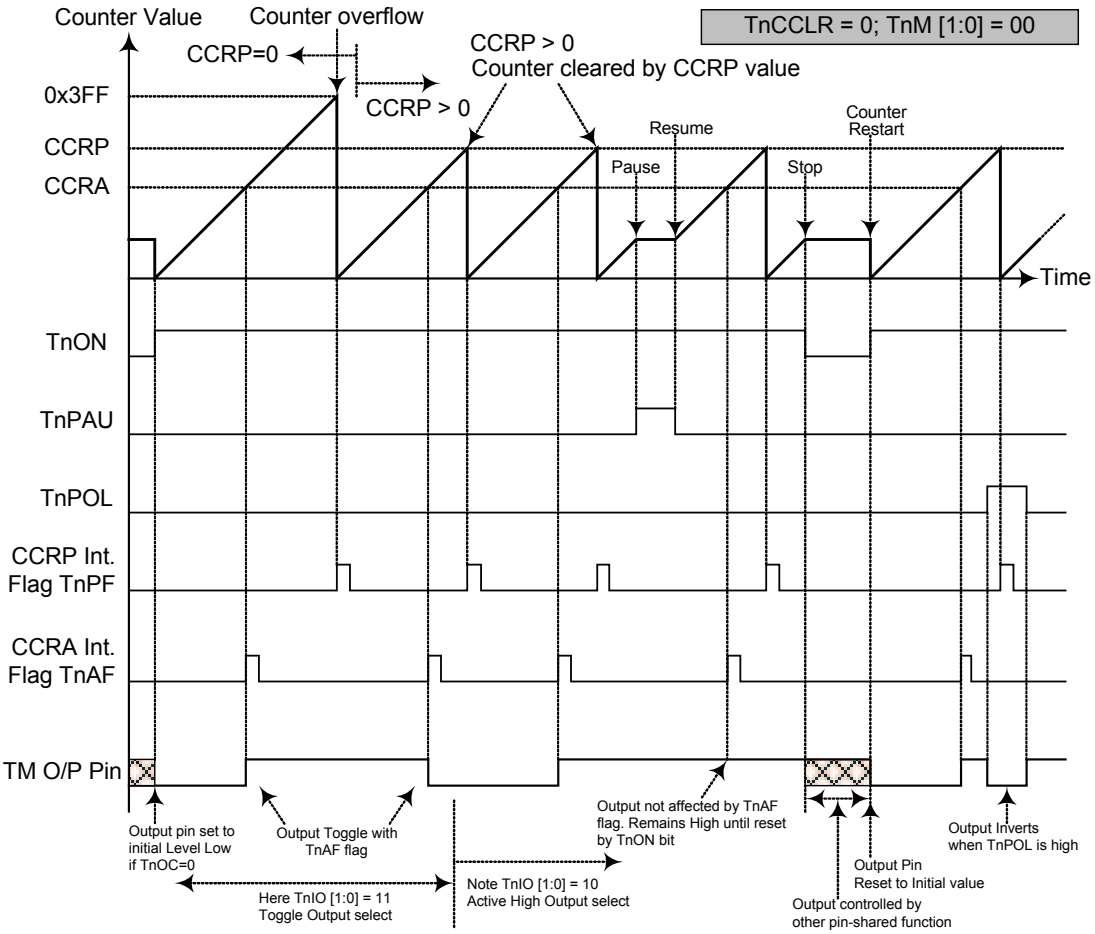
The Compact Type TM can operate in one of three operating modes, Compare Match Output Mode, PWM Mode or Timer/Counter Mode. The operating mode is selected using the TnM1 and TnM0 bits in the TMnC1 register.

Compare Match Output Mode

To select this mode, bits TnM1 and TnM0 in the TMnC1 register, should be set to "00" respectively. In this mode once the counter is enabled and running it can be cleared by three methods. These are a counter overflow, a compare match from Comparator A and a compare match from Comparator P. When the TnCCLR bit is low, there are two ways in which the counter can be cleared. One is when a compare match occurs from Comparator P, the other is when the CCRP bits are all zero which allows the counter to overflow. Here both TnAF and TnPF interrupt request flags for the Comparator A and Comparator P respectively, will both be generated.

If the TnCCLR bit in the TMnC1 register is high then the counter will be cleared when a compare match occurs from Comparator A. However, here only the TnAF interrupt request flag will be generated even if the value of the CCRP bits is less than that of the CCRA registers. Therefore when TnCCLR is high no TnPF interrupt request flag will be generated. If the CCRA bits are all zero, the counter will overflow when its reaches its maximum 10-bit, 3FF Hex, value, however here the TnAF interrupt request flag will not be generated.

As the name of the mode suggests, after a comparison is made, the TM output pin will change state. The TM output pin condition however only changes state when a TnAF interrupt request flag is generated after a compare match occurs from Comparator A. The TnPF interrupt request flag, generated from a compare match occurs from Comparator P, will have no effect on the TM output pin. The way in which the TM output pin changes state are determined by the condition of the TnIO1 and TnIO0 bits in the TMnC1 register. The TM output pin can be selected using the TnIO1 and TnIO0 bits to go high, to go low or to toggle from its present condition when a compare match occurs from Comparator A. The initial condition of the TM output pin, which is setup after the TnON bit changes from low to high, is setup using the TnOC bit. Note that if the TnIO1 and TnIO0 bits are zero then no pin change will take place.

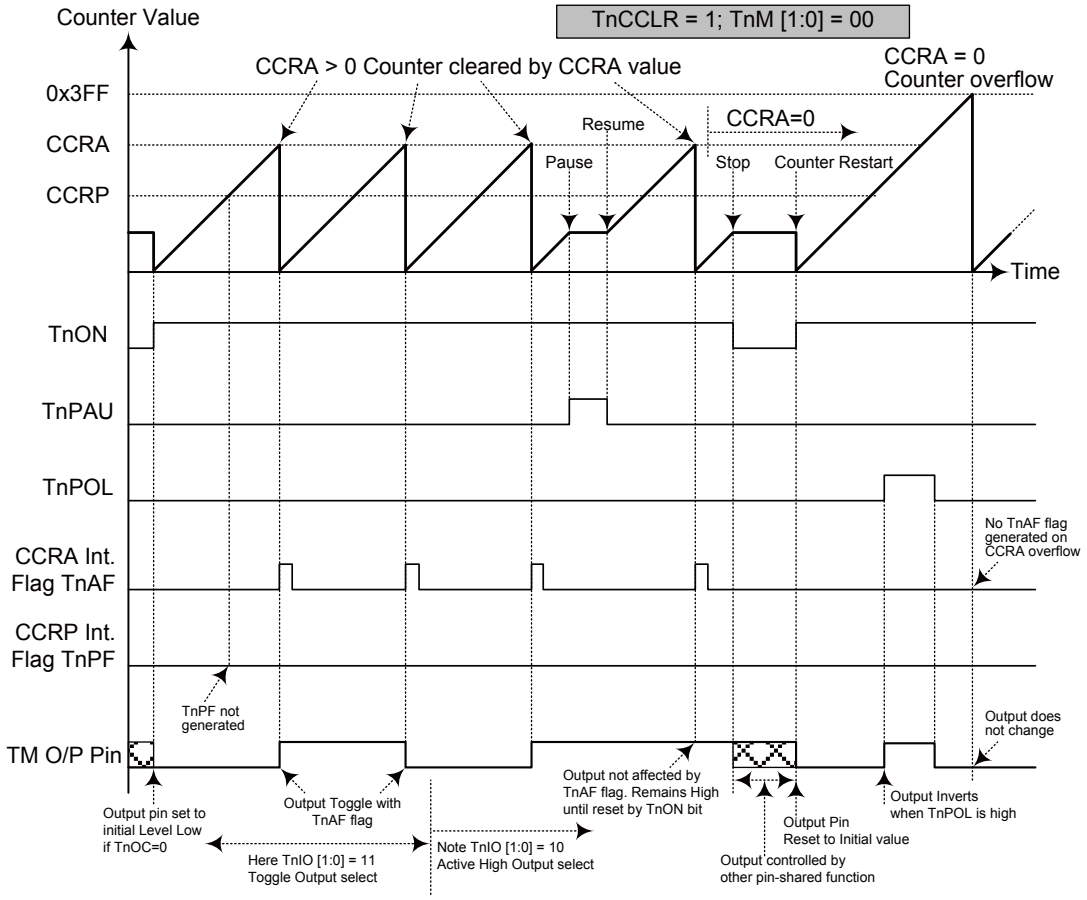


Compare Match Output Mode – TnCCLR=0

Note: 1. With TnCCLR=0, a Comparator P match will clear the counter

2. The TM output pin is controlled only by the TnAF flag

3. The output pin is reset to its initial state by a TnON bit rising edge



Compare Match Output Mode – TnCCLR=1

Note: 1. With TnCCLR=1, a Comparator A match will clear the counter

2. The TM output pin is controlled only by the TnAF flag

3. The output pin is reset to its initial state by a TnON bit rising edge

4. The TnPF flag is not generated when TnCCLR=1

Timer/Counter Mode

To select this mode, bits TnM1 and TnM0 in the TMnC1 register should be set to 11 respectively. The Timer/Counter Mode operates in an identical way to the Compare Match Output Mode generating the same interrupt flags. The exception is that in the Timer/Counter Mode the TM output pin is not used. Therefore the above description and Timing Diagrams for the Compare Match Output Mode can be used to understand its function. As the TM output pin is not used in this mode, the pin can be used as a normal I/O pin or other pin-shared function.

PWM Output Mode

To select this mode, bits TnM1 and TnM0 in the TMnC1 register should be set to 10 respectively. The PWM function within the TM is useful for applications which require functions such as motor control, heating control, illumination control etc. By providing a signal of fixed frequency but of varying duty cycle on the TM output pin, a square wave AC waveform can be generated with varying equivalent DC RMS values.

As both the period and duty cycle of the PWM waveform can be controlled, the choice of generated waveform is extremely flexible. In the PWM mode, the TnCCLR bit has no effect on the PWM operation. Both of the CCRA and CCRP registers are used to generate the PWM waveform, one register is used to clear the internal counter and thus control the PWM waveform frequency, while the other one is used to control the duty cycle. Which register is used to control either frequency or duty cycle is determined using the TnDPX bit in the TMnC1 register. The PWM waveform frequency and duty cycle can therefore be controlled by the values in the CCRA and CCRP registers.

An interrupt flag, one for each of the CCRA and CCRP, will be generated when a compare match occurs from either Comparator A or Comparator P. The TnOC bit in the TMnC1 register is used to select the required polarity of the PWM waveform while the two TnIO1 and TnIO0 bits are used to enable the PWM output or to force the TM output pin to a fixed high or low level. The TnPOL bit is used to reverse the polarity of the PWM output waveform.

CTM, PWM Mode, Edge-aligned Mode, TnDPX=0

CCRP	001b	010b	011b	100b	101b	110b	111b	000b
Period	128	256	384	512	640	768	896	1024
Duty	CCRA							

If f_{SYS}=16MHz, TM clock source is $f_{SYS}/4$, CCRP=100b and CCRA=128,

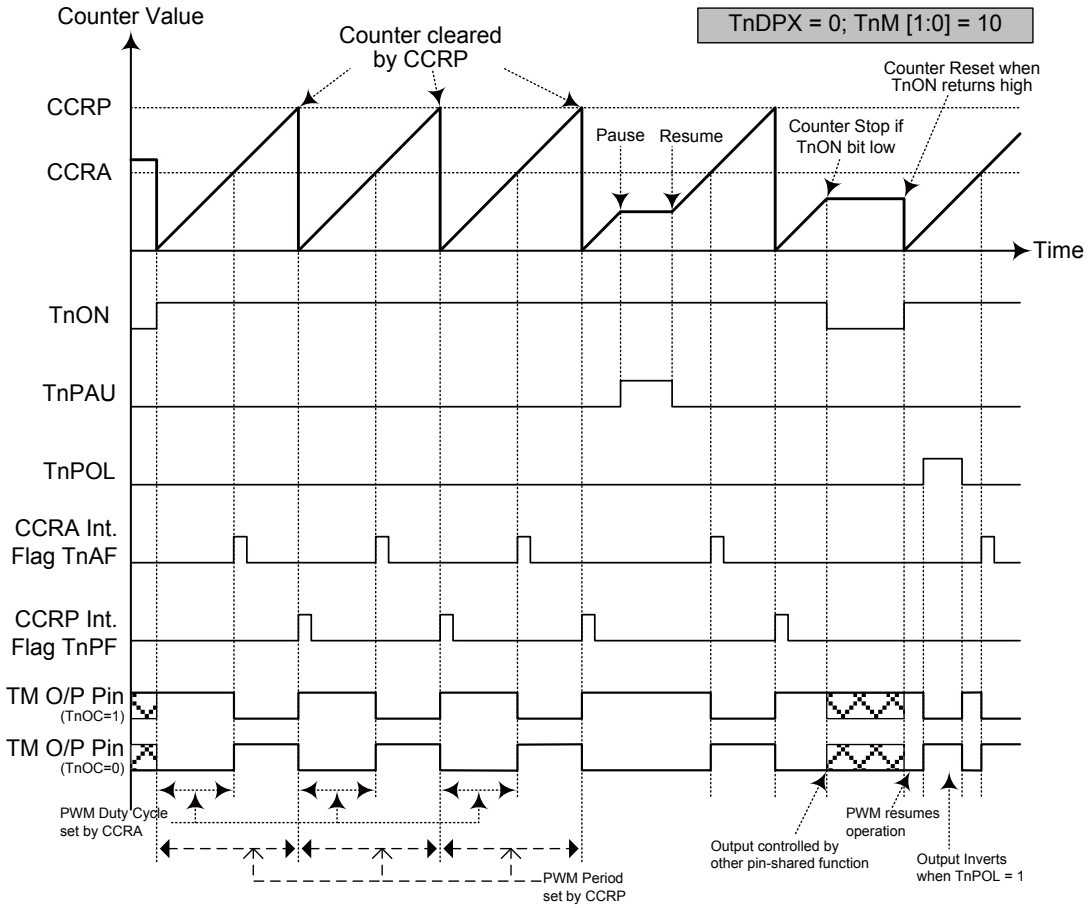
The CTM PWM output frequency=($f_{SYS}/4$)/512=$f_{SYS}/2048$=7.8125 kHz, duty=128/512=25%.

If the Duty value defined by the CCRA register is equal to or greater than the Period value, then the PWM output duty is 100%.

CTM, PWM Mode, Edge-aligned Mode, TnDPX=1

CCRP	001b	010b	011b	100b	101b	110b	111b	000b
Period	CCRA							
Duty	128	256	384	512	640	768	896	1024

The PWM output period is determined by the CCRA register value together with the TM clock while the PWM duty cycle is defined by the CCRP register value.



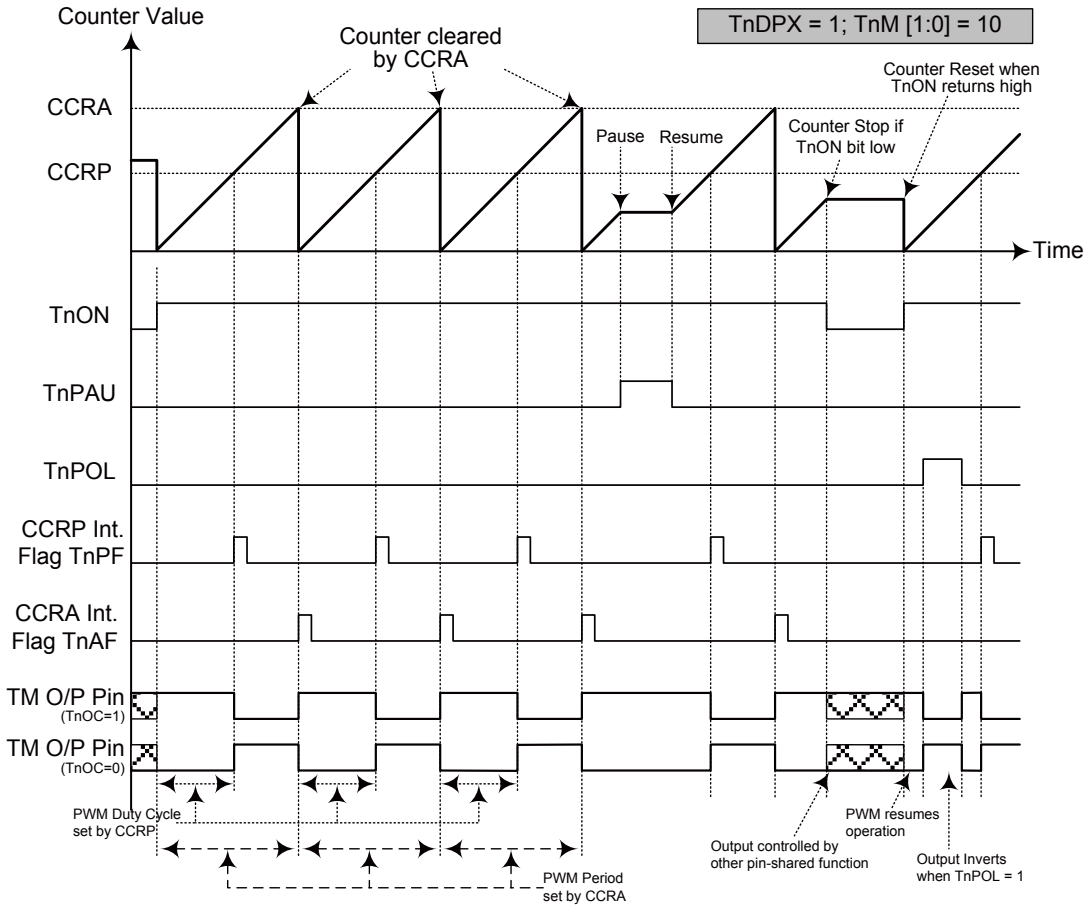
PWM Mode – TnDPX=0

Note: 1. Here TnDPX=0 – Counter cleared by CCRP

2. A counter clear sets the PWM Period

3. The internal PWM function continues even when TnIO [1:0]=00 or 01

4. The TnCCLR bit has no influence on PWM operation



PWM Mode – TnDPX=1

Note: 1. Here TnDPX=1 – Counter cleared by CCRA
2. A counter clear sets the PWM Period
3. The internal PWM function continues even when TnIO [1:0]=00 or 01
4. The TnCCLR bit has no influence on PWM operation

Standard Type TM – STM

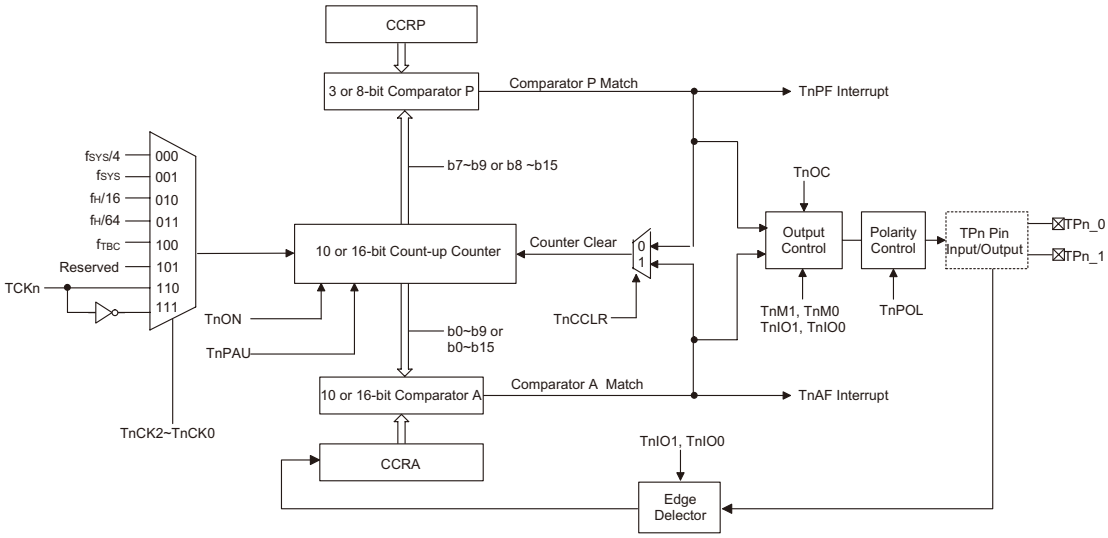
The Standard Type TM contains five operating modes, which are Compare Match Output, Timer/Event Counter, Capture Input, Single Pulse Output and PWM Output modes. The Standard TM can also be controlled with an external input pin and can drive one or two external output pins.

CTM	Name	TM No.	TM Input Pin	TM Output Pin
HT66FB540 HT66FB550 HT66FB560	16-bit STM 10-bit STM	0, 1	TCK0, TCK1	TP0_0, TP0_1 TP1_0, TP1_1

Standard TM Operation

There are two sizes of Standard TMs, one is 10-bits wide and the other is 16-bits wide. At the core is a 10 or 16-bit count-up counter which is driven by a user selectable internal or external clock source. There are also two internal comparators with the names, Comparator A and Comparator P. These comparators will compare the value in the counter with CCRP and CCRA registers. The CCRP comparator is 3 or 8-bits wide whose value is compared the with highest 3 or 8 bits in the counter while the CCRA is the ten or sixteen bits and therefore compares all counter bits.

The only way of changing the value of the 10 or 16-bit counter using the application program, is to clear the counter by changing the TnON bit from low to high. The counter will also be cleared automatically by a counter overflow or a compare match with one of its associated comparators. When these conditions occur, a TM interrupt signal will also usually be generated. The Standard Type TM can operate in a number of different operational modes, can be driven by different clock sources including an input pin and can also control an output pin. All operating setup conditions are selected using relevant internal registers.



Standard Type TM Block Diagram

Standard Type TM Register Description

Overall operation of the Standard TM is controlled using a series of registers. A read only register pair exists to store the internal counter 10 or 16-bit value, while a read/write register pair exists to store the internal 10 or 16-bit CCRA value. The remaining two registers are control registers which setup the different operating and control modes as well as the three or eight CCRP bits.

16-bit Standard TM Register List

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TM0C0	T0PAU	T0CK2	T0CK1	T0CK0	T0ON	—	—	—
TM0C1	T0M1	T0M0	T0IO1	T0IO0	T0OC	T0POL	T0PX	T0CLR
TM0DL	D7	D6	D5	D4	D3	D2	D1	D0
TM0DH	D15	D14	D13	D12	D11	D10	D9	D8
TM0AL	D7	D6	D5	D4	D3	D2	D1	D0
TM0AH	D15	D14	D13	D12	D11	D10	D9	D8
TM0RP	D7	D6	D5	D4	D3	D2	D1	D0

16-bit Standard TM Register List

TM0C0 Register – 16-bit STM

Bit	7	6	5	4	3	2	1	0
Name	T0PAU	T0CK2	T0CK1	T0CK0	T0ON	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	—	—	—
POR	0	0	0	0	0	—	—	—

Bit 7 **T0PAU:** TM0 Counter Pause Control
0: Run
1: Pause

The counter can be paused by setting this bit high. Clearing the bit to zero restores normal counter operation. When in a Pause condition the TM will remain powered up and continue to consume power. The counter will retain its residual value when this bit changes from low to high and resume counting from this value when the bit changes to a low value again.

Bit 6~4 **T0CK2, T0CK1, T0CK0:** Select TM0 Counter clock
000: $f_{SYS/4}$
001: f_{SYS}
010: $f_H/16$
011: $f_H/64$
100: f_{TBC}
101: Reserved
110: TCK0 rising edge clock
111: TCK0 falling edge clock

These three bits are used to select the clock source for the TM. Selecting the Reserved clock input will effectively disable the internal counter. The external pin clock source can be chosen to be active on the rising or falling edge. The clock source f_{SYS} is the system clock, while f_H and f_{TBC} are other internal clocks, the details of which can be found in the oscillator section.

Bit 3 **T0ON:** TM0 Counter On/Off Control
0: Off
1: On

This bit controls the overall on/off function of the TM. Setting the bit high enables the counter to run, clearing the bit disables the TM. Clearing this bit to zero will stop the counter from counting and turn off the TM which will reduce its power consumption. When the bit changes state from low to high the internal counter value will be reset to zero, however when the bit changes from high to low, the internal counter will retain its residual value until the bit returns high again. If the TM is in the Compare Match Output Mode then the TM output pin will be reset to its initial condition, as specified by the T0OC bit, when the T0ON bit changes from low to high.

Bit 2~0 Unimplemented, read as "0"

TM0C1 Register – 16-bit STM

Bit	7	6	5	4	3	2	1	0
Name	T0M1	T0M0	T0IO1	T0IO0	T0OC	T0POL	T0DPX	T0CCLR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 **T0M1~T0M0:** Select TM0 Operating Mode
00: Compare Match Output Mode
01: Capture Input Mode
10: PWM Mode or Single Pulse Output Mode
11: Timer/Counter Mode

These bits setup the required operating mode for the TM. To ensure reliable operation the TM should be switched off before any changes are made to the T0M1 and T0M0 bits. In the Timer/Counter Mode, the TM output pin control must be disabled.

Bit 5~4 **T0IO1~T0IO0:** Select TP0_0, TP0_1 output function
Compare Match Output Mode
00: No change
01: Output low
10: Output high
11: Toggle output
PWM Mode/Single Pulse Output Mode
00: Force inactive state
01: Force active state
10: PWM output
11: Single pulse output
Capture Input Mode
00: Input capture at rising edge of TP0_0, TP0_1
01: Input capture at falling edge of TP0_0, TP0_1
10: Input capture at falling/rising edge of TP0_0, TP0_1
11: Input capture disabled
Timer/counter Mode:
Unused

These two bits are used to determine how the TM output pin changes state when a certain condition is reached. The function that these bits select depends upon in which mode the TM is running.

In the Compare Match Output Mode, the T0IO1 and T0IO0 bits determine how the TM output pin changes state when a compare match occurs from the Comparator A. The TM output pin can be setup to switch high, switch low or to toggle its present state when a compare match occurs from the Comparator A. When the bits are both zero, then no change will take place on the output. The initial value of the TM output pin should be setup using the T0OC bit in the TM0C1 register. Note that the output level requested by the T0IO1 and T0IO0 bits must be different from the initial value setup using the T0OC bit otherwise no change will occur on the TM output pin when a compare match occurs. After the TM output pin changes state it can be reset to its initial level by changing the level of the T0ON bit from low to high.

In the PWM Mode, the T0IO1 and T0IO0 bits determine how the TM output pin changes state when a certain compare match condition occurs. The PWM output function is modified by changing these two bits. It is necessary to only change the values of the T0IO1 and T0IO0 bits only after the TM has been switched off. Unpredictable PWM outputs will occur if the T0IO1 and T0IO0 bits are changed when the TM is running.

Bit 3 **T0OC:** TP0_0, TP0_1 Output control bit
Compare Match Output Mode
0: Initial low
1: Initial high
PWM Mode/Single Pulse Output Mode
0: Active low
1: Active high
This is the output control bit for the TM output pin. Its operation depends upon whether TM is being used in the Compare Match Output Mode or in the PWM Mode/Single Pulse Output Mode. It has no effect if the TM is in the Timer/Counter Mode. In the Compare Match Output Mode it determines the logic level of the TM output pin before a compare match occurs. In the PWM Mode it determines if the PWM signal is active high or active low.

Bit 2 **T0POL:** TP0_0, TP0_1 Output polarity Control
0: Non-invert
1: Invert
This bit controls the polarity of the TP0_0 or TP0_1 output pin. When the bit is set high the TM output pin will be inverted and not inverted when the bit is zero. It has no effect if the TM is in the Timer/Counter Mode.

Bit 1 **T0DPX:** TM0 PWM period/duty Control
0: CCRP - period; CCRA - duty
1: CCRP - duty; CCRA - period
This bit, determines which of the CCRA and CCRP registers are used for period and duty control of the PWM waveform.

Bit 0 **T0CCLR:** Select TM0 Counter clear condition
0: TM0 Comparator P match
1: TM0 Comparator A match
This bit is used to select the method which clears the counter. Remember that the Standard TM contains two comparators, Comparator A and Comparator P, either of which can be selected to clear the internal counter. With the T0CCLR bit set high, the counter will be cleared when a compare match occurs from the Comparator A. When the bit is low, the counter will be cleared when a compare match occurs from the Comparator P or with a counter overflow. A counter overflow clearing method can only be implemented if the CCRP bits are all cleared to zero. The T0CCLR bit is not used in the PWM, Single Pulse or Input Capture Mode.

TM0DL Register – 16-bit STM

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	0	0	0	0

Bit 7~0 **TM0DL:** TM0 Counter Low Byte Register bit 7~bit 0
TM0 16-bit Counter bit 7~bit 0

TM0DH Register – 16-bit STM

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	0	0	0	0

Bit 7~0 **TM0DH:** TM0 Counter High Byte Register bit 7~bit 0
TM0 16-bit Counter bit 15~bit 8

TM0AL Register – 16-bit STM

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **TM0AL:** TM0 CCRA Low Byte Register bit 7~bit 0
TM0 16-bit CCRA bit 7~bit 0

TM0AH Register – 16-bit STM

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **TM0AH:** TM0 CCRA High Byte Register bit 7~bit 0
TM0 16-bit CCRA bit 15~bit 8

TM0RP Register – 16-bit STM

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **TM0RP:** TM0 CCRP Register bit 7~bit 0
TM0 CCRP 8-bit register, compared with the TM0 Counter bit 15~bit 8. Comparator P Match Period
0: 65536 TM0 clocks
1~255: 256×(1~255) TM0 clocks
These eight bits are used to setup the value on the internal CCRP 8-bit register, which are then compared with the internal counter's highest eight bits. The result of this comparison can be selected to clear the internal counter if the T0CCLR bit is set to zero. Setting the T0CCLR bit to zero ensures that a compare match with the CCRP values will reset the internal counter. As the CCRP bits are only compared with the highest eight counter bits, the compare values exist in 256 clock cycle multiples. Clearing all eight bits to zero is in effect allowing the counter to overflow at its maximum value.

10-bit Standard TM Register List

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TM1C0	T1PAU	T1CK2	T1CK1	T1CK0	T1ON	T1RP2	T1RP1	T1RP0
TM1C1	T1M1	T1M0	T1IO1	T1IO0	T1OC	T1POL	T1PX	T1CLR
TM1DL	D7	D6	D5	D4	D3	D2	D1	D0
TM1DH	—	—	—	—	—	—	D9	D8
TM1AL	D7	D6	D5	D4	D3	D2	D1	D0
TM1AH	—	—	—	—	—	—	D9	D8

10-bit Standard TM Register List

TM1C0 Register

Bit	7	6	5	4	3	2	1	0
Name	T1PAU	T1CK2	T1CK1	T1CK0	T1ON	T1RP2	T1RP1	T1RP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **T1PAU:** TM1 Counter Pause Control
0: Run
1: Pause

The counter can be paused by setting this bit high. Clearing the bit to zero restores normal counter operation. When in a Pause condition the TM will remain powered up and continue to consume power. The counter will retain its residual value when this bit changes from low to high and resume counting from this value when the bit changes to a low value again.

Bit 6~4 **T1CK2~T1CK0:** Select TM1 Counter clock
000: $f_{SYS}/4$
001: f_{SYS}
010: $f_H/16$
011: $f_H/64$
100: f_{TBC}
101: Undefined
110: TCK1 rising edge clock
111: TCK1 falling edge clock

These three bits are used to select the clock source for the TM. Selecting the Reserved clock input will effectively disable the internal counter. The external pin clock source can be chosen to be active on the rising or falling edge. The clock source f_{SYS} is the system clock, while f_H and f_{TBC} are other internal clocks, the details of which can be found in the oscillator section.

Bit 3 **T1ON:** TM1 Counter On/Off Control
0: Off
1: On

This bit controls the overall on/off function of the TM. Setting the bit high enables the counter to run, clearing the bit disables the TM. Clearing this bit to zero will stop the counter from counting and turn off the TM which will reduce its power consumption. When the bit changes state from low to high the internal counter value will be reset to zero, however when the bit changes from high to low, the internal counter will retain its residual value until the bit returns high again.

If the TM is in the Compare Match Output Mode then the TM output pin will be reset to its initial condition, as specified by the T1OC bit, when the T1ON bit changes from low to high.

Bit 2~0 **T1RP2~T1RP0:** TMn CCRP 3-bit register, compared with the TMn Counter bit 9~bit 7 Comparator P Match Period
000: 1024 TM1 clocks
001: 128 TM1 clocks
010: 256 TM1 clocks
011: 384 TM1 clocks
100: 512 TM1 clocks
101: 640 TM1 clocks
110: 768 TM1 clocks
111: 896 TM1 clocks

These three bits are used to setup the value on the internal CCRP 3-bit register, which are then compared with the internal counter's highest three bits. The result of this comparison can be selected to clear the internal counter if the T1CCLR bit is set to zero. Setting the T1CCLR bit to zero ensures that a compare match with the CCRP values will reset the internal counter. As the CCRP bits are only compared with the highest three counter bits, the compare values exist in 128 clock cycle multiples. Clearing all three bits to zero is in effect allowing the counter to overflow at its maximum value.

TM1C1 Register

Bit	7	6	5	4	3	2	1	0
Name	T1M1	T1M0	T1IO1	T1IO0	T1OC	T1POL	T1DPX	T1CCLR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 **T1M1~T1M0:** Select TM1 Operating Mode
00: Compare Match Output Mode
01: Capture Input Mode
10: PWM Mode or Single Pulse Output Mode
11: Timer/Counter Mode

These bits setup the required operating mode for the TM. To ensure reliable operation the TM should be switched off before any changes are made to the T1M1 and T1M0 bits. In the Timer/Counter Mode, the TM output pin control must be disabled.

Bit 5~4 **T1IO1~T1IO0:** Select TP1_0, TP1_1 output function
Compare Match Output Mode
00: No change
01: Output low
10: Output high
11: Toggle output
PWM Mode/Single Pulse Output Mode
00: PWM Output inactive state
01: PWM Output active state
10: PWM output
11: Single pulse output
Capture Input Mode
00: Input capture at rising edge of TP1_0, TP1_1
01: Input capture at falling edge of TP1_0, TP1_1
10: Input capture at falling/rising edge of TP1_0, TP1_1
11: Input capture disabled
Timer/counter Mode:
Unused

These two bits are used to determine how the TM output pin changes state when a certain condition is reached. The function that these bits select depends upon in which mode the TM is running. In the Compare Match Output Mode, the T1IO1 and T1IO0 bits determine how the TM output pin changes state when a compare match occurs from the Comparator A. The TM output pin can be setup to switch high, switch low or to toggle its present state when a compare match occurs from the Comparator A. When the bits are both zero, then no change will take place on the output. The initial value of the TM output pin should be setup using the T1OC bit in the TM1C1 register. Note that the output level requested by the T1IO1 and T1IO0 bits must be different from the initial value setup using the T1OC bit otherwise no change will occur on the TM output pin when a compare match occurs. After the TM output pin changes state it can be reset to its initial level by changing the level of the T1ON bit from low to high.

In the PWM Mode, the T1IO1 and T1IO0 bits determine how the TM output pin changes state when a certain compare match condition occurs. The PWM output function is modified by changing these two bits. It is necessary to only change the values of the T1IO1 and T1IO0 bits only after the TM has been switched off. Unpredictable PWM outputs will occur if the T1IO1 and T1IO0 bits are changed when the TM is running.

Bit 3 **T1OC:** TP1_0, TP1_1 Output control bit
Compare Match Output Mode
0: Initial low
1: Initial high
PWM Mode/Single Pulse Output Mode
0: Active low
1: Active high
This is the output control bit for the TM output pin. Its operation depends upon whether TM is being used in the Compare Match Output Mode or in the PWM Mode/Single Pulse Output Mode. It has no effect if the TM is in the Timer/Counter Mode. In the Compare Match Output Mode it determines the logic level of the TM output pin before a compare match occurs. In the PWM Mode it determines if the PWM signal is active high or active low.

Bit 2 **T1POL:** TP1_0, TP1_1 Output polarity Control
0: Non-invert
1: Invert
This bit controls the polarity of the TP1_0 or TP1_1 output pin. When the bit is set high the TM output pin will be inverted and not inverted when the bit is zero. It has no effect if the TM is in the Timer/Counter Mode.

Bit 1 **T1DPX:** TMn PWM period/duty Control
0: CCRP - period; CCRA - duty
1: CCRP - duty; CCRA - period
This bit, determines which of the CCRA and CCRP registers are used for period and duty control of the PWM waveform.

Bit 0 **T1CCLR:** Select TM1 Counter clear condition
0: TM1 Comparator P match
1: TM1 Comparator A match
This bit is used to select the method which clears the counter. Remember that the Standard TM contains two comparators, Comparator A and Comparator P, either of which can be selected to clear the internal counter. With the T1CCLR bit set high, the counter will be cleared when a compare match occurs from the Comparator A. When the bit is low, the counter will be cleared when a compare match occurs from the Comparator P or with a counter overflow. A counter overflow clearing method can only be implemented if the CCRP bits are all cleared to zero. The T1CCLR bit is not used in the PWM, Single Pulse or Input Capture Mode.

TM1DL Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	0	0	0	0

Bit 7~0 **TM1DL:** TM1 Counter Low Byte Register bit 7~bit 0
TMn 10-bit Counter bit 7~bit 0

TM1DH Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R	R
POR	—	—	—	—	—	—	0	0

Bit 7~2 Unimplemented

Bit 1~0 **TM1DH:** TM1 Counter High Byte Register bit 1~bit 0
TMn 10-bit Counter bit 9~bit 8

TM1AL Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **TM1AL:** TM1 CCRA Low Byte Register bit 7~bit 0
TM1 10-bit CCRA bit 7~bit 0

TM1AH Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	0

Bit 7~2 Unimplemented

Bit 1~0 **TM1AH:** TM1 CCRA High Byte Register bit 1~bit 0
TM1 10-bit CCRA bit 9~bit 8

Standard Type TM Operating Modes

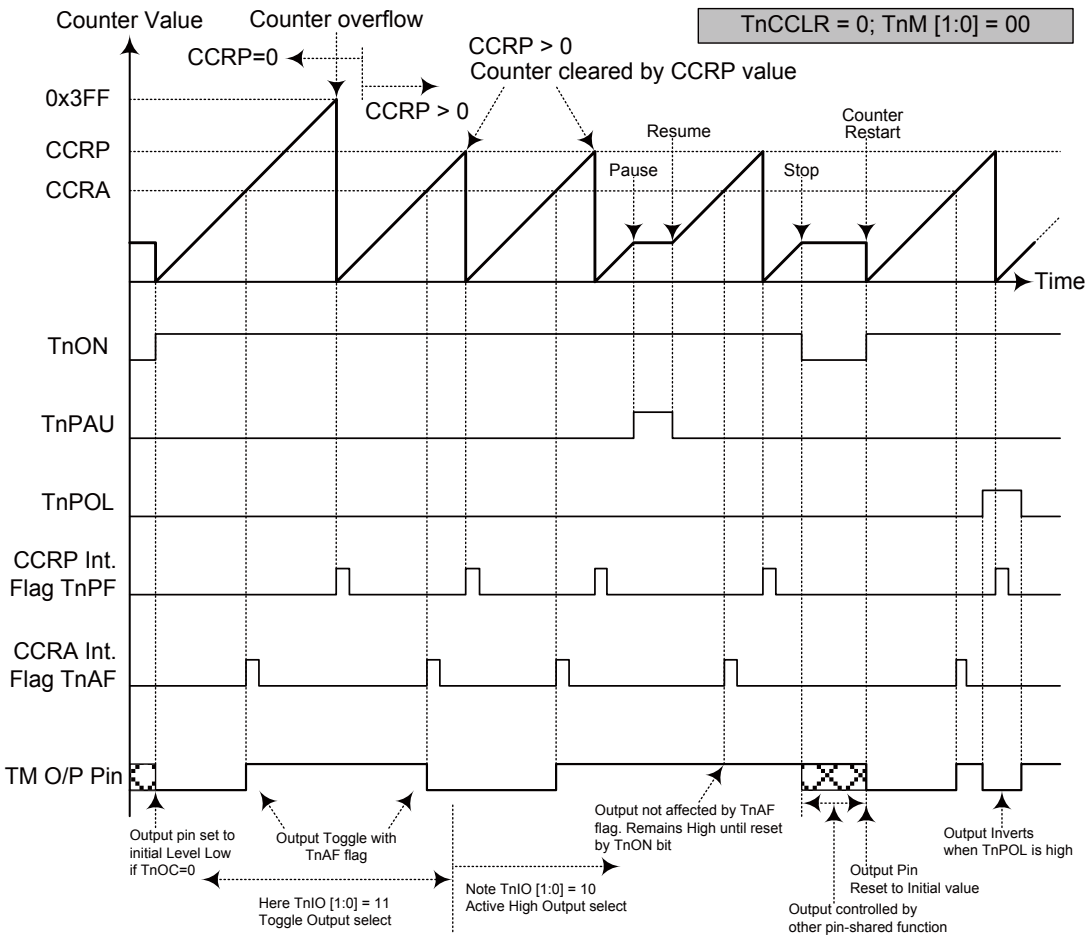
The Standard Type TM can operate in one of five operating modes, Compare Match Output Mode, PWM Output Mode, Single Pulse Output Mode, Capture Input Mode or Timer/Counter Mode. The operating mode is selected using the TnM1 and TnM0 bits in the TMnC1 register.

Compare Output Mode

To select this mode, bits TnM1 and TnM0 in the TMnC1 register, should be set to 00 respectively. In this mode once the counter is enabled and running it can be cleared by three methods. These are a counter overflow, a compare match from Comparator A and a compare match from Comparator P. When the TnCCLR bit is low, there are two ways in which the counter can be cleared. One is when a compare match from Comparator P, the other is when the CCRP bits are all zero which allows the counter to overflow. Here both TnAF and TnPF interrupt request flags for Comparator A and Comparator P respectively, will both be generated.

If the TnCCLR bit in the TMnC1 register is high then the counter will be cleared when a compare match occurs from Comparator A. However, here only the TnAF interrupt request flag will be generated even if the value of the CCRP bits is less than that of the CCRA registers. Therefore when TnCCLR is high no TnPF interrupt request flag will be generated. In the Compare Match Output Mode, the CCRA can not be set to “0”.

As the name of the mode suggests, after a comparison is made, the TM output pin, will change state. The TM output pin condition however only changes state when a TnAF interrupt request flag is generated after a compare match occurs from Comparator A. The TnPF interrupt request flag, generated from a compare match occurs from Comparator P, will have no effect on the TM output pin. The way in which the TM output pin changes state are determined by the condition of the TnIO1 and TnIO0 bits in the TMnC1 register. The TM output pin can be selected using the TnIO1 and TnIO0 bits to go high, to go low or to toggle from its present condition when a compare match occurs from Comparator A. The initial condition of the TM output pin, which is setup after the TnON bit changes from low to high, is setup using the TnOC bit. Note that if the TnIO1 and TnIO0 bits are zero then no pin change will take place.



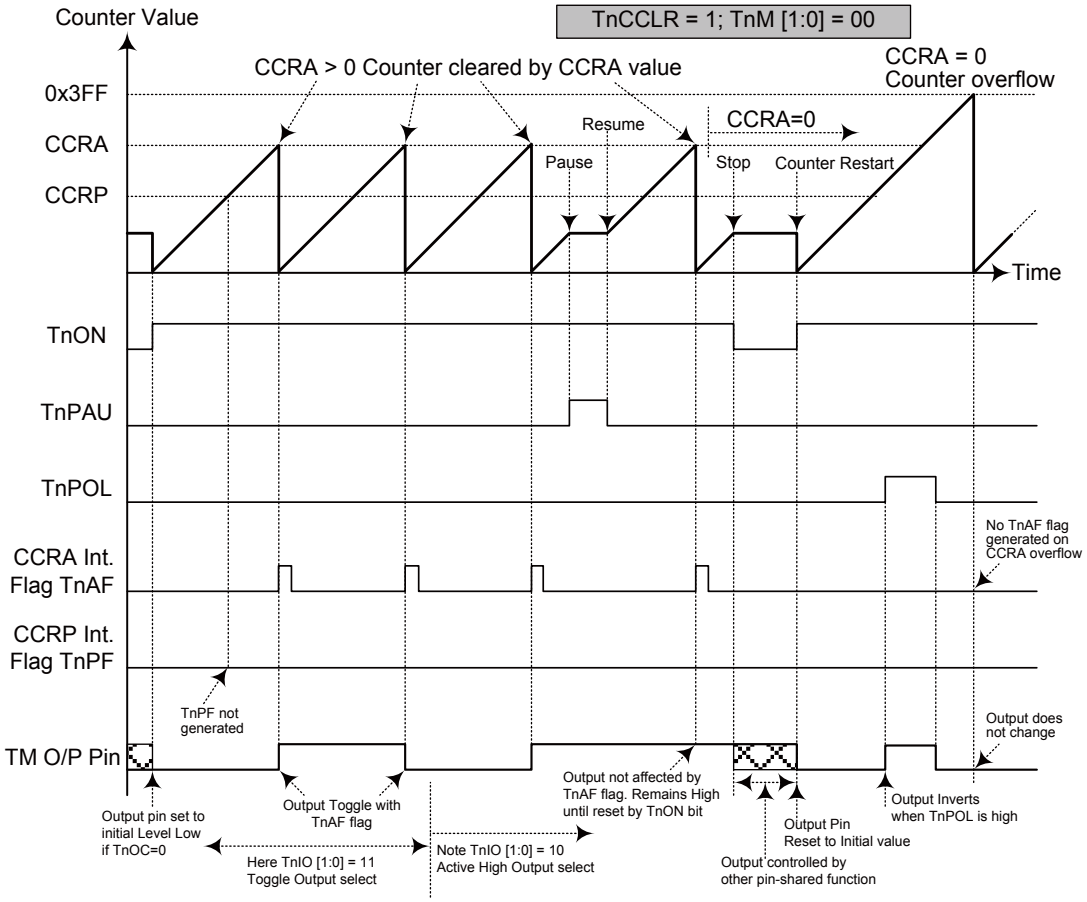
Compare Match Output Mode – TnCCLR=0

Note: 1. With TnCCLR=0 a Comparator P match will clear the counter

2. The TM output pin is controlled only by the TnAF flag

3. The output pin is reset to its initial state by a TnON bit rising edge

4. n=0, 1



Compare Match Output Mode – TnCCLR=1

Note: 1. With TnCCLR=1 a Comparator A match will clear the counter

2. The TM output pin is controlled only by the TnAF flag
3. The output pin is reset to its initial state by a TnON bit rising edge
4. A TnPF flag is not generated when TnCCLR=1

Timer/Counter Mode

To select this mode, bits TnM1 and TnM0 in the TMnC1 register should be set to 11 respectively. The Timer/Counter Mode operates in an identical way to the Compare Match Output Mode generating the same interrupt flags. The exception is that in the Timer/Counter Mode the TM output pin is not used. Therefore the above description and Timing Diagrams for the Compare Match Output Mode can be used to understand its function. As the TM output pin is not used in this mode, the pin can be used as a normal I/O pin or other pin-shared function.

PWM Output Mode

To select this mode, bits TnM1 and TnM0 in the TMnC1 register should be set to 10 respectively and also the TnIO1 and TnIO0 bits should be set to 10 respectively. The PWM function within the TM is useful for applications which require functions such as motor control, heating control, illumination control etc. By providing a signal of fixed frequency but of varying duty cycle on the TM output pin, a square wave AC waveform can be generated with varying equivalent DC RMS values.

As both the period and duty cycle of the PWM waveform can be controlled, the choice of generated waveform is extremely flexible. In the PWM mode, the TnCCLR bit has no effect as the PWM period. Both of the CCRA and CCRP registers are used to generate the PWM waveform, one register is used to clear the internal counter and thus control the PWM waveform frequency, while the other one is used to control the duty cycle. Which register is used to control either frequency or duty cycle is determined using the TnDPX bit in the TMnC1 register. The PWM waveform frequency and duty cycle can therefore be controlled by the values in the CCRA and CCRP registers.

An interrupt flag, one for each of the CCRA and CCRP, will be generated when a compare match occurs from either Comparator A or Comparator P. The TnOC bit in the TMnC1 register is used to select the required polarity of the PWM waveform while the two TnIO1 and TnIO0 bits are used to enable the PWM output or to force the TM output pin to a fixed high or low level. The TnPOL bit is used to reverse the polarity of the PWM output waveform.

16-bit STM, PWM Mode, Edge-aligned Mode, T0DPX=0

CCRP	1~255	000b
Period	CCRP×256	65536
Duty	CCRA	

If f_{SYS}=16MHz, TM clock source select f_{SYS}/4, CCRP=2 and CCRA=128, The STM PWM output frequency=(f_{SYS}/4)/(2×256)=f_{SYS}/2048=7.8125kHz, duty=128/512=25%.

If the Duty value defined by the CCRA register is equal to or greater than the Period value, then the PWM output duty is 100%.

16-bit STM, PWM Mode, Edge-aligned Mode, T0DPX=1

CCRP	1~255	000b
Period	CCRA	
Duty	CCRP x 256	65536

The PWM output period is determined by the CCRA register value together with the TM clock while the PWM duty cycle is defined by the (CCRP×256) except when CCRP value is equal to 000b.

10-bit STM, PWM Mode, Edge-aligned Mode, T1DPX=0

CCRP	001b	010b	011b	100b	101b	110b	111b	000b
Period	128	256	384	512	640	768	896	1024
Duty	CCRA							

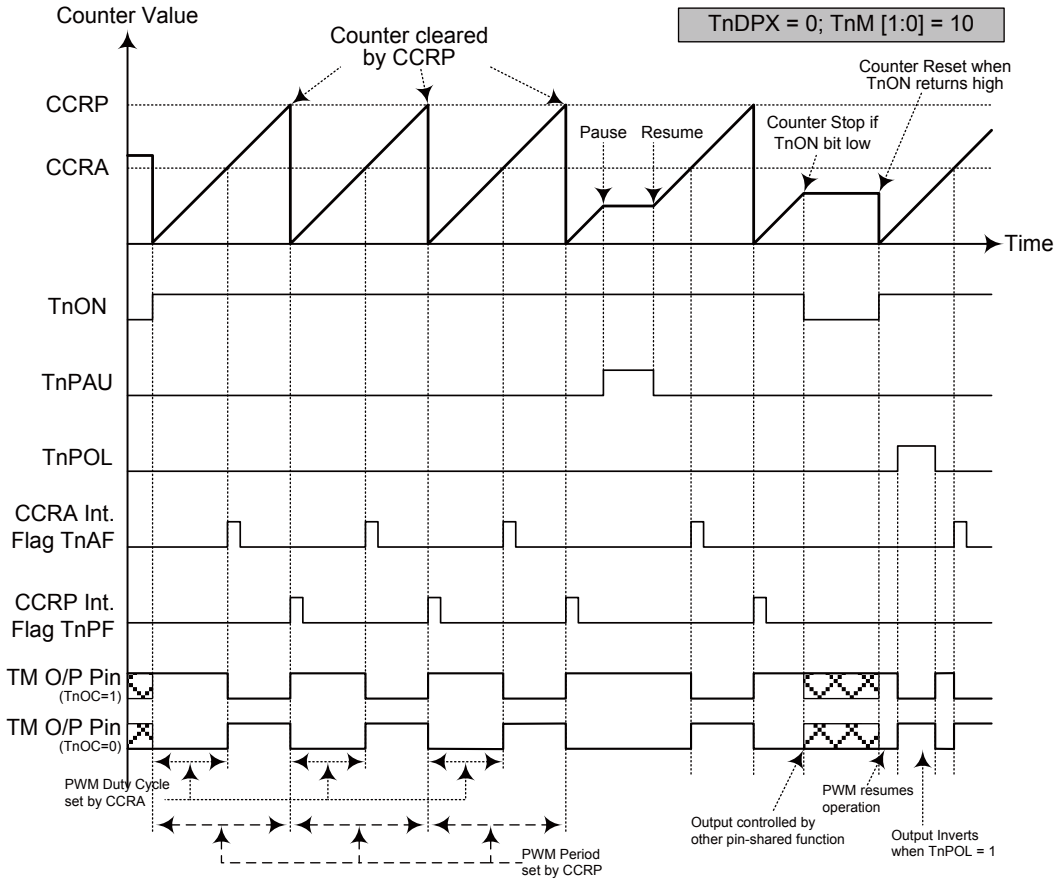
If f_{SYS}=16MHz, TM clock source select f_{SYS}/4, CCRP=100b and CCRA=128, The STM PWM output frequency=(f_{SYS}/4)/512=f_{SYS}/2048=7.8125kHz, duty=128/512=25%.

If the Duty value defined by the CCRA register is equal to or greater than the Period value, then the PWM output duty is 100%.

10-bit STM, PWM Mode, Edge-aligned Mode, T1DPX=1

CCRP	001b	010b	011b	100b	101b	110b	111b	000b
Period	CCRA							
Duty	128	256	384	512	640	768	896	1024

The PWM output period is determined by the CCRA register value together with the TM clock while the PWM duty cycle is defined by the CCRP register value.



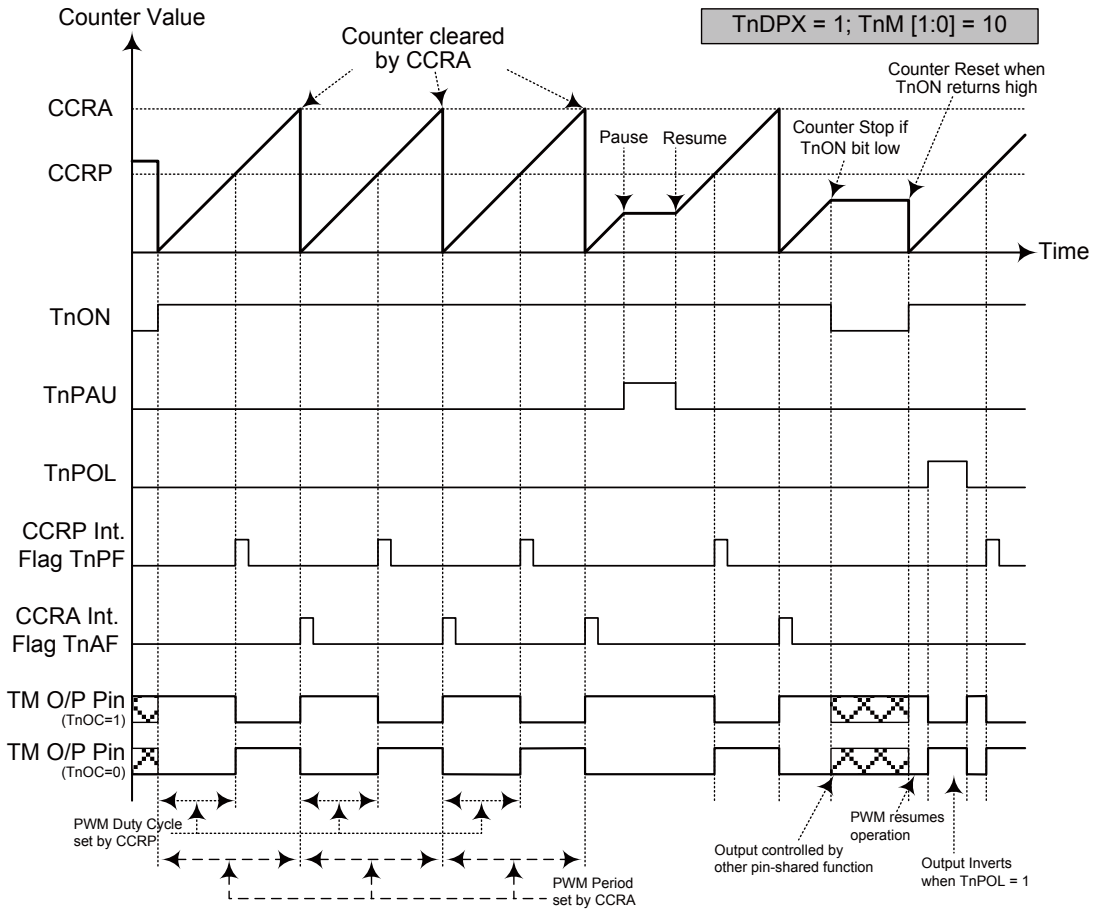
PWM Mode – TnDPX=0

Note: 1. Here TnDPX=0 – Counter cleared by CCRP

2. A counter clear sets the PWM Period

3. The internal PWM function continues running even when TnIO [1:0]=00 or 01

4. The TnCCLR bit has no influence on PWM operation



PWM Mode – TnDPX=1

Note: 1. Here TnDPX=1 – Counter cleared by CCRA

2. A counter clear sets the PWM Period

3. The internal PWM function continues even when TnIO [1:0]=00 or 01

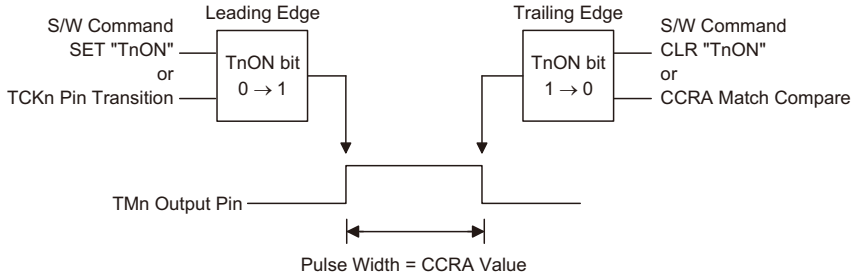
4. The TnCCLR bit has no influence on PWM operation

Single Pulse Mode

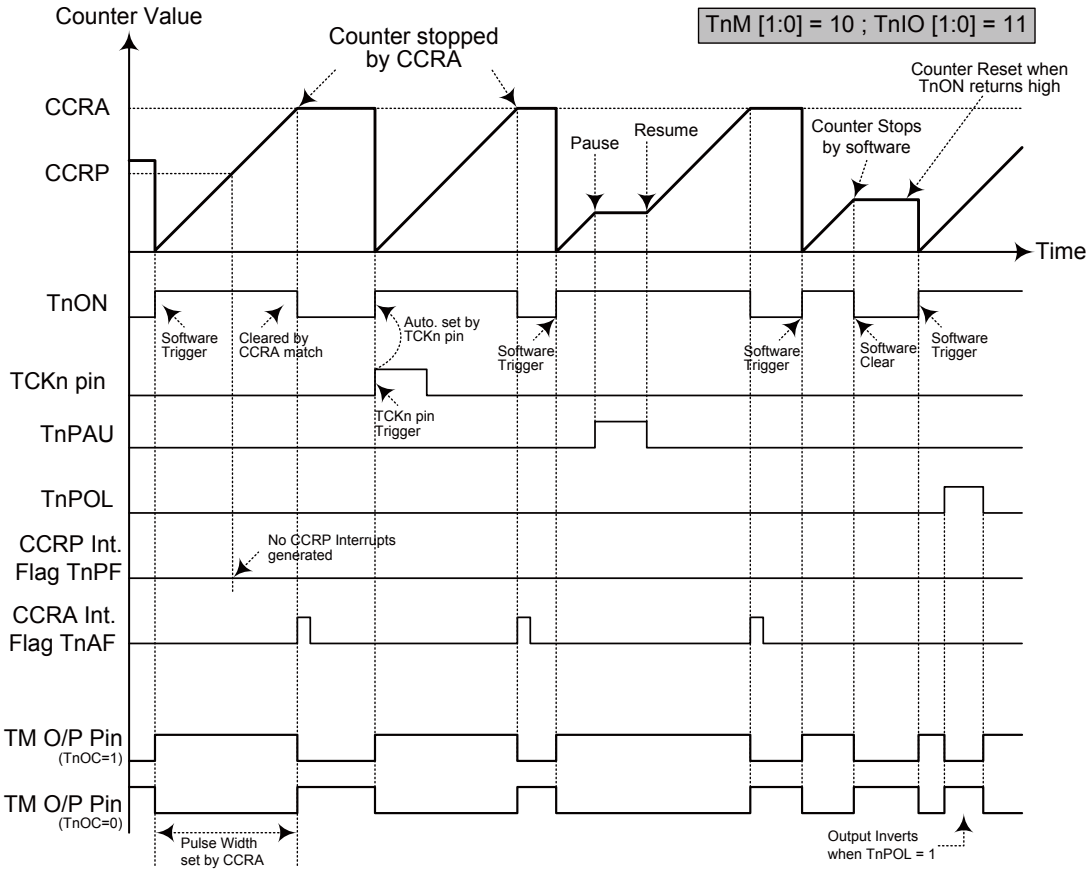
To select this mode, bits TnM1 and TnM0 in the TMnC1 register should be set to 10 respectively and also the TnIO1 and TnIO0 bits should be set to 11 respectively. The Single Pulse Output Mode, as the name suggests, will generate a single shot pulse on the TM output pin.

The trigger for the pulse output leading edge is a low to high transition of the TnON bit, which can be implemented using the application program. However in the Single Pulse Mode, the TnON bit can also be made to automatically change from low to high using the external TCKn pin, which will in turn initiate the Single Pulse output. When the TnON bit transitions to a high level, the counter will start running and the pulse leading edge will be generated. The TnON bit should remain high when the pulse is in its active state. The generated pulse trailing edge will be generated when the TnON bit is cleared to zero, which can be implemented using the application program or when a compare match occurs from Comparator A.

However a compare match from Comparator A will also automatically clear the TnON bit and thus generate the Single Pulse output trailing edge. In this way the CCRA value can be used to control the pulse width. A compare match from Comparator A will also generate a TM interrupt. The counter can only be reset back to zero when the TnON bit changes from low to high when the counter restarts. In the Single Pulse Mode CCRP is not used. The TnCCLR and TnDPX bits are not used in this Mode.



Single Pulse Generation



Single Pulse Mode

Note: 1. Counter stopped by CCRA

2. CCRP is not used

3. The pulse is triggered by the TCKn pin or by setting the TnON bit high

4. A TCKn pin active edge will automatically set the TnON bit hight

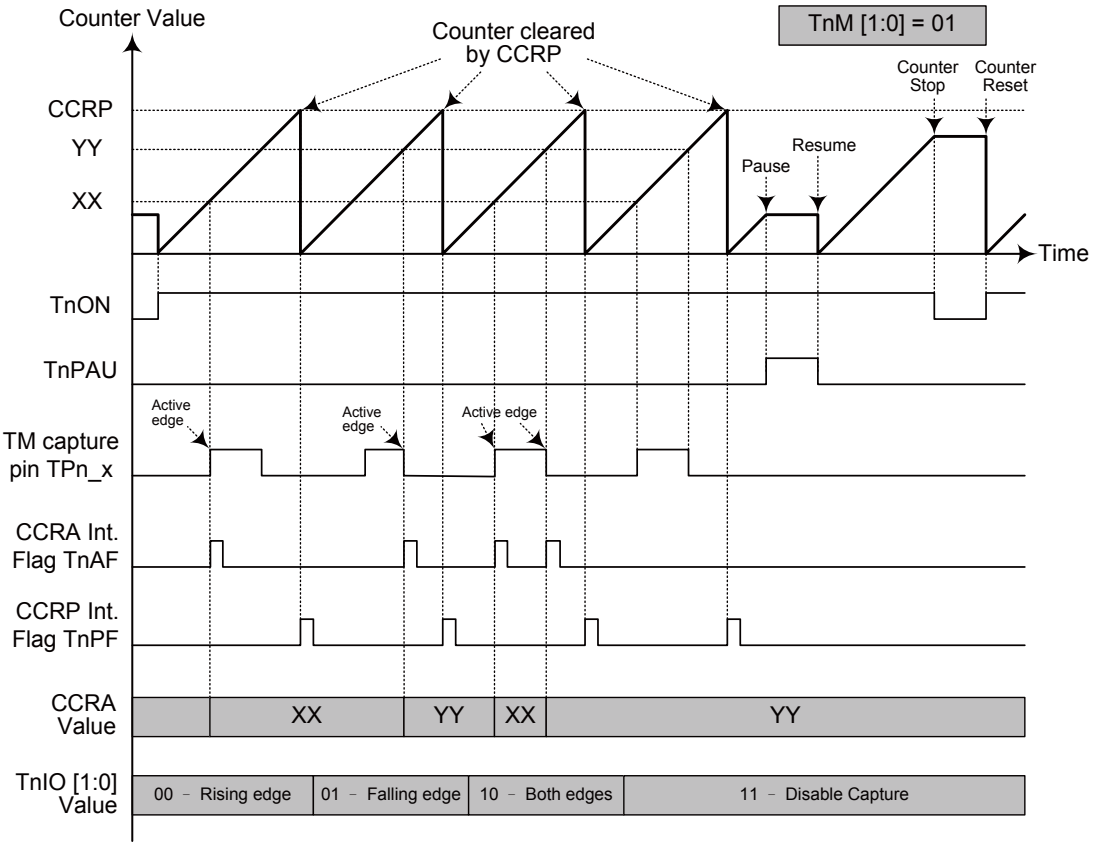
5. In the Single Pulse Mode, TnIO [1:0] must be set to “11” and can not be changed.

Capture Input Mode

To select this mode bits TnM1 and TnM0 in the TMnC1 register should be set to 01 respectively. This mode enables external signals to capture and store the present value of the internal counter and can therefore be used for applications such as pulse width measurements. The external signal is supplied on the TPn_0 or TPn_1 pin, whose active edge can be either a rising edge, a falling edge or both rising and falling edges; the active edge transition type is selected using the TnIO1 and TnIO0 bits in the TMnC1 register. The counter is started when the TnON bit changes from low to high which is initiated using the application program.

When the required edge transition appears on the TPn_0 or TPn_1 pin the present value in the counter will be latched into the CCRA registers and a TM interrupt generated. Irrespective of what events occur on the TPn_0 or TPn_1 pin the counter will continue to free run until the TnON bit changes from high to low. When a CCRP compare match occurs the counter will reset back to zero; in this way the CCRP value can be used to control the maximum counter value. When a CCRP compare match occurs from Comparator P, a TM interrupt will also be generated. Counting the number of overflow interrupt signals from the CCRP can be a useful method in measuring long pulse widths. The TnIO1 and TnIO0 bits can select the active trigger edge on the TPn_0 or TPn_1 pin to be a rising edge, falling edge or both edge types. If the TnIO1 and TnIO0 bits are both set high, then no capture operation will take place irrespective of what happens on the TPn_0 or TPn_1 pin, however it must be noted that the counter will continue to run.

As the TPn_0 or TPn_1 pin is pin shared with other functions, care must be taken if the TM is in the Input Capture Mode. This is because if the pin is setup as an output, then any transitions on this pin may cause an input capture operation to be executed. The TnCCLR and TnDPX bits are not used in this Mode.



Capture Input Mode

Note: 1. TnM [1:0]=01 and active edge set by the TnIO [1:0] bits

2. A TM Capture input pin active edge transfers the counter value to CCRA
3. TnCCLR bit not used
4. No output function – TnOC and TnPOL bits are not used
5. CCRP determines the counter value and the counter has a maximum count value when CCRP is equal to zero.

Analog to Digital Converter

The need to interface to real world analog signals is a common requirement for many electronic systems. However, to properly process these signals by a microcontroller, they must first be converted into digital signals by A/D converters. By integrating the A/D conversion electronic circuitry into the microcontroller, the need for external components is reduced significantly with the corresponding follow-on benefits of lower costs and reduced component space requirements.

A/D Overview

The devices contains a multi-channel analog to digital converter which can directly interface to external analog signals, such as that from sensors or other control signals and convert these signals directly into either a 12-bit digital value.

Part No.	Input Channels	A/D Channel Select Bits	Input Pins
HT66FB540	8	ACS4, ACS2~ACS0	AN0~AN7
HT66FB550 HT66FB560	16	ACS4~ACS0	AN0~AN15

The accompanying block diagram shows the overall internal structure of the A/D converter, together with its associated registers.

A/D Converter Register Description

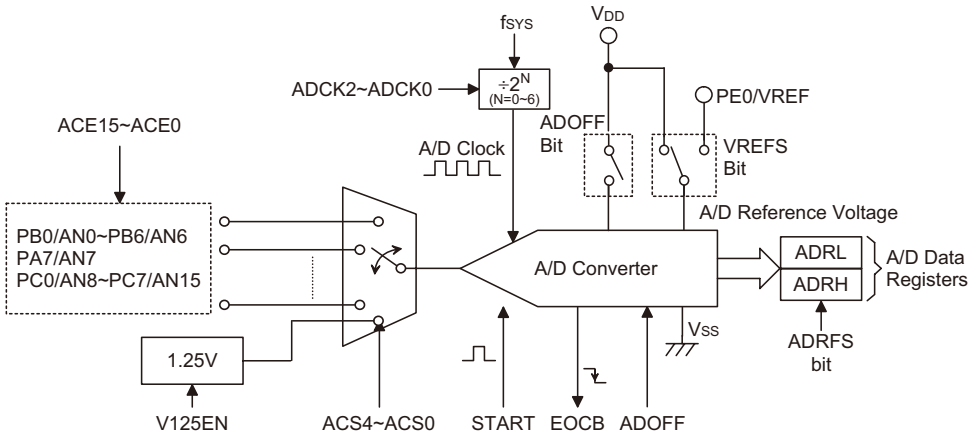
Overall operation of the A/D converter is controlled using seven registers. A read only register pair exists to store the ADC data 12-bit value. The remaining five registers are control registers which setup the operating and control function of the A/D converter.

Register Name	Bit							
	7	6	5	4	3	2	1	0
ADRL(ADRFS=0)	D3	D2	D1	D0	—	—	—	—
ADRL(ADRFS=1)	D7	D6	D5	D4	D3	D2	D1	D0
ADRH(ADRFS=0)	D11	D10	D9	D8	D7	D6	D5	D4
ADRH(ADRFS=1)	—	—	—	—	D11	D10	D9	D8
ADCR0	START	EOCB	ADOFF	ADRFS	—	ACS2	ACS1	ACS0
ADCR1	ACS4	V125EN	—	VREFS	—	ADCK2	ADCK1	ADCK0
ACER0	ACE7	ACE6	ACE5	ACE4	ACE3	ACE2	ACE1	ACE0

HT66FB540 A/D Converter Register List

Register Name	Bit							
	7	6	5	4	3	2	1	0
ADRL(ADRFS=0)	D3	D2	D1	D0	—	—	—	—
ADRL(ADRFS=1)	D7	D6	D5	D4	D3	D2	D1	D0
ADRH(ADRFS=0)	D11	D10	D9	D8	D7	D6	D5	D4
ADRH(ADRFS=1)	—	—	—	—	D11	D10	D9	D8
ADCR0	START	EOCB	ADOFF	ADRFS	ACS3	ACS2	ACS1	ACS0
ADCR1	ACS4	V125EN	—	VREFS	—	ADCK2	ADCK1	ADCK0
ACER0	ACE7	ACE6	ACE5	ACE4	ACE3	ACE2	ACE1	ACE0
ACER1	ACE15	ACE14	ACE13	ACE12	ACE11	ACE10	ACE9	ACE8

HT66FB550/HT66FB560 A/D Converter Register List



A/D Converter Structure

A/D Converter Data Registers – ADRL, ADRH

As the devices contain an internal 12-bit A/D converter, they require two data registers to store the converted value.

These are a high byte register, known as ADRH, and a low byte register, known as ADRL. After the conversion process takes place, these registers can be directly read by the microcontroller to obtain the digitised conversion value. As only 12 bits of the 16-bit register space is utilised, the format in which the data is stored is controlled by the ADRFS bit in the ADCR0 register as shown in the accompanying table. D0~D11 are the A/D conversion result data bits. Any unused bits will be read as zero.

ADRFS	ADRH								ADRL							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0
1	0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

A/D Data Registers

A/D Converter Control Registers – ADCR0, ADCR1, ACER0, ACER1

To control the function and operation of the A/D converter, five control registers known as ADCR0, ADCR1, ACER0 and ACER1 are provided. These 8-bit registers define functions such as the selection of which analog channel is connected to the internal A/D converter, the digitised data format, the A/D clock source as well as controlling the start function and monitoring the A/D converter end of conversion status. The ACS3~ACS0 bits in the ADCR0 register and ACS4 bit is the ADCR1 register define the ADC input channel number. As the devices contain only one actual analog to digital converter hardware circuit, each of the individual 8 analog inputs must be routed to the converter. It is the function of the ACS4 and ACS3~ACS0 bits to determine which analog channel input pins or internal 1.25V is actually connected to the internal A/D converter.

The ACER1~ACER0 control registers contain the ACER15~ACER0 bits which determine which pins on PA7, Port B and Port C are used as analog inputs for the A/D converter input and which pins are not to be used as the A/D converter input. Setting the corresponding bit high will select the A/D input function, clearing the bit to zero will select either the I/O or other pin-shared function. When the pin is selected to be an A/D input, its original function whether it is an I/O or other pin-shared function will be removed. In addition, any internal pull-high resistors connected to these pins will be automatically removed if the pin is selected to be an A/D input.

ADCR0 Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	START	EOCB	ADOFF	ADRFS	—	ACS2	ACS1	ACS0
R/W	R/W	R	R/W	R/W	R	R/W	R/W	R/W
POR	0	1	1	0	0	0	0	0

Bit 7 **START:** Start the A/D conversion
0→1→0: start
0→1: reset the A/D converter and set EOCB to "1"
This bit is used to initiate an A/D conversion process. The bit is normally low but if set high and then cleared low again, the A/D converter will initiate a conversion process. When the bit is set high the A/D converter will be reset.

Bit 6 **EOCB:** End of A/D conversion flag
0: A/D conversion ended
1: A/D conversion in progress
This read only flag is used to indicate when an A/D conversion process has completed. When the conversion process is running, the bit will be high.

Bit 5 **ADOFF** : ADC module power on/off control bit
0: ADC module power on
1: ADC module power off
This bit controls the power to the A/D internal function. This bit should be cleared to zero to enable the A/D converter. If the bit is set high then the A/D converter will be switched off reducing the devices power consumption. As the A/D converter will consume a limited amount of power, even when not executing a conversion, this may be an important consideration in power sensitive battery powered applications.
Note: 1. it is recommended to set ADOFF=1 before entering IDLE/SLEEP Mode for saving power.
2. ADOFF=1 will power down the ADC module.

Bit 4 **ADRFS:** ADC Data Format Control
0: ADC Data MSB is ADRH bit 7, LSB is ADRL bit 4
1: ADC Data MSB is ADRH bit 3, LSB is ADRL bit 0
This bit controls the format of the 12-bit converted A/D value in the two A/D data registers. Details are provided in the A/D data register section.

Bit 3 Unimplemented

Bit 2~0 **ACS2, ACS1, ACS0:** Select A/D channel (when ACS4 is "0")
000: AN0
001: AN1
010: AN2
011: AN3
100: AN4
101: AN5
110: AN6
111: AN7
These are the A/D channel select control bits. As there is only one internal hardware A/D converter each of the eight A/D inputs must be routed to the internal converter using these bits. If bit ACS4 in the ADCR1 register is set high then the internal 1.25V will be routed to the A/D Converter.

• **HT66FB550/HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	START	EOCB	ADOFF	ADRFS	ACS3	ACS2	ACS1	ACS0
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	1	1	0	0	0	0	0

Bit 7 **START:** Start the A/D conversion
0→1→0: start
0→1: reset the A/D converter and set EOCB to "1"
This bit is used to initiate an A/D conversion process. The bit is normally low but if set high and then cleared low again, the A/D converter will initiate a conversion process. When the bit is set high the A/D converter will be reset.

Bit 6 **EOCB:** End of A/D conversion flag
0: A/D conversion ended
1: A/D conversion in progress
This read only flag is used to indicate when an A/D conversion process has completed. When the conversion process is running, the bit will be high.

Bit 5 **ADOFF** : ADC module power on/off control bit
0: ADC module power on
1: ADC module power off
This bit controls the power to the A/D internal function. This bit should be cleared to zero to enable the A/D converter. If the bit is set high then the A/D converter will be switched off reducing the devices power consumption. As the A/D converter will consume a limited amount of power, even when not executing a conversion, this may be an important consideration in power sensitive battery powered applications.
Note: 1. it is recommended to set ADOFF=1 before entering IDLE/SLEEP Mode for saving power.
2. ADOFF=1 will power down the ADC module.

Bit 4 **ADRFS:** ADC Data Format Control
0: ADC Data MSB is ADRH bit 7, LSB is ADRL bit 4
1: ADC Data MSB is ADRH bit 3, LSB is ADRL bit 0
This bit controls the format of the 12-bit converted A/D value in the two A/D data registers. Details are provided in the A/D data register section.

Bit 3~0 **ACS3, ACS2, ACS1, ACS0:** Select A/D channel (when ACS4 is "0")
0000: AN0
0001: AN1
0010: AN2
0011: AN3
0100: AN4
0101: AN5
0110: AN6
0111: AN7
1000: AN8
1001: AN9
1010: AN10
1011: AN11
1100: AN12
1101: AN13
1110: AN14
1111: AN15
These are the A/D channel select control bits. As there is only one internal hardware A/D converter each of the eight A/D inputs must be routed to the internal converter using these bits. If bit ACS4 in the ADCR1 register is set high then the internal 1.25V will be routed to the A/D Converter.

ADCR1 Register

Bit	7	6	5	4	3	2	1	0
Name	ACS4	V125EN	—	VREFS	—	ADCK2	ADCK1	ADCK0
R/W	R/W	R/W	R	R/W	R	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **ACS4:** Select Internal 1.25V bandgap voltage as ADC input
0: Disable
1: Enable
This bit enables the1.25V bandgap voltage to be connected to the A/D converter. The V125EN bit must first have been set to enable the bandgap circuit 1.25V voltage to be used by the A/D converter. When the ACS4 bit is set high, the bandgap 1.25V voltage will be routed to the A/D converter and the other A/D input channels disconnected.

Bit 6 **V125EN:** Internal 1.25V Control
0: Disable
1: Enable
This bit controls the internal Bandgap circuit on/off function to the A/D converter. When the bit is set high the 1.25V bandgap voltage can be used as an A/D converter input. If the 1.25V bandgap voltage is not used by the A/D converter and the LVR/LVD function is disabled then the bandgap reference circuit will be automatically switched off to conserve power. When the 1.25V bandgap voltage is switched on for use by the A/D converter, a time t_{BG} should be allowed for the bandgap circuit to stabilise before implementing an A/D conversion.

Bit 5 Unimplemented

Bit 4 **VREFS:** Select ADC reference voltage
0: Internal ADC power
1: VREF pin
This bit is used to select the reference voltage for the A/D converter. If the bit is high, then the A/D converter reference voltage is supplied on the external VREF pin. If the pin is low, then the internal reference is used which is taken from the power supply pin, VDD.

Bit 3 Unimplemented

Bit 2~0 **ADCK2, ADCK1, ADCK0:** Select ADC clock source
000: f_{SYS}
001: $f_{SYS}/2$
010: $f_{SYS}/4$
011: $f_{SYS}/8$
100: $f_{SYS}/16$
101: $f_{SYS}/32$
110: $f_{SYS}/64$
111: Undefined
These three bits are used to select the clock source for the A/D converter.

ACER0 Register

Bit	7	6	5	4	3	2	1	0
Name	ACE7	ACE6	ACE5	ACE4	ACE3	ACE2	ACE1	ACE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

Bit 7 **ACE7:** Define PA7 is A/D input or not
0: Not A/D input
1: A/D input, AN7

Bit 6 **ACE6:** Define PB6 is A/D input or not
0: Not A/D input
1: A/D input, AN6

Bit 5 **ACE5:** Define PB5 is A/D input or not
0: Not A/D input
1: A/D input, AN5

Bit 4 **ACE4:** Define PB4 is A/D input or not
0: Not A/D input
1: A/D input, AN4

Bit 3 **ACE3:** Define PB3 is A/D input or not
0: Not A/D input
1: A/D input, AN3

Bit 2 **ACE2:** Define PB2 is A/D input or not
0: Not A/D input
1: A/D input, AN2

Bit 1 **ACE1:** Define PB1 is A/D input or not
0: Not A/D input
1: A/D input, AN1

Bit 0 **ACE0:** Define PB0 is A/D input or not
0: Not A/D input
1: A/D input, AN0

ACER1 Register

- **HT66FB550/HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	ACE15	ACE14	ACE13	ACE12	ACE11	ACE10	ACE9	ACE8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

Bit 7 **ACE15:** Define PC7 is A/D input or not
0: Not A/D input
1: A/D input, AN15

Bit 6 **ACE14:** Define PC6 is A/D input or not
0: Not A/D input
1: A/D input, AN14

Bit 5 **ACE13:** Define PC5 is A/D input or not
0: Not A/D input
1: A/D input, AN13

Bit 4 **ACE12:** Define PC4 is A/D input or not
0: Not A/D input
1: A/D input, AN12

Bit 3 **ACE11:** Define PC3 is A/D input or not
0: Not A/D input
1: A/D input, AN11

Bit 2 **ACE10:** Define PC2 is A/D input or not
0: Not A/D input
1: A/D input, AN10

Bit 1 **ACE9:** Define PC1 is A/D input or not
0: Not A/D input
1: A/D input, AN9

Bit 0 **ACE8:** Define PC0 is A/D input or not
0: Not A/D input
1: A/D input, AN8

A/D Operation

The START bit in the ADCR0 register is used to start and reset the A/D converter. When the microcontroller sets this bit from low to high and then low again, an analog to digital conversion cycle will be initiated. When the START bit is brought from low to high but not low again, the EOCB bit in the ADCR0 register will be set high and the analog to digital converter will be reset. It is the START bit that is used to control the overall start operation of the internal analog to digital converter.

The EOCB bit in the ADCR0 register is used to indicate when the analog to digital conversion process is complete. This bit will be automatically set to "0" by the microcontroller after a conversion cycle has ended. In addition, the corresponding A/D interrupt request flag will be set in the interrupt control register, and if the interrupts are enabled, an appropriate internal interrupt signal will be generated. This A/D internal interrupt signal will direct the program flow to the associated A/D internal interrupt address for processing. If the A/D internal interrupt is disabled, the microcontroller can be used to poll the EOCB bit in the ADCR0 register to check whether it has been cleared as an alternative method of detecting the end of an A/D conversion cycle.

The clock source for the A/D converter, which originates from the system clock f_{SYS}, can be chosen to be either f_{SYS} or a subdivided version of f_{SYS}. The division ratio value is determined by the ADCK2~ADCK0 bits in the ADCR1 register.

Although the A/D clock source is determined by the system clocky, f_{SYS}, and by bits ADCK2~ADCK0, there are some limitations on the maximum A/D clock source speed that can be selected. As the minimum value of permissible A/D clock period, t_{AD}, is 0.5μs, care must be taken for system clock frequencies equal to or greater than 4MHz. For example, if the system clock operates at a frequency of 4MHz, the ADCK2~ADCK0 bits should not be set to "000". Doing so will give A/D clock periods that are less than the minimum A/D clock period which may result in inaccurate A/D conversion values. Refer to the following table for examples, where values marked with an asterisk * show where, depending upon the devices, special care must be taken, as the values may be less than the specified minimum A/D Clock Period.

f_{SYS}	A/D Clock Period (t_{AD})							
	ADCK2, ADCK1, ADCK0 =000 (f_{SYS})	ADCK2, ADCK1, ADCK0 =001 (f_{SYS}/2)	ADCK2, ADCK1, ADCK0 =010 (f_{SYS}/4)	ADCK2, ADCK1, ADCK0 =011 (f_{SYS}/8)	ADCK2, ADCK1, ADCK0 =100 (f_{SYS}/16)	ADCK2, ADCK1, ADCK0 =101 (f_{SYS}/32)	ADCK2, ADCK1, ADCK0 =110 (f_{SYS}/64)	ADCK2, ADCK1, ADCK0 =111
1MHz	1μs	2μs	4μs	8μs	16μs	32μs	64μs	Undefined
2MHz	500ns	1μs	2μs	4μs	8μs	16μs	32μs	Undefined
4MHz	250ns*	500ns	1μs	2μs	4μs	8μs	16μs	Undefined
8MHz	125ns*	250ns*	500ns	1μs	2μs	4μs	8μs	Undefined
12MHz	83ns*	167ns*	333ns*	667ns	1.33μs	2.67μs	5.33μs	Undefined
16MHz	62ns*	125ns*	250ns*	500ns	1μs	2μs	4μs	Undefined

A/D Clock Period Examples

Controlling the power on/off function of the A/D converter circuitry is implemented using the ADOFF bit in the ADCR0 register. This bit must be zero to power on the A/D converter. Even if no pins are selected for use as A/D inputs by clearing the ACE15~ACE0 bits in the ACER1~ACER0 registers, if the ADOFF bit is zero then some power will still be consumed. In power conscious applications it is therefore recommended that the ADOFF is set high to reduce power consumption when the A/D converter function is not being used.

The reference voltage supply to the A/D Converter can be supplied from either the positive power supply pin, VDD, or from an external reference sources supplied on pin VREF. The desired selection is made using the VREFS bit. As the VREF pin is pin-shared with other functions, when the VREFS bit is set high, the VREF pin function will be selected and the other pin functions will be disabled automatically.

A/D Input Pins

All of the A/D analog input pins are pin-shared with the I/O pins on PA7, Port B and Port C as well as other functions. The ACE15~ACE0 bits in the ACER1~ACER0 registers, determine whether the input pins are setup as A/D converter analog inputs or whether they have other functions. If the ACE15~ACE0 bits for its corresponding pin is set high then the pin will be setup to be an A/D converter input and the original pin functions disabled. In this way, pins can be changed under program control to change their function between A/D inputs and other functions. All pull-high resistors, which are setup through register programming, will be automatically disconnected if the pins are setup as A/D inputs. Note that it is not necessary to first setup the A/D pin as an input in the PAC, PBC, PCC port control registers to enable the A/D input as when the ACE15~ACE0 bits enable an A/D input, the status of the port control register will be overridden.

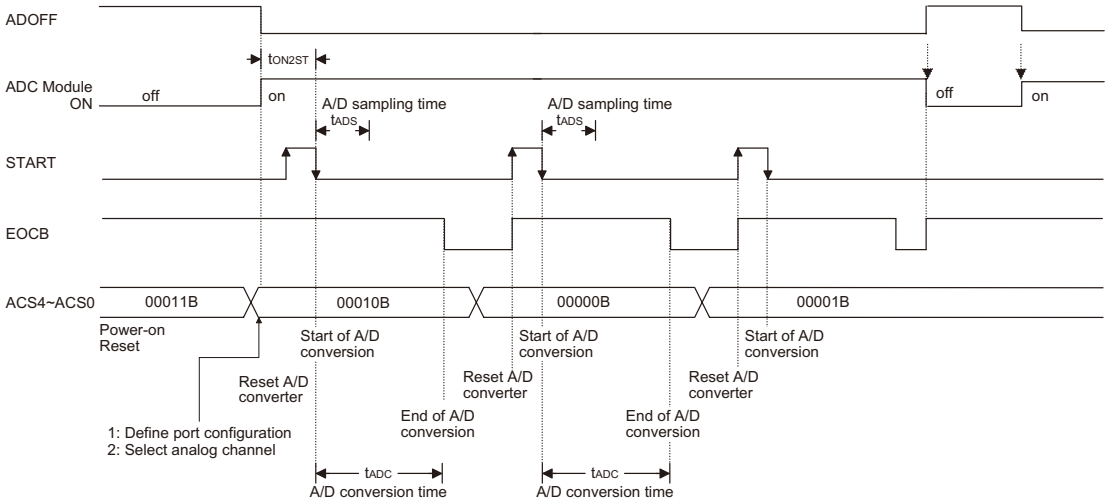
The A/D converter has its own reference voltage pin, VREF, however the reference voltage can also be supplied from the power supply pin, a choice which is made through the VREFS bit in the ADCR1 register. The analog input values must not be allowed to exceed the value of V_{REF}.

Summary of A/D Conversion Steps

The following summarises the individual steps that should be executed in order to implement an A/D conversion process.

- Step 1
  Select the required A/D conversion clock by correctly programming bits ADCK2~ADCK0 in the ADCR1 register.
- Step 2
  Enable the A/D by clearing the ADOFF bit in the ADCR0 register to zero.
- Step 3
  Select which channel is to be connected to the internal A/D converter by correctly programming the ACS4~ACS0 bits which are also contained in the ADCR1 and ADCR0 register.
- Step 4
  Select which pins are to be used as A/D inputs and configure them by correctly programming the ACE15~ACE0 bits in the ACER1~ACER0 registers.
- Step 5
  If the interrupts are to be used, the interrupt control registers must be correctly configured to ensure the A/D converter interrupt function is active. The master interrupt control bit, EMI, and the A/D converter interrupt bit, ADE, must both be set high to do this.
- Step 6
  The analog to digital conversion process can now be initialised by setting the START bit in the ADCR0 register from low to high and then low again. Note that this bit should have been originally cleared to zero.
- Step 7
  To check when the analog to digital conversion process is complete, the EOCB bit in the ADCR0 register can be polled. The conversion process is complete when this bit goes low. When this occurs the A/D data registers ADRL and ADRH can be read to obtain the conversion value. As an alternative method, if the interrupts are enabled and the stack is not full, the program can wait for an A/D interrupt to occur.
  Note: When checking for the end of the conversion process, if the method of polling the EOCB bit in the ADCR0 register is used, the interrupt enable step above can be omitted.

The accompanying diagram shows graphically the various stages involved in an analog to digital conversion process and its associated timing. After an A/D conversion process has been initiated by the application program, the microcontroller internal hardware will begin to carry out the conversion, during which time the program can continue with other functions. The time taken for the A/D conversion is $16t_{AD}$ where t_{AD} is equal to the A/D clock period.



A/D Conversion Timing

Programming Considerations

During microcontroller operations where the A/D converter is not being used, the A/D internal circuitry can be switched off to reduce power consumption, by setting bit ADOFF high in the ADCR0 register. When this happens, the internal A/D converter circuits will not consume power irrespective of what analog voltage is applied to their input lines. If the A/D converter input lines are used as normal I/Os, then care must be taken as if the input voltage is not at a valid logic level, then this may lead to some increase in power consumption.

A/D Transfer Function

As the devices contain a 12-bit A/D converter, its full-scale converted digitised value is equal to FFFH. Since the full-scale analog input value is equal to the V_{DD} or V_{REF} voltage, this gives a single bit analog input value of V_{DD} or V_{REF} divided by 4096.

$$1\ LSB=(V_{DD}\ or\ V_{REF})\div 4096$$

The A/D Converter input voltage value can be calculated using the following equation:

$$A/D\ input\ voltage=A/D\ output\ digital\ value\times(V_{DD}\ or\ V_{REF})\div 4096$$

The diagram shows the ideal transfer function between the analog input value and the digitised output value for the A/D converter. Except for the digitised zero value, the subsequent digitised values will change at a point 0.5 LSB below where they would change without the offset, and the last full scale digitised value will change at a point 1.5 LSB below the V_{DD} or V_{REF} level.

A/D Programming Example

The following two programming examples illustrate how to setup and implement an A/D conversion. In the first example, the method of polling the EOCB bit in the ADCR0 register is used to detect when the conversion cycle is complete, whereas in the second example, the A/D interrupt is used to determine when the conversion is complete.

Example: using an EOCB polling method to detect the end of conversion

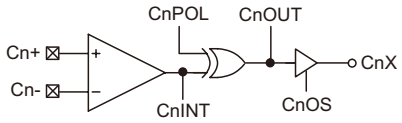
```
clr  ADE                    ; disable ADC interrupt
mov  a,03H
mov  ADCR1,a                ; select fSYS/8 as A/D clock and switch off 1.25V
clr  ADOFF
clr  ACER1
mov  a,0Fh                  ; setup ACER to configure pins AN0~AN3
mov  ACER0,a
mov  a,00h
mov  ADCR0,a                ; enable and connect AN0 channel to A/D converter
:
start_conversion:
     clr START              ; high pulse on start bit to initiate conversion
     set START              ; reset A/D
     clr START              ; start A/D
polling_EOC:
     sz  EOCB               ; poll the ADCR0 register EOCB bit to detect end
                            ; of A/D conversion
     jmp polling_EOC        ; continue polling
     mov a,ADRL             ; read low byte conversion result value
     mov ADRL_buffer,a      ; save result to user defined register
     mov a,ADRH             ; read high byte conversion result value
     mov ADRH_buffer,a      ; save result to user defined register
:
:
jmp  start_conversion       ; start next a/d conversion
```

Example: using the interrupt method to detect the end of conversion

```
clr  ADE                    ; disable ADC interrupt
mov  a,03H
mov  ADCR1,a                ; select fSYS/8 as A/D clock and switch off 1.25V
Clr  ADOFF
clr  ACER1
mov  a,0Fh                  ; setup ACER to configure pins AN0~AN3
mov  ACER0,a
mov  a,00h
mov  ADCR0,a                ; enable and connect AN0 channel to A/D converter
Start_conversion:
     clr START              ; high pulse on START bit to initiate conversion
     set START              ; reset A/D
     clr START              ; start A/D
     clr ADF                ; clear ADC interrupt request flag
     set ADE                ; enable ADC interrupt
     set EMI                ; enable global interrupt
:
:
                            ; ADC interrupt service routine
ADC_ISR:
     mov acc_stack,a        ; save ACC to user defined memory
     mov a,STATUS
     mov status_stack,a     ; save STATUS to user defined memory
:
:
     mov a,ADRL             ; read low byte conversion result value
     mov adrl_buffer,a      ; save result to user defined register
     mov a,ADRH             ; read high byte conversion result value
     mov adrh_buffer,a      ; save result to user defined register
:
:
EXIT_INT_ISR:
     mov a,status_stack
     mov STATUS,a           ; restore STATUS from user defined memory
     mov a,acc_stack        ; restore ACC from user defined memory
     reti
```

Comparators

Two independent analog comparators are contained within these devices. These functions offer flexibility via their register controlled features such as power-down, polarity select, hysteresis etc. In sharing their pins with normal I/O pins the comparators do not waste precious I/O pins if there functions are otherwise unused.



Comparator

Comparator Operation

The devices contain two comparator functions which are used to compare two analog voltages and provide an output based on their difference. Full control over the two internal comparators is provided via two control registers, CP0C and CP1C, one assigned to each comparator. The comparator output is recorded via a bit in their respective control register, but can also be transferred out onto a shared I/O pin. Additional comparator functions include, output polarity, hysteresis functions and power down control.

Any pull-high resistors connected to the shared comparator input pins will be automatically disconnected when the comparator is enabled. As the comparator inputs approach their switching level, some spurious output signals may be generated on the comparator output due to the slow rising or falling nature of the input signals. This can be minimised by selecting the hysteresis function will apply a small amount of positive feedback to the comparator. Ideally the comparator should switch at the point where the positive and negative inputs signals are at the same voltage level, however, unavoidable input offsets introduce some uncertainties here. The hysteresis function, if enabled, also increases the switching offset value.

Comparator Registers

There are two registers for overall comparator operation, one for each comparator. As corresponding bits in the two registers have identical functions, they following register table applies to both registers.

Register Name	Bit							
	7	6	5	4	3	2	1	0
CP0C	C0SEL	C0EN	C0POL	C0OUT	C0OS	—	—	C0HYEN
CP1C	C1SEL	C1EN	C1POL	C1OUT	C1OS	—	—	C1HYEN

Comparator Registers List

Comparator Interrupt

Each also possesses its own interrupt function. When any one of the changes state, its relevant interrupt flag will be set, and if the corresponding interrupt enable bit is set, then a jump to its relevant interrupt vector will be executed. Note that it is the changing state on C0INT or C1INT which generate an interrupt. If the microcontroller is in the SLEEP or IDLE Mode and the Comparator is enabled, then if the external input lines cause the Comparator output to change state, the resulting generated interrupt flag will also generate a wake-up. If it is required to disable a wake-up from occurring, then the interrupt flag should be first set high before entering the SLEEP or IDLE Mode.

Programming Considerations

If the comparator is enabled, it will remain active when the microcontroller enters the SLEEP or IDLE Mode, however as it will consume a certain amount of power, the user may wish to consider disabling it before the SLEEP or IDLE Mode is entered.

As comparator pins are shared with normal I/O pins the I/O registers for these pins will be read as zero (port control register is "1") or read as port data register value (port control register is "0") if the comparator function is enabled.

CP0C Register

Bit	7	6	5	4	3	2	1	0
Name	C0SEL	C0EN	C0POL	C0OUT	C0OS	—	—	C0HYEN
R/W	R/W	R/W	R/W	R	R/W	—	—	R/W
POR	1	0	0	0	0	—	—	1

Bit 7 **C0SEL:** Select Comparator pins or I/O pins
0: I/O pin select
1: Comparator pin select
This is the Comparator pin or I/O pin select bit. If the bit is high the comparator will be selected and the two comparator input pins will be enabled. As a result, these two pins will lose their I/O pin functions. Any pull-high configuration options associated with the comparator shared pins will also be automatically disconnected.

Bit 6 **C0EN:** Comparator On/Off control
0: Off
1: On
This is the Comparator on/off control bit. If the bit is zero the comparator will be switched off and no power consumed even if analog voltages are applied to its inputs. For power sensitive applications this bit should be cleared to zero if the comparator is not used or before the devices enter the SLEEP or IDLE mode.

Bit 5 **C0POL:** Comparator output polarity
0: output not inverted
1: output inverted
This is the comparator polarity bit. If the bit is zero then the C0OUT bit will reflect the non-inverted output condition of the comparator. If the bit is high the comparator C0OUT bit will be inverted.

Bit 4 **C0OUT:** Comparator output bit
C0POL=0
0: C0+ < C0-
1: C0+ > C0-
C0POL=1
0: C0+ > C0-
1: C0+ < C0-
This bit stores the comparator output bit. The polarity of the bit is determined by the voltages on the comparator inputs and by the condition of the C0POL bit.

Bit 3 **C0OS:** Output path select
0: C0X pin
1: Internal use
This is the comparator output path select control bit. If the bit is set to "0" and the C0SEL bit is "1" the comparator output is connected to an external C0X pin. If the bit is set to "1" or the C0SEL bit is "0" the comparator output signal is only used internally by the devices allowing the shared comparator output pin to retain its normal I/O operation.

Bit 2~1 Unimplemented, read as "0"

Bit 0 **C0HYEN:** Hysteresis Control
0: Off
1: On
This is the hysteresis control bit and if set high will apply a limited amount of hysteresis to the comparator, as specified in the Comparator Electrical Characteristics table. The positive feedback induced by hysteresis reduces the effect of spurious switching near the comparator threshold.

• **CP1C Register**

Bit	7	6	5	4	3	2	1	0
Name	C1SEL	C1EN	C1POL	C1OUT	C1OS	—	—	C1HYEN
R/W	R/W	R/W	R/W	R	R/W	—	—	R/W
POR	1	0	0	0	0	—	—	1

Bit 7 **C1SEL:** Select Comparator pins or I/O pins
0: I/O pin select
1: Comparator pin select
This is the Comparator pin or I/O pin select bit. If the bit is high the comparator will be selected and the two comparator input pins will be enabled. As a result, these two pins will lose their I/O pin functions. Any pull-high configuration options associated with the comparator shared pins will also be automatically disconnected.

Bit 6 **C1EN:** Comparator On/Off control
0: Off
1: On
This is the Comparator on/off control bit. If the bit is zero the comparator will be switched off and no power consumed even if analog voltages are applied to its inputs. For power sensitive applications this bit should be cleared to zero if the comparator is not used or before the devices enter the SLEEP or IDLE mode.

Bit 5 **C1POL:** Comparator output polarity
0: output not inverted
1: output inverted
This is the comparator polarity bit. If the bit is zero then the C1OUT bit will reflect the non-inverted output condition of the comparator. If the bit is high the comparator C1OUT bit will be inverted.

Bit 4 **C1OUT:** Comparator output bit
C1POL=0
0: C1+ < C1-
1: C1+ > C1-
C1POL=1
0: C1+ > C1-
1: C1+ < C1-
This bit stores the comparator output bit. The polarity of the bit is determined by the voltages on the comparator inputs and by the condition of the C1POL bit.

Bit 3 **C1OS:** Output path select
0: C1X pin
1: Internal use
This is the comparator output path select control bit. If the bit is set to "0" and the C1SEL bit is "1" the comparator output is connected to an external C1X pin. If the bit is set to "1" or the C1SEL bit is "0" the comparator output signal is only used internally by the devices allowing the shared comparator output pin to retain its normal I/O operation.

Bit 2~1 Unimplemented, read as "0"

Bit 0 **C1HYEN:** Hysteresis Control
0: Off
1: On
This is the hysteresis control bit and if set high will apply a limited amount of hysteresis to the comparator, as specified in the Comparator Electrical Characteristics table. The positive feedback induced by hysteresis reduces the effect of spurious switching near the comparator threshold.

Serial Interface Module – SIM

The devices contain a Serial Interface Module, which includes both the four line SPI interface and the two line I²C interface types, to allow an easy method of communication with external peripheral hardware. Having relatively simple communication protocols, these serial interface types allow the microcontroller to interface to external SPI or I²C based hardware such as sensors, Flash or EEPROM memory, etc. The SIM interface pins are pin-shared with other I/O pins therefore the SIM interface function must first be selected by software control. As both interface types share the same pins and registers, the choice of whether the SPI or I²C type is used is made using the SIM operating mode control bits, named SIM2~SIM0, in the SIMC0 register. These pull-high resistors of the SIM pin-shared I/O are selected using pull-high control registers, and also if the SIM function is enabled.

There is one control register associated with the serial interface control, namely SBSC. This is used to enable the SIM WCOL bit function, SPIA WCOL bit function and I²C debounce selection.

The devices provide two kinds of SPI function, namely SPI and SPIA, each of them has the corresponding WCOL control bits to enable the SIM WCOL and SPIA WCOL control bits, namely SIM_WCOL and SA_WCOL respectively. In addition, the I2CDB1 and I2CDB0 bits are used to select the I²C debounce time.

SPI Interface

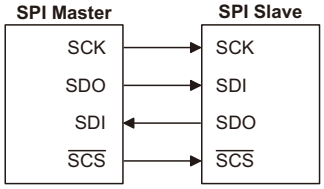
This SPI interface function, which is part of the Serial Interface Module, should not be confused with the other independent SPI function, known as SPIA, which is described in another section of this datasheet.

The SPI interface is often used to communicate with external peripheral devices such as sensors, Flash or EEPROM memory devices etc. Originally developed by Motorola, the four line SPI interface is a synchronous serial data interface that has a relatively simple communication protocol simplifying the programming requirements when communicating with external hardware devices.

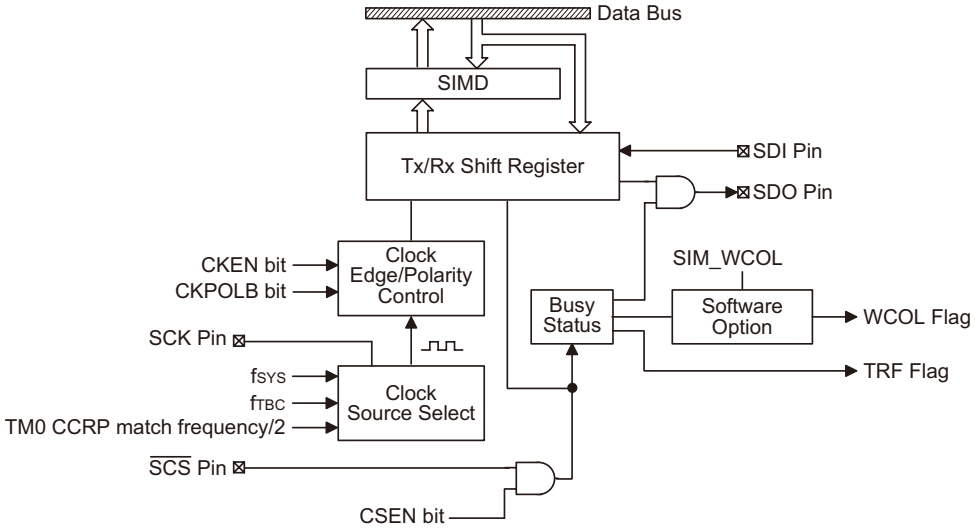
The communication is full duplex and operates as a slave/master type, where the devices can be either master or slave. Although the SPI interface specification can control multiple slave devices from a single master, but these devices provided only one $\overline{SCS}$ pin. If the master needs to control multiple slave devices from a single master, the master can use I/O pin to select the slave devices.

SPI Interface Operation

The SPI interface is a full duplex synchronous serial data link. It is a four line interface with pin names SDI, SDO, SCK and $\overline{SCS}$. Pins SDI and SDO are the Serial Data Input and Serial Data Output lines, SCK is the Serial Clock line and $\overline{SCS}$ is the Slave Select line. As the SPI interface pins are pin-shared with other functions and with the I²C function pins, the SPI interface must first be selected by the correct bits in the SIMC0 and SIMC2 registers. After the SPI option has been selected, it can also be additionally disabled or enabled using the SIMEN bit in the SIMC0 register.



SPI Master/Slave Connection



SPI Bolck Diagram

The SPI function in these devices offers the following features:

- Full duplex synchronous data transfer
- Both Master and Slave modes
- LSB first or MSB first data transmission modes
- Transmission complete flag
- Rising or falling active clock edge
- WCOL bit enabled or disable select

The status of the SPI interface pins is determined by a number of factors such as whether the devices are in the master or slave mode and upon the condition of certain control bits such as CSEN and SIMEN.

SPI Registers

There are four internal registers which control the overall operation of the SPI interface. These are the SIMD data register and three registers SIMC0, SIMC2 and SBSC. Note that the SIMC1 register is only used by the I²C interface.

Register Name	Bit							
	7	6	5	4	3	2	1	0
SIMC0	SIM2	SIM1	SIM0	PCKEN	PCKP1	PCKP0	SIMEN	—
SIMD	D7	D6	D5	D4	D3	D2	D1	D0
SIMC2	D7	D6	CKPOLB	CKEG	MLS	CSEN	WCOL	TRF
SBSC	SIM_WCOL	—	I2CDB1	I2CDB0	—	—	—	SA_WCOL

SIM Registers List

The SIMD register is used to store the data being transmitted and received. The same register is used by both the SPI and I²C functions. Before the devices write data to the SPI bus, the actual data to be transmitted must be placed in the SIMD register. After the data is received from the SPI bus, the devices can read it from the SIMD register. Any transmission or reception of data from the SPI bus must be made via the SIMD register.

SIMD Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x" unknown

There are also three control registers for the SPI interface, SIMC0 and SIMC2 and SBSC. Note that the SIMC2 register also has the name SIMA which is used by the I²C function. The SIMC1 register is not used by the SPI function, only by the I²C function. Register SIMC0 is used to control the enable/disable function and to set the data transmission clock frequency. Although not connected with the SPI function, the SIMC0 register is also used to control the Peripheral Clock Prescaler. Register SIMC2 is used for other control functions such as LSB/MSB selection, write collision flag etc. The SIM_WCOL bit in the SBSC register is used to control the SPI WCOL function.

SIMC0 Register

Bit	7	6	5	4	3	2	1	0
Name	SIM2	SIM1	SIM0	PCKEN	PCKP1	PCKP0	SIMEN	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—
POR	1	1	1	0	0	0	0	—

Bit 7~5 **SIM2, SIM1, SIM0:** SIM Operating Mode Control
000: SPI master mode; SPI clock is $f_{SYS}/4$
001: SPI master mode; SPI clock is $f_{SYS}/16$
010: SPI master mode; SPI clock is $f_{SYS}/64$
011: SPI master mode; SPI clock is f_{TBC}
100: SPI master mode; SPI clock is TM0 CCRP match frequency/2
101: SPI slave mode
110: I^2C slave mode
111: Non SIM function

These bits setup the overall operating mode of the SIM function. As well as selecting if the I^2C or SPI function, they are used to control the SPI Master/Slave selection and the SPI Master clock frequency. The SPI clock is a function of the system clock but can also be chosen to be sourced from TM0. If the SPI Slave Mode is selected then the clock will be supplied by an external Master devices.

Bit 4 **PCKEN:** PCK Output Pin Control
0: Disable
1: Enable

Bit 3~2 **PCKP1, PCKP0:** Select PCK output pin frequency
00: f_{SYS}
01: $f_{SYS}/4$
10: $f_{SYS}/8$
11: TM0 CCRP match frequency/2

Bit 1 **SIMEN:** SIM Control
0: Disable
1: Enable

The bit is the overall on/off control for the SIM interface. When the SIMEN bit is cleared to zero to disable the SIM interface, the SDI, SDO, SCK and $\overline{SCS}$, or SDA and SCL lines will lose their SPI or I^2C function and the SIM operating current will be reduced to a minimum value. When the bit is high the SIM interface is enabled. If the SIM is configured to operate as an SPI interface via the SIM2~SIM0 bits, the contents of the SPI control registers will remain at the previous settings when the SIMEN bit changes from low to high and should therefore be first initialised by the application program. If the SIM is configured to operate as an I^2C interface via the SIM2~SIM0 bits and the SIMEN bit changes from low to high, the contents of the I^2C control bits such as HTX and TXAK will remain at the previous settings and should therefore be first initialised by the application program while the relevant I^2C flags such as HCF, HAAS, HBB, SRW and RXAK will be set to their default states.

Bit 0 Unimplemented

SIMC2 Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	CKPOLB	CKEG	MLS	CSEN	WCOL	TRF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 Undefined bit
This bit can be read or written by the application program.

Bit 5 **CKPOLB:** Determines the base condition of the clock line
0: the SCK line will be high when the clock is inactive
1: the SCK line will be low when the clock is inactive
The CKPOLB bit determines the base condition of the clock line, if the bit is high, then the SCK line will be low when the clock is inactive. When the CKPOLB bit is low, then the SCK line will be high when the clock is inactive.

Bit 4 **CKEG:** Determines SPI SCK active clock edge type
CKPOLB=0
0: SCK is high base level and data capture at SCK rising edge
1: SCK is high base level and data capture at SCK falling edge
CKPOLB=1
0: SCK is low base level and data capture at SCK falling edge
1: SCK is low base level and data capture at SCK rising edge
The CKEG and CKPOLB bits are used to setup the way that the clock signal outputs and inputs data on the SPI bus. These two bits must be configured before data transfer is executed otherwise an erroneous clock edge may be generated. The CKPOLB bit determines the base condition of the clock line, if the bit is high, then the SCK line will be low when the clock is inactive. When the CKPOLB bit is low, then the SCK line will be high when the clock is inactive. The CKEG bit determines active clock edge type which depends upon the condition of CKPOLB bit.

Bit 3 **MLS:** SPI Data shift order
0: LSB
1: MSB
This is the data shift select bit and is used to select how the data is transferred, either MSB or LSB first. Setting the bit high will select MSB first and low for LSB first.

Bit 2 **CSEN:** SPI $\overline{SCS}$ pin Control
0: Disable
1: Enable
The CSEN bit is used as an enable/disable for the $\overline{SCS}$ pin. If this bit is low, then the $\overline{SCS}$ pin will be disabled and placed into I/O pin or the other functions. If the bit is high the $\overline{SCS}$ pin will be enabled and used as a select pin.

Bit 1 **WCOL:** SPI Write Collision flag
0: No collision
1: Collision
The WCOL flag is used to detect if a data collision has occurred. If this bit is high it means that data has been attempted to be written to the SIMD register during a data transfer operation. This writing operation will be ignored if data is being transferred. The bit can be cleared by the application program. Note that using the WCOL bit can be disabled or enabled via the SIM_WCOL bit in the SBSC register.

Bit 0 **TRF:** SPI Transmit/Receive Complete flag
0: Data is being transferred
1: SPI data transmission is completed
The TRF bit is the Transmit/Receive Complete flag and is set “1” automatically when an SPI data transmission is completed, but must set to “0” by the application program. It can be used to generate an interrupt.

SBSC Register

Bit	7	6	5	4	3	2	1	0
Name	SIM_WCOL	—	I2CDB1	I2CDB0	—	—	—	SA_WCOL
R/W	R/W	R	R/W	R/W	R	R	R	R/W
POR	0	0	0	0	0	0	0	0

Bit 7: **SIM_WCOL:** SIM WCOL control bit
0: Disable
1: Enable

Bit 6: Unimplemented

Bit 5,4: **I2CDB1, I2CDB0 :** I^2C debounce selection bits
related to I^2C function, described elsewhere

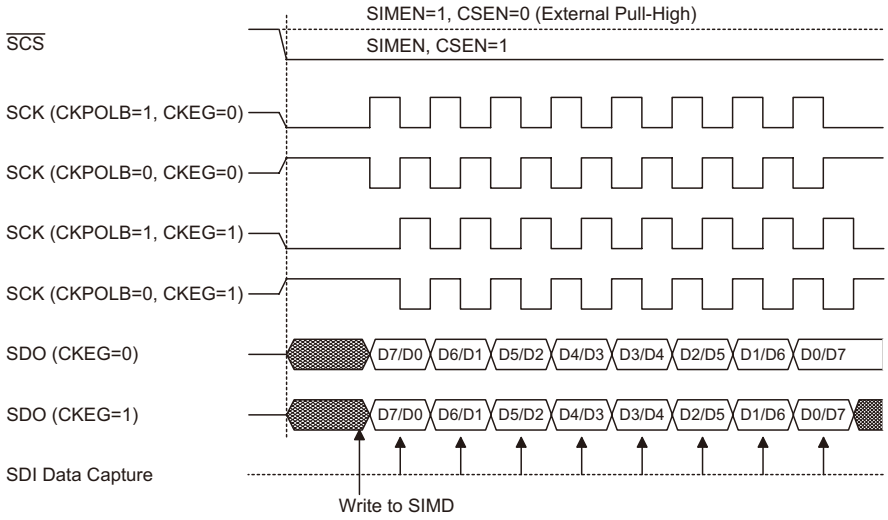
Bit 3~1: Unimplemented

Bit 0: **SA_WCOL** : SPIA WCOL function control
0: Disable
1: Enable
related to SPIA function, described elsewhere

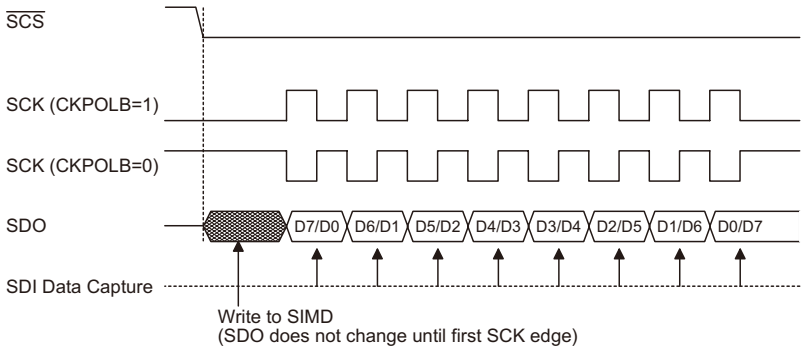
SPI Communication

After the SPI interface is enabled by setting the SIMEN bit high, then in the Master Mode, when data is written to the SIMD register, transmission/reception will begin simultaneously. When the data transfer is complete, the TRF flag will be set automatically, but must be cleared using the application program. In the Slave Mode, when the clock signal from the master has been received, any data in the SIMD register will be transmitted and any data on the SDI pin will be shifted into the SIMD register. The master should output an $\overline{SCS}$ signal to enable the slave devices before a clock signal is provided. The slave data to be transferred should be well prepared at the appropriate moment relative to the $\overline{SCS}$ signal depending upon the configurations of the CKPOLB bit and CKEG bit. The accompanying timing diagram shows the relationship between the slave data and $\overline{SCS}$ signal for various configurations of the CKPOLB and CKEG bits.

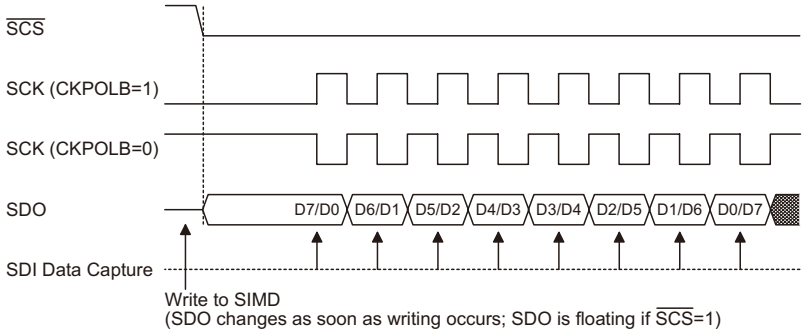
The SPI will continue to function even in the IDLE Mode.



SPI Master Mode Timing

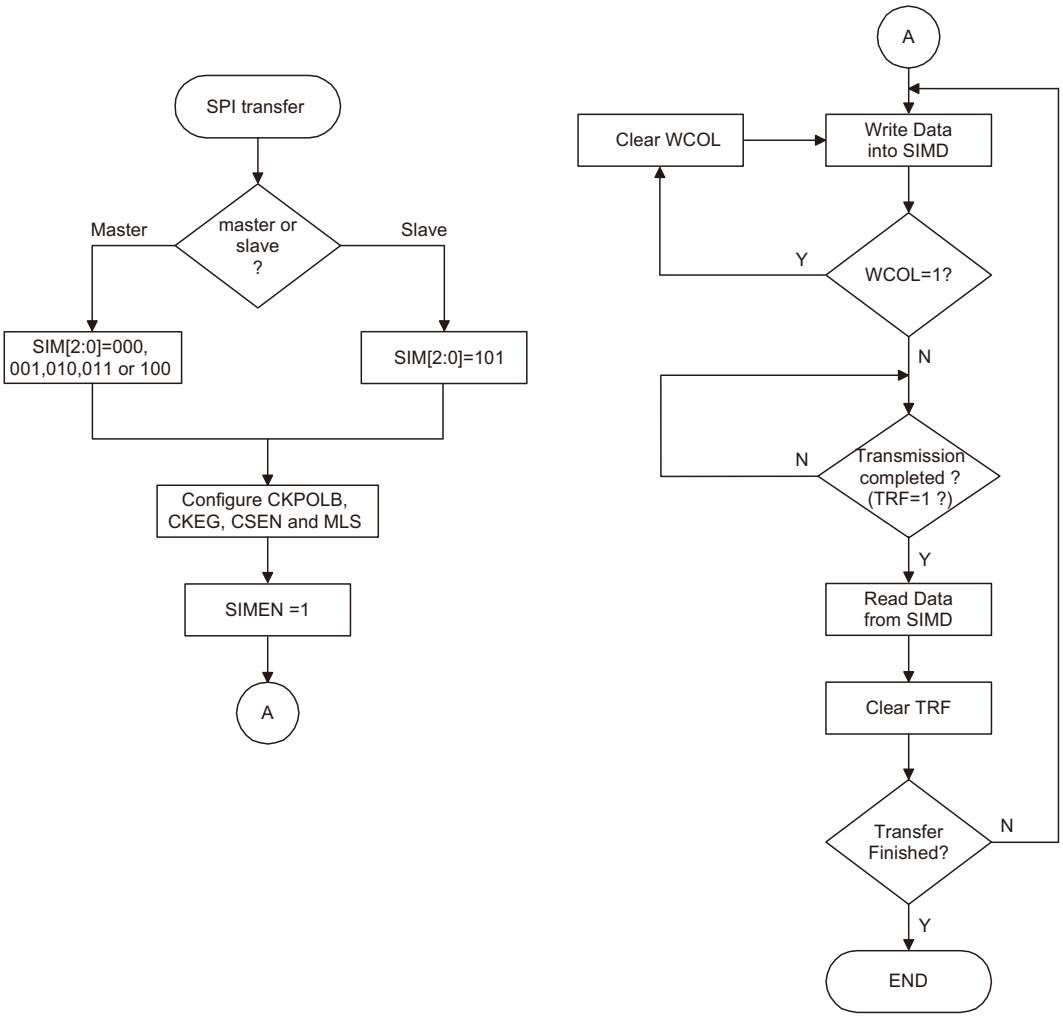


SPI Slave Mode Timing – CKEG=0



Note: For SPI slave mode, if SIMEN=1 and CSEN=0, SPI is always enabled and ignores the $\overline{SCS}$ level.

SPI Slave Mode Timing – CKEG=1



SPI Transfer Control Flowchart

SPI Bus Enable/Disable

To enable the SPI bus, set CSEN=1 and $\overline{SCS}$=0, then wait for data to be written into the SIMD (TXRX buffer) register. For the Master Mode, after data has been written to the SIMD (TXRX buffer) register, then transmission or reception will start automatically. When all the data has been transferred, the TRF bit should be set. For the Slave Mode, when clock pulses are received on SCK, data in the TXRX buffer will be shifted out or data on SDI will be shifted in.

To disable the SPI bus, the SCK, SDI, SDO and $\overline{SCS}$ will become I/O pins or the other functions.

SPI Operation

All communication is carried out using the 4-line interface for either Master or Slave Mode.

The CSEN bit in the SIMC2 register controls the overall function of the SPI interface. Setting this bit high will enable the SPI interface by allowing the $\overline{SCS}$ line to be active, which can then be used to control the SPI interface. If the CSEN bit is low, the SPI interface will be disabled and the $\overline{SCS}$ line will be an I/O pin or the other functions and can therefore not be used for control of the SPI interface. If the CSEN bit and the SIMEN bit in the SIMC0 are set high, this will place the SDI line in a floating condition and the SDO line high. If in Master Mode the SCK line will be either high or low depending upon the clock polarity selection bit CKPOLB in the SIMC2 register. If in Slave Mode the SCK line will be in a floating condition. If the SIMEN bit is low, then the bus will be disabled and $\overline{SCS}$, SDI, SDO and SCK will all become I/O pins or the other functions. In the Master Mode the Master will always generate the clock signal. The clock and data transmission will be initiated after data has been written into the SIMD register. In the Slave Mode, the clock signal will be received from an external master devices for both data transmission and reception. The following sequences show the order to be followed for data transfer in both Master and Slave Mode:

Master Mode:

- Step 1
  Select the SPI Master mode and clock source using the SIM2~SIM0 bits in the SIMC0 control register
- Step 2
  Setup the CSEN bit and setup the MLS bit to choose if the data is MSB or LSB first, this setting must be the same with the Slave devices.
- Step 3
  Setup the SIMEN bit in the SIMC0 control register to enable the SPI interface.
- Step 4
  For write operations: write the data to the SIMD register, which will actually place the data into the TXRX buffer. Then use the SCK and $\overline{SCS}$ lines to output the data. After this, go to step5.
  For read operations: the data transferred in on the SDI line will be stored in the TXRX buffer until all the data has been received at which point it will be latched into the SIMD register.
- Step 5
  Check the WCOL bit if set high then a collision error has occurred so return to step 4. If equal to zero then go to the following step.
- Step 6
  Check the TRF bit or wait for a SPI serial bus interrupt.
- Step 7
  Read data from the SIMD register.
- Step 8
  Clear TRF.
- Step 9
  Go to step 4.

Slave Mode:

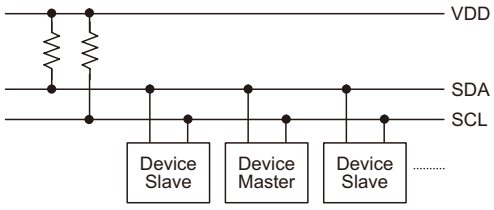
- Step 1
  Select the SPI Slave mode using the SIM2~SIM0 bits in the SIMC0 control register
- Step 2
  Setup the CSEN bit and setup the MLS bit to choose if the data is MSB or LSB first, this setting must be the same with the Master devices.
- Step 3
  Setup the SIMEN bit in the SIMC0 control register to enable the SPI interface.
- Step 4
  For write operations: write the data to the SIMD register, which will actually place the data into the TXRX buffer. Then wait for the master clock SCK and $\overline{SCS}$ signal. After this, go to step5.
  For read operations: the data transferred in on the SDI line will be stored in the TXRX buffer until all the data has been received at which point it will be latched into the SIMD register.
- Step 5
  Check the WCOL bit if set high then a collision error has occurred so return to step 4. If equal to zero then go to the following step.
- Step 6
  Check the TRF bit or wait for a SPI serial bus interrupt.
- Step 7
  Read data from the SIMD register.
- Step 8
  Clear TRF.
- Step 9
  Go to step 4.

Error Detection

The WCOL bit in the SIMC2 register is provided to indicate errors during data transfer. The bit is set by the SPI serial Interface but must be cleared by the application program. This bit indicates a data collision has occurred which happens if a write to the SIMD register takes place during a data transfer operation and will prevent the write operation from continuing. The overall function of the WCOL bit can be disabled or enabled by the SIM_WCOL bit in the SBSC register. .

I²C Interface

The I²C interface is used to communicate with external peripheral devices such as sensors, EEPROM memory etc. Originally developed by Philips, it is a two line low speed serial interface for synchronous serial data transfer. The advantage of only two lines for communication, relatively simple communication protocol and the ability to accommodate multiple devices on the same bus has made it an extremely popular interface type for many applications.



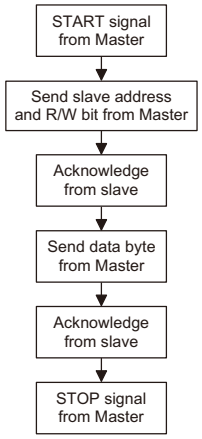
I²C Master Slave Bus Connection

I²C Interface Operation

The I²C serial interface is a two line interface, a serial data line, SDA, and serial clock line, SCL. As many devices may be connected together on the same bus, their outputs are both open drain types. For this reason it is necessary that external pull-high resistors are connected to these outputs. Note that no chip select line exists, as each device on the I²C bus is identified by a unique address which will be transmitted and received on the I²C bus.

When two devices communicate with each other on the bidirectional I²C bus, one is known as the master device and one as the slave device. Both master and slave can transmit and receive data, however, it is the master device that has overall control of the bus. For these devices, which only operate in slave mode, there are two methods of transferring data on the I²C bus, the slave transmit mode and the slave receive mode.

The debounce time of the I²C interface can be determined by the I2CDB1 and I2CDB0 bits in the SBSC register. This uses the internal clock to in effect add a debounce time to the external clock to reduce the possibility of glitches on the clock line causing erroneous operation. The debounce time, if selected, can be chosen to be either 1 or 2 system clocks.



I²C Registers

There are three control registers associated with the I²C bus, SIMC0, SIMC1 and SBSC, one address register SIMA and one data register, SIMD. The SIMD register, which is shown in the above SPI section, is used to store the data being transmitted and received on the I²C bus. Before the microcontroller writes data to the I²C bus, the actual data to be transmitted must be placed in the SIMD register. After the data is received from the I²C bus, the microcontroller can read it from the SIMD register. Any transmission or reception of data from the I²C bus must be made via the SIMD register.

Note that the SIMA register also has the name SIMC2 which is used by the SPI function. Bit SIMEN and bits SIM2~SIM0 in register SIMC0 are used by the I²C interface. The I2CDB0 and I2CDB1 in the SBSC register are used to select the I²C debounce time.

Register Name	Bit							
	7	6	5	4	3	2	1	0
SIMC0	SIM2	SIM1	SIM0	PCKEN	PCKP1	PCKP0	SIMEN	—
SIMC1	HCF	HANS	HBB	HTX	TXAK	SRW	IAMWU	RXAK
SIMD	D7	D6	D5	D4	D3	D2	D1	D0
SIMA	IICA6	IICA5	IICA4	IICA3	IICA2	IICA1	IICA0	D0
SBSC	SIM_WCOL	—	I2CDB1	I2CDB0	—	—	—	SA_WCOL

I²C Registers List

SIMC0 Register

Bit	7	6	5	4	3	2	1	0
Name	SIM2	SIM1	SIM0	PCKEN	PCKP1	PCKP0	SIMEN	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—
POR	1	1	1	0	0	0	0	—

Bit 7~5 **SIM2, SIM1, SIM0:** SIM Operating Mode Control
000: SPI master mode; SPI clock is $f_{SYS}/4$
001: SPI master mode; SPI clock is $f_{SYS}/16$
010: SPI master mode; SPI clock is $f_{SYS}/64$
011: SPI master mode; SPI clock is f_{TBC}
100: SPI master mode; SPI clock is TM0 CCRP match frequency/2
101: SPI slave mode
110: I^2C slave mode
111: Non SIM function

These bits setup the overall operating mode of the SIM function. As well as selecting if the I^2C or SPI function, they are used to control the SPI Master/Slave selection and the SPI Master clock frequency. The SPI clock is a function of the system clock but can also be chosen to be sourced from the TM0. If the SPI Slave Mode is selected then the clock will be supplied by an external Master device.

Bit 4 **PCKEN:** PCK Output Pin Control
0: Disable
1: Enable

Bit 3~2 **PCKP1, PCKP0:** Select PCK output pin frequency
00: f_{SYS}
01: $f_{SYS}/4$
10: $f_{SYS}/8$
11: TM0 CCRP match frequency/2

Bit 1 **SIMEN:** SIM Control
0: Disable
1: Enable

The bit is the overall on/off control for the SIM interface. When the SIMEN bit is cleared to zero to disable the SIM interface, the SDI, SDO, SCK and $\overline{SCS}$, or SDA and SCL lines will be in a floating condition and the SIM operating current will be reduced to a minimum value. When the bit is high the SIM interface is enabled. If the SIM is configured to operate as an SPI interface via SIM2~SIM0 bits, the contents of the SPI control registers will remain at the previous settings when the SIMEN bit changes from low to high and should therefore be first initialised by the application program. If the SIM is configured to operate as an I^2C interface via the SIM2~SIM0 bits and the SIMEN bit changes from low to high, the contents of the I^2C control bits such as HTX and TXAK will remain at the previous settings and should therefore be first initialised by the application program while the relevant I^2C flags such as HCF, HAAS, HBB, SRW and RXAK will be set to their default states.

Bit 0 Unimplemented

SIMC1 Register

Bit	7	6	5	4	3	2	1	0
Name	HCF	HAAS	HBB	HTX	TXAK	SRW	IAMWU	RXAK
R/W	R	R	R	R/W	R/W	R	R/W	R
POR	1	0	0	0	0	0	0	1

Bit 7 **HCF:** I²C Bus data transfer completion flag
0: Data is being transferred
1: Completion of an 8-bit data transfer
The HCF flag is the data transfer flag. This flag will be zero when data is being transferred. Upon completion of an 8-bit data transfer the flag will go high and an interrupt will be generated.

Bit 6 **HAAS:** I²C Bus address match flag
0: Not address match
1: Address match
The HASS flag is the address match flag. This flag is used to determine if the slave device address is the same as the master transmit address. If the addresses match then this bit will be high, if there is no match then the flag will be low.

Bit 5 **HBB:** I²C Bus busy flag
0: I²C Bus is not busy
1: I²C Bus is busy
The HBB flag is the I²C busy flag. This flag will be "1" when the I²C bus is busy which will occur when a START signal is detected. The flag will be set to "0" when the bus is free which will occur when a STOP signal is detected.

Bit 4 **HTX:** Select I²C slave device is transmitter or receiver
0: Slave device is the receiver
1: Slave device is the transmitter

Bit 3 **TXAK:** I²C Bus transmit acknowledge flag
0: Slave send acknowledge flag
1: Slave do not send acknowledge flag
The TXAK bit is the transmit acknowledge flag. After the slave device receipt of 8-bits of data, this bit will be transmitted to the bus on the 9th clock from the slave device. The slave device must always set TXAK bit to "0" before further data is received.

Bit 2 **SRW:** I²C Slave Read/Write flag
0: Slave device should be in receive mode
1: Slave device should be in transmit mode
The SRW flag is the I²C Slave Read/Write flag. This flag determines whether the master device wishes to transmit or receive data from the I²C bus. When the transmitted address and slave address is match, that is when the HAAS flag is set high, the slave device will check the SRW flag to determine whether it should be in transmit mode or receive mode. If the SRW flag is high, the master is requesting to read data from the bus, so the slave device should be in transmit mode. When the SRW flag is zero, the master will write data to the bus, therefore the slave device should be in receive mode to read this data.

Bit 1 **IAMWU:** I²C Address Match Wake-up Control
0: Disable
1: Enable
This bit should be set to "1" to enable I²C address match wake up from SLEEP or IDLE Mode.

Bit 0 **RXAK:** I²C Bus Receive acknowledge flag
0: Slave receive acknowledge flag
1: Slave does not receive acknowledge flag

The RXAK flag is the receiver acknowledge flag. When the RXAK flag is "0", it means that a acknowledge signal has been received at the 9th clock, after 8 bits of data have been transmitted. When the slave device in the transmit mode, the slave device checks the RXAK flag to determine if the master receiver wishes to receive the next byte. The slave transmitter will therefore continue sending out data until the RXAK flag is "1". When this occurs, the slave transmitter will release the SDA line to allow the master to send a STOP signal to release the I²C Bus.

The SIMD register is used to store the data being transmitted and received. The same register is used by both the SPI and I²C functions. Before the devices write data to the SPI bus, the actual data to be transmitted must be placed in the SIMD register. After the data is received from the SPI bus, the devices can read it from the SIMD register. Any transmission or reception of data from the SPI bus must be made via the SIMD register.

SIMD Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	X	x	x	x	x	x	x

"x" unknown

SIMA Register

Bit	7	6	5	4	3	2	1	0
Name	IICA6	IICA5	IICA4	IICA3	IICA2	IICA1	IICA0	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—
POR	x	X	x	x	x	x	x	—

"x" unknown

Bit 7~1 **IICA6~IICA0:** I²C slave address
IICA6~IICA0 is the I²C slave address bit 6~bit 0.

The SIMA register is also used by the SPI interface but has the name SIMC2. The SIMA register is the location where the 7-bit slave address of the slave device is stored. Bits 7~1 of the SIMA register define the device slave address. Bit 0 is not defined.

When a master device, which is connected to the I²C bus, sends out an address, which matches the slave address in the SIMA register, the slave device will be selected. Note that the SIMA register is the same register address as SIMC2 which is used by the SPI interface.

Bit 0 Undefined bit
This bit can be read or written by user software program.

SBSC Register

Bit	7	6	5	4	3	2	1	0
Name	SIM_WCOL	—	I2CDB1	I2CDB0	—	—	—	SA_WCOL
R/W	R/W	R	R/W	R/W	R	R	R	R/W
POR	0	0	0	0	0	0	0	0

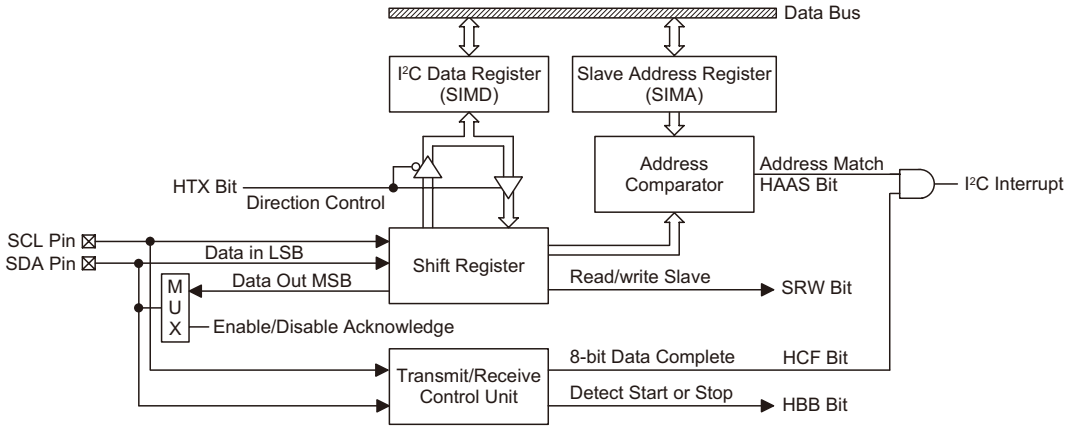
Bit 7 **SIM_WCOL** : SIM WCOL control bit
Related to SPI, described elsewhere.

Bit 6 Unimplemented

Bit 5, 4 **I2CDB1, I2CDB0:** I2C debounce selection bits
00: No debounce (default)
01: 1 system clock debounce
10, 11: 2 system clocks debounce

Bit 3~1 Unimplemented

Bit 0 **SA_WCOL:** SPIA WCOL function control
Related to SPIA, described elsewhere.

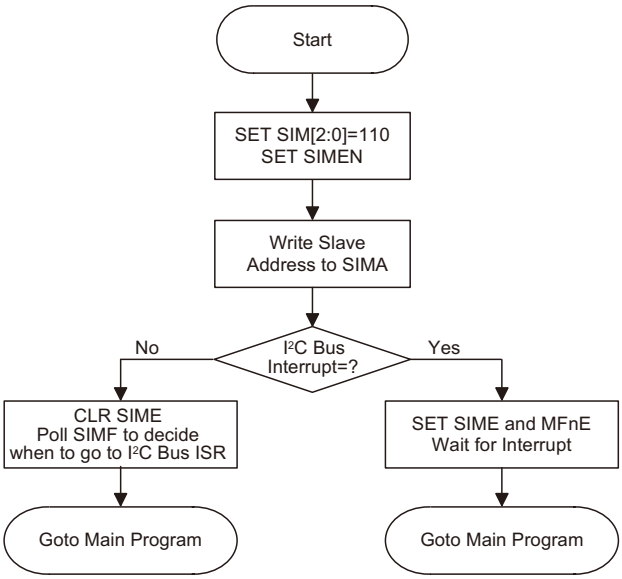


I²C Block Diagram

I²C Bus Communication

Communication on the I²C bus requires four separate steps, a START signal, a slave device address transmission, a data transmission and finally a STOP signal. When a START signal is placed on the I²C bus, all devices on the bus will receive this signal and be notified of the imminent arrival of data on the bus. The first seven bits of the data will be the slave address with the first bit being the MSB. If the address of the slave device matches that of the transmitted address, the HAAS bit in the SIMC1 register will be set and an I²C interrupt will be generated. After entering the interrupt service routine, the slave device must first check the condition of the HAAS bit to determine whether the interrupt source originates from an address match or from the completion of an 8-bit data transfer. During a data transfer, note that after the 7-bit slave address has been transmitted, the following bit, which is the 8th bit, is the read/write bit whose value will be placed in the SRW bit. This bit will be checked by the slave device to determine whether to go into transmit or receive mode. Before any transfer of data to or from the I²C bus, the microcontroller must initialise the bus, the following are steps to achieve this:

- Step 1
  Set the SIM2~SIM0 and SIMEN bits in the SIMC0 register to "1" to enable the I²C bus.
- Step 2
  Write the slave address of the device to the I²C bus address register SIMA.
- Step 3
  Set the SIME and SIM Muti-Function interrupt enable bit of the interrupt control register to enable the SIM interrupt and Multi-function interrupt.



I²C Bus Initialisation Flow Chart

I²C Bus Start Signal

The START signal can only be generated by the master device connected to the I²C bus and not by the slave device. This START signal will be detected by all devices connected to the I²C bus. When detected, this indicates that the I²C bus is busy and therefore the HBB bit will be set. A START condition occurs when a high to low transition on the SDA line takes place when the SCL line remains high.

Slave Address

The transmission of a START signal by the master will be detected by all devices on the I²C bus. To determine which slave device the master wishes to communicate with, the address of the slave device will be sent out immediately following the START signal. All slave devices, after receiving this 7-bit address data, will compare it with their own 7-bit slave address. If the address sent out by the master matches the internal address of the microcontroller slave device, then an internal I²C bus interrupt signal will be generated. The next bit following the address, which is the 8th bit, defines the read/write status and will be saved to the SRW bit of the SIMC1 register. The slave device will then transmit an acknowledge bit, which is a low level, as the 9th bit. The slave device will also set the status flag HAAS when the addresses match.

As an I²C bus interrupt can come from two sources, when the program enters the interrupt subroutine, the HAAS bit should be examined to see whether the interrupt source has come from a matching slave address or from the completion of a data byte transfer. When a slave address is matched, the devices must be placed in either the transmit mode and then write data to the SIMD register, or in the receive mode where it must implement a dummy read from the SIMD register to release the SCL line.

I²C Bus Read/Write Signal

The SRW bit in the SIMC1 register defines whether the slave device wishes to read data from the I²C bus or write data to the I²C bus. The slave device should examine this bit to determine if it is to be a transmitter or a receiver. If the SRW flag is "1" then this indicates that the master device wishes to read data from the I²C bus, therefore the slave device must be setup to send data to the I²C bus as a transmitter. If the SRW flag is "0" then this indicates that the master wishes to send data to the I²C bus, therefore the slave device must be setup to read data from the I²C bus as a receiver.

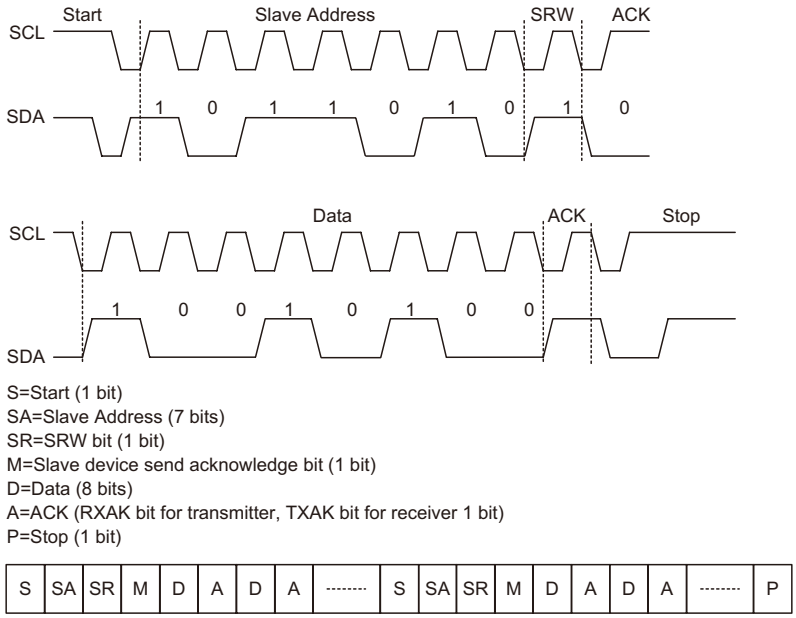
I²C Bus Slave Address Acknowledge Signal

After the master has transmitted a calling address, any slave device on the I²C bus, whose own internal address matches the calling address, must generate an acknowledge signal. The acknowledge signal will inform the master that a slave device has accepted its calling address. If no acknowledge signal is received by the master then a STOP signal must be transmitted by the master to end the communication. When the HAAS flag is high, the addresses have matched and the slave device must check the SRW flag to determine if it is to be a transmitter or a receiver. If the SRW flag is high, the slave device should be setup to be a transmitter so the HTX bit in the SIMC1 register should be set to "1". If the SRW flag is low, then the microcontroller slave device should be setup as a receiver and the HTX bit in the SIMC1 register should be set to "0".

I²C Bus Data and Acknowledge Signal

The transmitted data is 8-bits wide and is transmitted after the slave device has acknowledged receipt of its slave address. The order of serial bit transmission is the MSB first and the LSB last. After receipt of 8-bits of data, the receiver must transmit an acknowledge signal, level "0", before it can receive the next data byte. If the slave transmitter does not receive an acknowledge bit signal from the master receiver, then the slave transmitter will release the SDA line to allow the master to send a STOP signal to release the I²C Bus. The corresponding data will be stored in the SIMD register. If setup as a transmitter, the slave device must first write the data to be transmitted into the SIMD register. If setup as a receiver, the slave device must read the transmitted data from the SIMD register.

When the slave receiver receives the data byte, it must generate an acknowledge bit, known as TXAK, on the 9th clock. The slave device, which is setup as a transmitter will check the RXAK bit in the SIMC1 register to determine if it is to send another data byte, if not then it will release the SDA line and await the receipt of a STOP signal from the master.

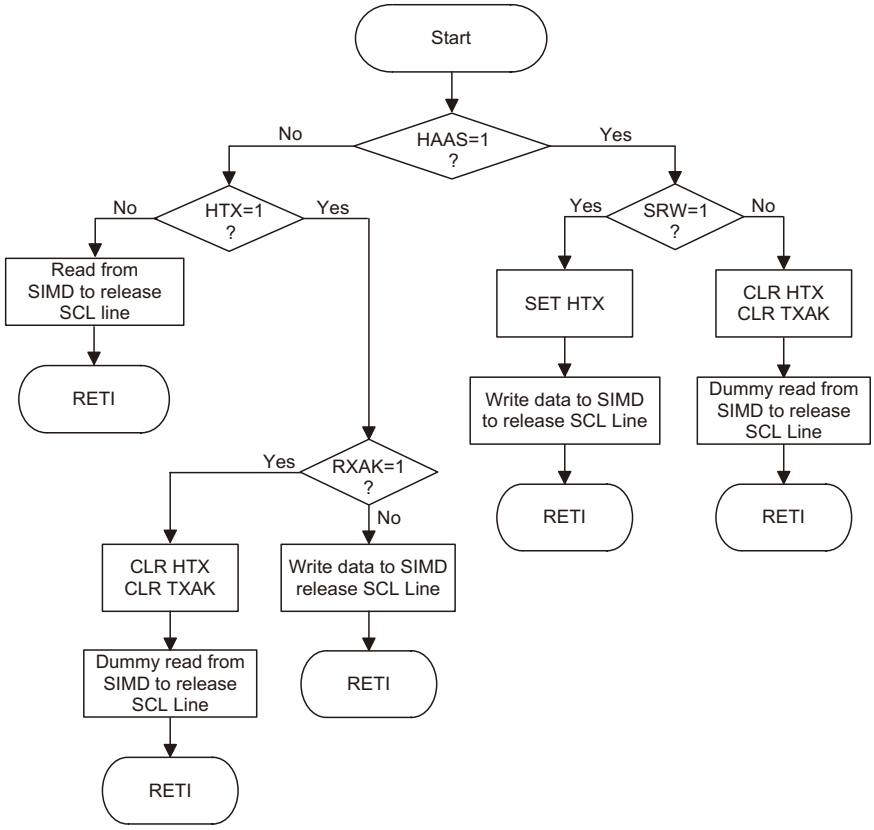


S=Start (1 bit)
SA=Slave Address (7 bits)
SR=SRW bit (1 bit)
M=Slave device send acknowledge bit (1 bit)
D=Data (8 bits)
A=ACK (RXAK bit for transmitter, TXAK bit for receiver 1 bit)
P=Stop (1 bit)

S	SA	SR	M	D	A	D	A	--------	S	SA	SR	M	D	A	D	A	--------	P

I²C Communication Timing Diagram

Note: *When a slave address is matched, the devices must be placed in either the transmit mode and then write data to the SIMD register, or in the receive mode where it must implement a dummy read from the SIMD register to release the SCL line.



I²C Bus ISR flow Chart

I²C Time Out function

The I²C interface provides a time-out scheme to prevent a locked situation which might take place by an unexpected clock timing generated by a niose input signal. When the I²C interface has been locked for a period of time, the I²C hardware and the register, SIMC1, will be initialized automatically and the I2CTOF bit in the I2CTOC register will be set high. The Time Out function eable/disable and the time-out period are managed by the I2CTOC register.

I²C Time Out operation

The time-out counter will start counting when the I²C interface received the START bit and address match. After that the counter will be cleared on each falling edge of the SCL pin. If the time counter is larger than the selected time-out time, then the anti-locked protection scheme will take place and the time-out counter will be stopped by hardware automatically, the I2CTOF bit will be set high and an I²C interrupt will also take place. Note that this scheme can also be stopped when the I²C received the STOP bit. There are several time-out periods can be selected by the I2CTOS0~I2CTOS5 bits in the I2CTOC register.

I2CTOC Register

Bit	7	6	5	4	3	2	1	0
Name	I2CTOEN	I2CTOF	I2CTOS5	I2CTOS4	I2CTOS3	I2CTOS2	I2CTOS1	I2CTOS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **I2CTOEN:** I²C Time Out function control bit
0: Disable
1: Enable

Bit 6 **I2CTOF:** I²C Time Out indication bit
0: Not occurred
1: Occurred

Bit 5~0 **I2CTOS5~I2CTOS0:** I²C Time out time period select
The I²C Time out clock is provided by the $f_{SUB}/32$. The time out time period can be calculated from the accompanying equation ([I2CTOS5: I2CTOS0]+1)×$(32/f_{SUB})$.

Serial Interface – SPIA

The devices contain an independent SPI function. It is important not to confuse this independent SPI function with the additional one contained within the combined SIM function, which is described in another section of this datasheet. This independent SPI function will carry the name SPIA to distinguish it from the other one in the SIM.

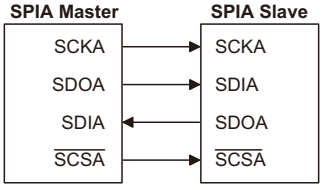
The SPI interface is often used to communicate with external peripheral devices such as sensors, Flash or EEPROM memory devices etc. Originally developed by Motorola, the four line SPI interface is a synchronous serial data interface that has a relatively simple communication protocol simplifying the programming requirements when communicating with external hardware devices.

The communication is full duplex and operates as a slave/master type, where the device can be either master or slave. Although the SPIA interface specification can control multiple slave devices from a single master, however these devices are provided with only one $\overline{\text{SCSA}}$ pin. If the master needs to control multiple slave devices from a single master, the master can use I/O pins to select the slave devices.

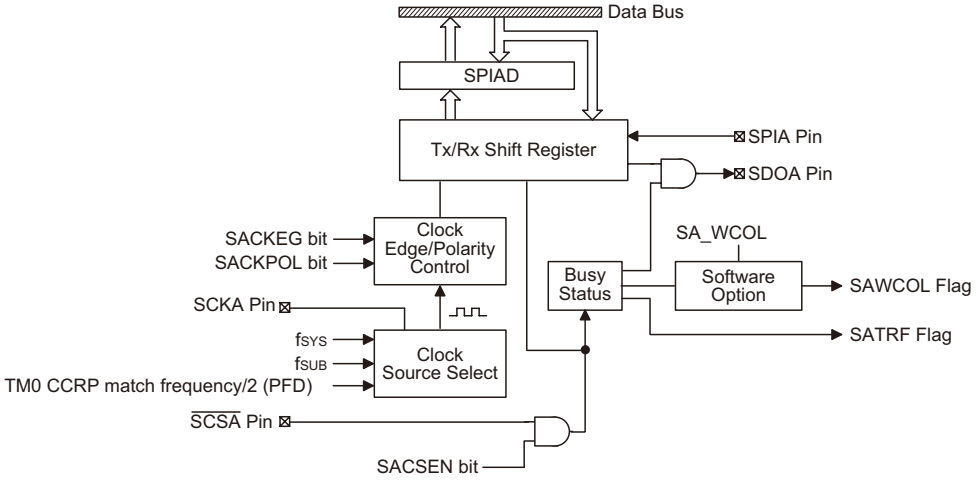
SPIA Interface Operation

The SPIA interface is a full duplex synchronous serial data link. It is a four line interface with pin names SDIA, SDOA, SCKA and $\overline{\text{SCSA}}$. Pins SDIA and SDOA are the Serial Data Input and Serial Data Output lines, SCKA is the Serial Clock line and $\overline{\text{SCSA}}$ is the Slave Select line. As the SPIA interface pins are pin-shared with normal I/O pins, the SPIA interface must first be enabled by setting the correct bits in the SPIAC0 and SPIAC1 registers. The SPIA can be disabled or enabled using the SPIAEN bit in the SPIAC0 register. Communication between devices connected to the SPIA interface is carried out in a slave/master mode with all data transfer initiations being implemented by the master. The Master also controls the clock signal. As the device only contains a single $\overline{\text{SCSA}}$ pin only one slave device can be utilized.

The $\overline{\text{SCSA}}$ pin is controlled by the application program, set the SACSEN bit to "1" to enable the $\overline{\text{SCSA}}$ pin function and clear the SACSEN bit to "0" to place the $\overline{\text{SCSA}}$ pin into a floating state.



SPIA Master/Slave Connection



SPIA Block Diagram

The SPIA function in these devices offers the following features:

- Full duplex synchronous data transfer
- Both Master and Slave modes
- LSB first or MSB first data transmission modes
- Transmission complete flag
- Rising or falling active clock edge
- SAWCOL bit enabled or disable select

The status of the SPIA interface pins is determined by a number of factors such as whether the device is in the master or slave mode and upon the condition of certain control bits such as SACSEN and SPIAEN.

There are several configuration options associated with the SPIA interface. One of these is to enable the SPIA function which selects the SPIA pins rather than normal I/O pins. Note that if the configuration option does not select the SPIA function then the SPIAEN bit in the SPIAC0 register will have no effect. Another two SPIA configuration options determine if the SACSEN and SAWCOL bits are to be used.

SPIA Registers

There are four internal registers which control the overall operation of the SPIA interface. These are the SPIAD data register and three registers SPIAC0, SPIAC1 and SBSC. The SA_WCOL bit in the SBSC register is used to control the SPIA WCOL function.

Register Name	Bit							
	7	6	5	4	3	2	1	0
SPIAC0	SASPI2	SASPI1	SASPI0	—	—	—	SPIAEN	—
SPIAC1	—	—	SACKPOL	SACKEG	SAMLS	SACSEN	SAWCOL	SATRF
SPIAD	D7	D6	D5	D4	D3	D2	D1	D0
SBSC	SIM_WCOL	—	I2CDB1	I2CDB0	—	—	—	SA_WCOL

SPIA Registers List

The SPIAD register is used to store the data being transmitted and received. Before the device writes data to the SPI bus, the actual data to be transmitted must be placed in the SPIAD register. After the data is received from the SPI bus, the device can read it from the SPIAD register. Any transmission or reception of data from the SPI bus must be made via the SPIAD register.

SPIAD Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x" unknown

There are also three control registers for the SPIA interface, SPIAC0, SPIAC1 and SBSC. Register SPIAC0 is used to control the enable/disable function and to set the data transmission clock frequency. Register SPIAC1 is used for other control functions such as LSB/MSB selection, write collision flag etc.

SPIAC0 Register

Bit	7	6	5	4	3	2	1	0
Name	SASPI2	SASPI1	SASPI0	—	—	—	SPIAEN	—
R/W	R/W	R/W	R/W	—	—	—	R/W	—
POR	1	1	1	0	0	0	0	0

Bit 7~5 **SASPI2~SASPI0:** Master/Slave Clock Select
000 : SPIA master, $f_{SYS}/4$
001 : SPIA master, $f_{SYS}/16$
010 : SPIA master, $f_{SYS}/64$
011 : SPIA master, f_{TBC}
100 : SPIA master, TM0 CCRP match frequency/2 (PFD)
101 : SPIA slave
110: Unimplemented
111: Unimplemented
These bits are used to control the SPI Master/Slave selection and the SPIA Master clock frequency. The SPIA clock is a function of the system clock but can also be chosen to be sourced from TM0. If the SPIA Slave Mode is selected then the clock will be supplied by an external Master device.

Bit 4~2 Unimplemented, read as "0"

Bit 1 **SPIAEN:** SPIA enable or disable
0: Disable
1: Enable
The bit is the overall on/off control for the SIMA interface. When the SPIAEN bit is cleared to zero to disable the SPIA interface, the SDIA, SDOA, SCKA and $\overline{SCSA}$ lines will lose their SPI function and the SPIA operating current will be reduced to a minimum value. When the bit is high the SPIA interface is enabled.

Bit 0 Unimplemented, read as "0"

SPIAC1 Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	SACKPOL	SACKEG	SAMLS	SACSEN	SAWCOL	SATRF
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 Unimplemented, read as "0".
This bit can be read or written by user software program.

Bit 5 **SACKPOL:** Determines the base condition of the clock line
0: SCKA line will be high when the clock is inactive
1: SCKA line will be low when the clock is inactive
The SACKPOL bit determines the base condition of the clock line, if the bit is high, then the SCKA line will be low when the clock is inactive. When the SACKPOL bit is low, then the SCKA line will be high when the clock is inactive.

Bit 4 **SACKEG:** Determines the SPIA SCKA active clock edge type
SACKPOL=0
0: SCKA has high base level with data capture on SCKA rising edge
1: SCKA has high base level with data capture on SCKA falling edge
SACKPOL=1
0: SCKA has low base level with data capture on SCKA falling edge
1: SCKA has low base level with data capture on SCKA rising edge
The SACKEG and SACKPOL bits are used to setup the way that the clock signal outputs and inputs data on the SPI bus. These two bits must be configured before a data transfer is executed otherwise an erroneous clock edge may be generated. The SACKPOL bit determines the base condition of the clock line, if the bit is high, then the SCKA line will be low when the clock is inactive. When the SACKPOL bit is low, then the SCKA line will be high when the clock is inactive. The SACKEG bit determines active clock edge type which depends upon the condition of the SACKPOL bit.

Bit 3 **SAMLS:** MSB/LSB First Bit
0: LSB shift first
1: MSB shift first
This is the data shift select bit and is used to select how the data is transferred, either MSB or LSB first. Setting the bit high will select MSB first and low for LSB first.

Bit 2 **SACSEN:** Select Signal Enable/Disable Bit
0: Disable, other functions
1: Enable
The SACSEN bit is used as an enable/disable for the $\overline{\text{SCSA}}$ pin. If this bit is low, then the $\overline{\text{SCSA}}$ pin will be disabled and placed into other functions. If the bit is high the $\overline{\text{SCSA}}$ pin will be enabled and used as a select pin.

Bit 1 **SAWCOL:** Write Collision Bit
0: Collision free
1: Collision detected
The SAWCOL flag is used to detect if a data collision has occurred. If this bit is high it means that data has been attempted to be written to the SPIAD register during a data transfer operation. This writing operation will be ignored if data is being transferred. The bit can be cleared by the application program. Note that this function can be disabled or enabled via the SA_WCOL bit in the SBSC register.

Bit 0 **SATRF:** Transmit/Receive Flag
0: Not complete
1: Transmission/reception complete
The SATRF bit is the Transmit/Receive Complete flag and is set "1" automatically when an SPIA data transmission is completed, but must set to zero by the application program. It can be used to generate an interrupt.

SBSC Register

Bit	7	6	5	4	3	2	1	0
Name	SIM_WCOL	—	I2CDB1	I2CDB0	—	—	—	SA_WCOL
R/W	R/W	R	R/W	R/W	R	R	R	R/W
POR	0	0	0	0	0	0	0	0

Bit 7: **SIM_WCOL:** SIM WCOL control bit
Related to SPI, described elsewhere.

Bit 6: Unimplemented

Bit 5, 4: **I2CDB1, I2CDB0:** I^2C debounce selection bits
Related to I^2C, described elsewhere.

Bit 3~1: Unimplemented

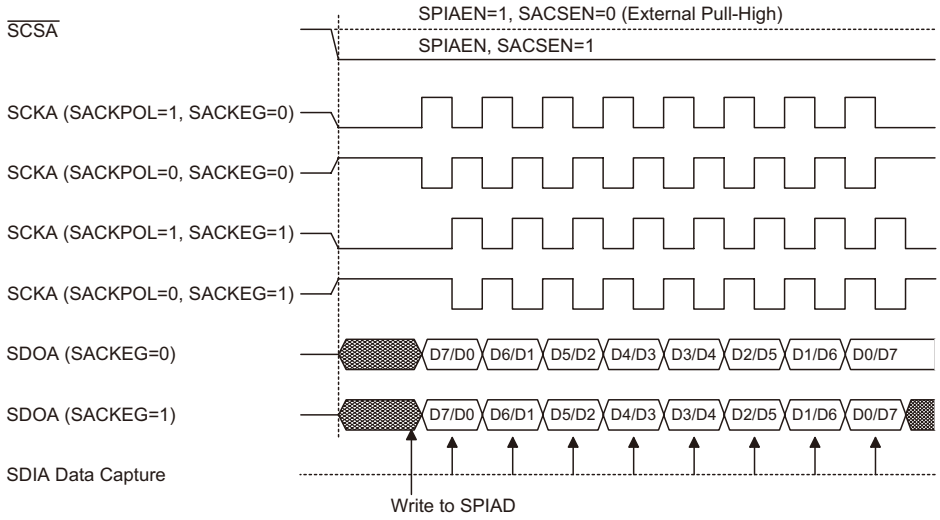
Bit 0: **SA_WCOL:** SPIA WCOL function control
0: Disable
1: Enable

SPIA Communication

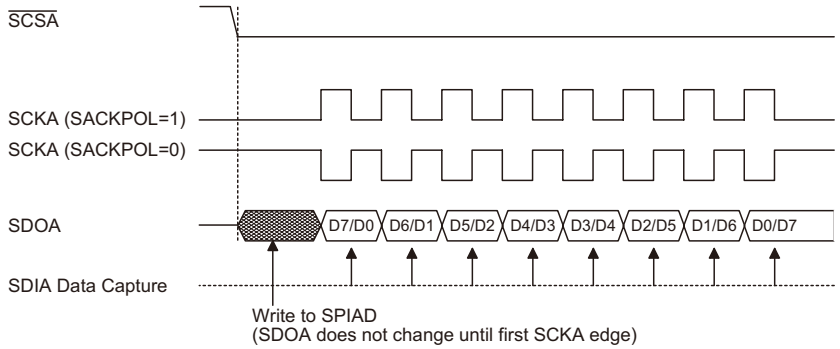
After the SPIA interface is enabled by setting the SPIAEN bit high, then in the Master Mode, when data is written to the SPIAD register, transmission/reception will begin simultaneously. When the data transfer is complete, the SATRF flag will be set automatically, but must be cleared using the application program. In the Slave Mode, when the clock signal from the master has been received, any data in the SPIAD register will be transmitted and any data on the SDIA pin will be shifted into the SPIAD register.

The master should output an $\overline{SCSA}$ signal to enable the slave device before a clock signal is provided. The slave data to be transferred should be well prepared at the appropriate moment relative to the $\overline{SCSA}$ signal depending upon the configurations of the SACKPOL bit and SACKEG bit. The accompanying timing diagram shows the relationship between the slave data and $\overline{SCS}$ signal for various configurations of the SACKPOL and SACKEG bits.

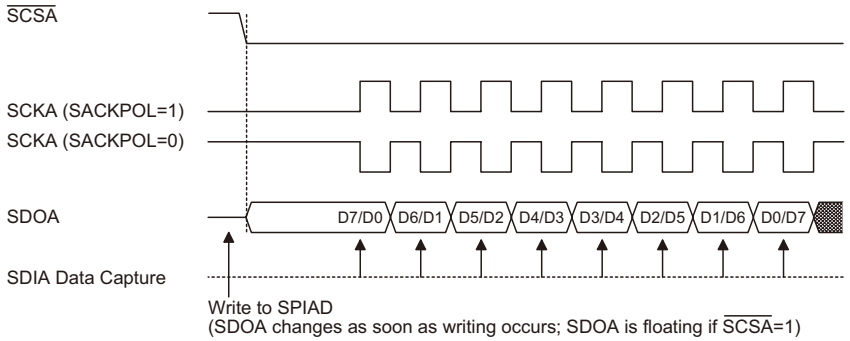
The SPIA will continue to function even in the IDLE Mode.



SPIA Master Mode Timing

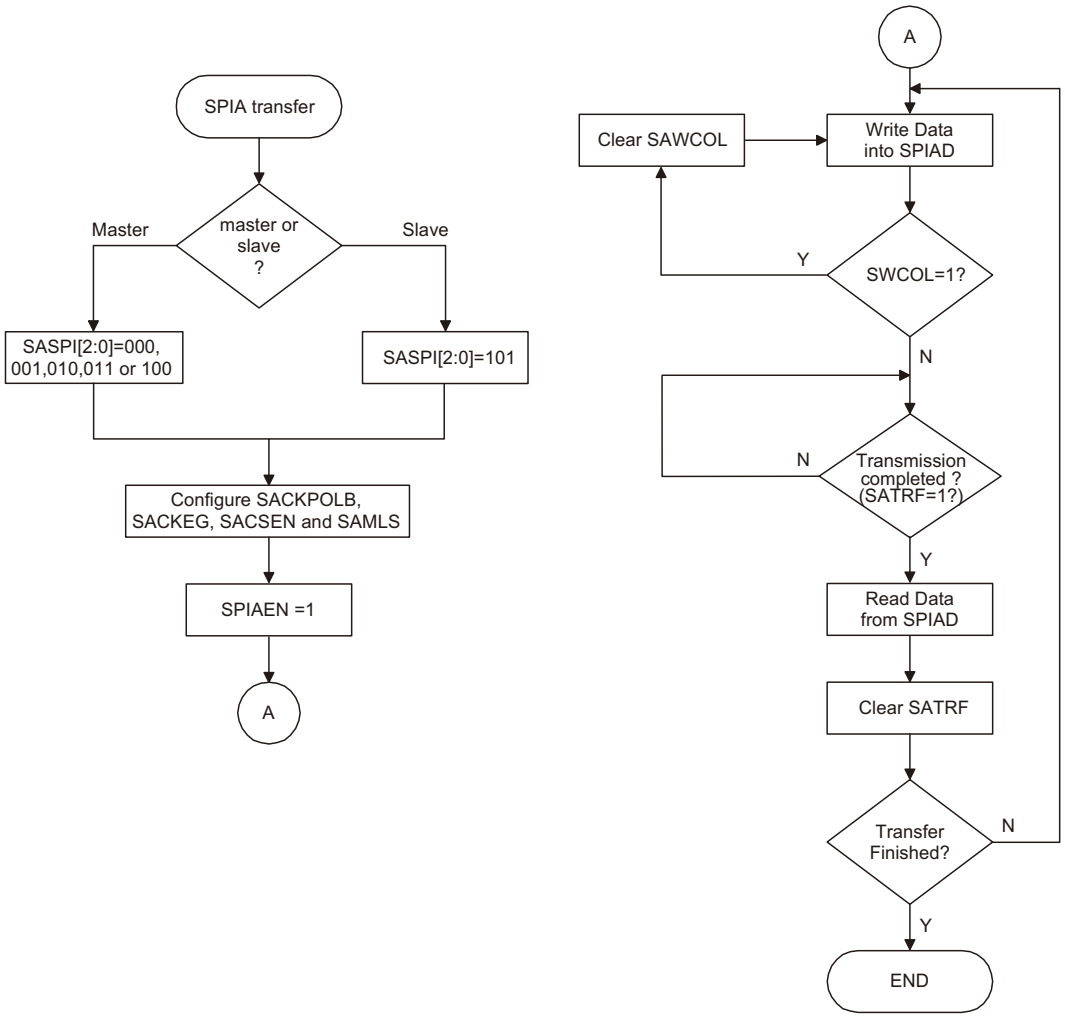


SPIA Slave Mode Timing – SACKEG=0



Note: For SPIA slave mode, if SPLAEN=1 and SACSEN=0, SPIA is always enabled and ignores the $\overline{SCSA}$ level.

SPIA Slave Mode Timing – SACKEG=1



SPI Transfer Control Flowchart

SPIA Bus Enable/Disable

To enable the SPIA bus, set SACSEN=1 and $\overline{SCSA}$=0, then wait for data to be written into the SPIAD (TXRX buffer) register. For the Master Mode, after data has been written to the SPIAD (TXRX buffer) register, then transmission or reception will start automatically. When all the data has been transferred the SATRF bit should be set. For the Slave Mode, when clock pulses are received on SCKA, data in the TXRX buffer will be shifted out or data on SDIA will be shifted in.

To Disable the SPIA bus SCKA, SDIA, SDOA, $\overline{SCSA}$ will become I/O pins or the other functions.

SPIA Operation

All communication is carried out using the 4-line interface for either Master or Slave Mode.

The SACSEN bit in the SPIAC1 register controls the overall function of the SPIA interface. Setting this bit high will enable the SPIA interface by allowing the $\overline{SCSA}$ line to be active, which can then be used to control the SPIA interface. If the SACSEN bit is low, the SPIA interface will be disabled and the $\overline{SCSA}$ line will be an I/O pin or the other functions and can therefore not be used for control of the SPIA interface. If the SACSEN bit and the SPIAEN bit in the SPIAC0 register are set high, this will place the SDIA line in a floating condition and the SDOA line high. If in Master Mode the SCKA line will be either high or low depending upon the clock polarity selection bit SACKPOLB in the SPIAC1 register. If in Slave Mode the SCKA line will be in a floating condition. If SPIAEN is low then the bus will be disabled and $\overline{SCSA}$, SDIA, SDOA and SCKA will all become I/O pins or the other functions. In the Master Mode the Master will always generate the clock signal. The clock and data transmission will be initiated after data has been written into the SPIAD register. In the Slave Mode, the clock signal will be received from an external master device for both data transmission and reception. The following sequences show the order to be followed for data transfer in both Master and Slave Mode.

Master Mode:

- Step 1
  Select the clock source and Master mode using the SASPI2~SASPI0 bits in the SPIAC0 control register.
- Step 2
  Setup the SACSEN bit and setup the SAMLS bit to choose if the data is MSB or LSB first, this must be same as the Slave device.
- Step 3
  Setup the SPIAEN bit in the SPIAC0 control register to enable the SPIA interface.
- Step 4
  For write operations: write the data to the SPIAD register, which will actually place the data into the TXRX buffer. Then use the SCKA and $\overline{SCSA}$ lines to output the data. After this go to step 5.
  For read operations: the data transferred in on the SDIA line will be stored in the TXRX buffer until all the data has been received at which point it will be latched into the SPIAD register.
- Step 5
  Check the SAWCOL bit if set high then a collision error has occurred so return to step 4. If equal to zero then go to the following step.
- Step 6
  Check the SATRF bit or wait for a SPIA serial bus interrupt.
- Step 7
  Read data from the SPIAD register.
- Step 8
  Clear SATRF.
- Step 9
  Go to step 4.

Slave Mode:

- Step 1
  Select the SPI Slave mode using the SASPI2~SASPI0 bits in the SPIAC0 control register.
- Step 2
  Setup the SACSEN bit and setup the SAMLS bit to choose if the data is MSB or LSB first, this setting must be the same with the Master device.
- Step 3
  Setup the SPIAEN bit in the SPIAC0 control register to enable the SPIA interface.
- Step 4
  For write operations: write the data to the SPIAD register, which will actually place the data into the TXRX buffer. Then wait for the master clock SCKA and $\overline{\text{SCSA}}$ signal. After this, go to step 5.
  For read operations: the data transferred in on the SDIA line will be stored in the TXRX buffer until all the data has been received at which point it will be latched into the SPIAD register.
- Step 5
  Check the SAWCOL bit if set high then a collision error has occurred so return to step 4. If equal to zero then go to the following step.
- Step 6
  Check the SATRF bit or wait for a SPIA serial bus interrupt.
- Step 7
  Read data from the SPIAD register.
- Step 8
  Clear SATRF.
- Step 9
  Go to step 4.

Error Detection

The SAWCOL bit in the SPIAC register is provided to indicate errors during data transfer. The bit is set by the SPIA serial Interface but must be cleared by the application program. This bit indicates a data collision has occurred which happens if a write to the SPIAD register takes place during a data transfer operation and will prevent the write operation from continuing. The overall function of the SAWCOL bit can be disabled or enabled by the SA_WCOL bit in the SBSC register.

Peripheral Clock Output

The Peripheral Clock Output allows the device to supply external hardware with a clock signal synchronised to the microcontroller clock.

Peripheral Clock Operation

As the peripheral clock output pin, PCK, is shared with I/O line, the required pin function is chosen via PCKEN in the SIMC0 register. The Peripheral Clock function is controlled using the SIMC0 register. The clock source for the Peripheral Clock Output can originate from either the TM0 CCRP match frequency/2 or a divided ratio of the internal f_{SYS} clock. The PCKEN bit in the SIMC0 register is the overall on/off control, setting PCKEN bit to "1" enables the Peripheral Clock, setting PCKEN bit to "0" disables it. The required division ratio of the system clock is selected using the PCKP1 and PCKP0 bits in the same register. If the device enters the SLEEP Mode this will disable the Peripheral Clock output.

SIMC0 Register

Bit	7	6	5	4	3	2	1	0
Name	SIM2	SIM1	SIM0	PCKEN	PCKP1	PCKP0	SIMEN	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—
POR	1	1	1	0	0	0	0	—

Bit 7~5 **SIM2, SIM1, SIM0:** SIM operating mode control
000: SPI master mode; SPI clock is $f_{SYS}/4$
001: SPI master mode; SPI clock is $f_{SYS}/16$
010: SPI master mode; SPI clock is $f_{SYS}/64$
011: SPI master mode; SPI clock is f_{TBC}
100: SPI master mode; SPI clock is TM0 CCRP match frequency/2
101: SPI slave mode
110: I^2C slave mode
111: Non SIM function

These bits setup the overall operating mode of the SIM function. As well as selecting if the I^2C or SPI function, they are used to control the SPI Master/Slave selection and the SPI Master clock frequency. The SPI clock is a function of the system clock but can also be chosen to be sourced from the TM0. If the SPI Slave Mode is selected then the clock will be supplied by an external Master device.

Bit 4 **PCKEN:** PCK output pin control
0: Disable
1: Enable

Bit 3~2 **PCKP1, PCKP0:** select PCK output pin frequency
00: f_{SYS}
01: $f_{SYS}/4$
10: $f_{SYS}/8$
11: TM0 CCRP match frequency/2

Bit 1 **SIMEN:** SIM control
0: Disable
1: Enable

The bit is the overall on/off control for the SIM interface. When the SIMEN bit is cleared to zero to disable the SIM interface, the SDI, SDO, SCK and $\overline{SCS}$, or SDA and SCL lines will be in a floating condition and the SIM operating current will be reduced to a minimum value. When the bit is high the SIM interface is enabled. Note that when the SIMEN bit changes from low to high the contents of the SPI control registers will be in an unknown condition and should therefore be first initialised by the application program.

Bit 0 Unimplemented

Interrupts

Interrupts are an important part of any microcontroller system. When an external event or an internal function such as a Timer Module or an A/D converter requires microcontroller attention, their corresponding interrupt will enforce a temporary suspension of the main program allowing the microcontroller to direct attention to their respective needs. The device contains several external interrupt and internal interrupts functions. The external interrupts are generated by the action of the external INT0~INT1 and PINT pins, while the internal interrupts are generated by various internal functions such as the TMs, Comparators,Time Base, LVD, SIM , SPI , USB, and the A/D converter.

Interrupt Registers

Overall interrupt control, which basically means the setting of request flags when certain microcontroller conditions occur and the setting of interrupt enable bits by the application program, is controlled by a series of registers, located in the Special Purpose Data Memory, as shown in the accompanying table. The number of registers depends upon the device chosen but fall into three categories. The first is the INTC0~INTC3 registers which setup the primary interrupts, the second is the MFI0~MFI2 registers which setup the Multi-function interrupts. Finally there is an INTEG register to setup the external interrupt trigger edge type.

Each register contains a number of enable bits to enable or disable individual registers as well as interrupt flags to indicate the presence of an interrupt request. The naming convention of these follows a specific pattern. First is listed an abbreviated interrupt type, then the (optional) number of that interrupt followed by either an “E” for enable/disable bit or “F” for request flag.

Function	Enable Bit	Request Flag	Notes
Global	EMI	—	—
Comparator	CPnE	CPnF	n=0 or 1
INTn Pin	INTnE	INTnF	n=0 or 1
A/D Converter	ADE	ADF	—
Multi-function	MFnE	MFnF	n=0~4
Time Base	TBnE	TBnF	n=0 or 1
SIM	SIME	SIMF	—
SPIA	SPIAE	SPIAF	—
LVD	LVE	LVF	—
TM	TnPE	TnPF	n=0~3
	TnAE	TnAF	
USB	USBE	USBF	—

Interrupt Register Bit Naming Conventions

Interrupt Register Contents

Name	Bit							
	7	6	5	4	3	2	1	0
INTEG	—	—	—	—	INT1S1	INT1S0	INT0S1	INT0S0
INTC0	—	USBF	INT1F	INT0F	USBE	INT1E	INT0E	EMI
INTC1	MF1F	MF0F	CP1F	CP0F	MF1E	MF0E	CP1E	CP0E
INTC2	SPIAF	SIMF	MF3F	MF2F	SPIAE	SIME	MF3E	MF2E
INTC3	—	MF4F	TB1F	TB0F	—	MF4E	TB1E	TB0E
MFI0	T1AF	T1PF	T0AF	T0PF	T1AE	T1PE	T0AE	T0PE
MFI1	T3AF	T3PF	T2AF	T2PF	T3AE	T3PE	T2AE	T2PE
MFI2	—	ADF	—	LVF	—	ADE	—	LVE

INTEG Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	INT1S1	INT1S0	INT0S1	INT0S0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~4 Unimplemented, read as "0"

Bit 3~2 **INT1S1, INT1S0:** interrupt edge control for INT1 pin
00: Disable
01: Rising edge
10: Falling edge
11: Rising and falling edges

Bit 1~0 **INT0S1, INT0S0:** interrupt edge control for INT0 pin
00: Disable
01: Rising edge
10: Falling edge
11: Rising and falling edges

INTC0 Register

Bit	7	6	5	4	3	2	1	0
Name	—	USBF	INT1F	INT0F	USBE	INT1E	INT0E	EMI
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 Unimplemented, read as "0"

Bit 6 **USBF:** USB Interrupt Request Flag
0: No request
1: Interrupt request

Bit 5 **INT1F:** INT1 interrupt request flag
0: No request
1: Interrupt request

Bit 4 **INT0F:** INT0 interrupt request flag
0: No request
1: Interrupt request

Bit 3 **USBE:** USB Interrupt Control
0: Disable
1: Enable

Bit 2 **INT1E:** INT1 interrupt control
0: Disable
1: Enable

Bit 1 **INT0E:** INT0 interrupt control
0: Disable
1: Enable

Bit 0 **EMI:** Global interrupt control
0: Disable
1: Enable

INTC1 Register

Bit	7	6	5	4	3	2	1	0
Name	MF1F	MF0F	CP1F	CP0F	MF1E	MF0E	CP1E	CP0E
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **MF1F:** Multi-function Interrupt 1 Request Flag
0: No request
1: Interrupt request

Bit 6 **MF0F:** Multi-function Interrupt 0 Request Flag
0: No request
1: Interrupt request

Bit 5 **CP1F:** Comparator 1 Interrupt Request Flag
0: no request
1: interrupt request

Bit 4 **CP0F:** Comparator 0 Interrupt Request Flag
0: No request
1: Interrupt request

Bit 3 **MF1E:** Multi-function Interrupt 1 Interrupt Control
0: Disable
1: Enable

Bit 2 **MF0E:** Multi-function Interrupt 0 Interrupt Control
0: Disable
1: Enable

Bit 1 **CP1E:** Comparator 1 Interrupt Control
0: Disable
1: Enable

Bit 0 **CP0E:** Comparator 0 Interrupt Control
0: Disable
1: Enable

INTC2 Register

Bit	7	6	5	4	3	2	1	0
Name	SPIAF	SIMF	MF3F	MF2F	SPIAE	SIME	MF3E	MF2E
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **SPIAF:** SPIA interrupt request flag
0: No request
1: Interrupt request

Bit 6 **SIMF:** SIM interrupt request flag
0: No request
1: Interrupt request

Bit 5 **MF3F:** Multi-function Interrupt 3 Request Flag
0: No request
1: Interrupt request

Bit 4 **MF2F:** Multi-function Interrupt 2 Request Flag
0: No request
1: Interrupt request

Bit 3 **SPIAE:** SPIA Interrupt Control
0: Disable
1: Enable

Bit 2 **SIME:** SIM Interrupt Control
0: Disable
1: Enable

Bit 1 **MF3E:** Multi-function Interrupt 3 Control
0: Disable
1: Enable

Bit 0 **MF2E:** Multi-function Interrupt 2 Control
0: Disable
1: Enable

INTC3 Register

Bit	7	6	5	4	3	2	1	0
Name	—	MF4F	TB1F	TB0F	—	MF4E	TB1E	TB0E
R/W	—	R/W	R/W	R/W	—	R/W	R/W	R/W
POR	—	0	0	0	—	0	0	0

Bit 7 Unimplemented

Bit 6 **MF4F:** Multi-function Interrupt 4 request flag
0: Inactive
1: Active

Bit 5 **TB1F:** Time Base 1 Interrupt Request Flag
0: Inactive
1: Active

Bit 4 **TB0F:** Time Base 0 Interrupt Request Flag
0: Inactive
1: Active

Bit 3 Unimplemented

Bit 2 **MF4E:** Multi-function Interrupt 4 Control
0: No request
1: Interrupt request

Bit 1 **TB1E:** Time Base 1 Interrupt Control
0: Disable
1: Enable

Bit 0 **TB0E:** Time Base 0 Interrupt Control
0: Disable
1: Enable

MFI0 Register

Bit	7	6	5	4	3	2	1	0
Name	T1AF	T1PF	T0AF	T0PF	T1AE	T1PE	T0AE	T0PE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **T1AF:** TM1 Comparator A match interrupt request flag
0: No request
1: Interrupt request

Bit 6 **T1PF:** TM1 Comparator P match interrupt request flag
0: No request
1: Interrupt request

Bit 5 **T0AF:** TM0 Comparator A match interrupt request flag
0: No request
1: Interrupt request

Bit 4 **T0PF:** TM0 Comparator P match interrupt request flag
0: No request
1: Interrupt request

Bit 3 **T1AE:** TM1 Comparator A match interrupt control
0: Disable
1: Enable

Bit 2 **T1PE:** TM1 Comparator P match interrupt control
0: Disable
1: Enable

Bit 1 **T0AE:** TM0 Comparator A match interrupt control
0: Disable
1: Enable

Bit 0 **T0PE:** TM0 Comparator P match interrupt control
0: Disable
1: Enable

MFI1 Register

Bit	7	6	5	4	3	2	1	0
Name	T3AF	T3PF	T2AF	T2PF	T3AE	T3PE	T2AE	T2PE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **T3AF:** TM3 Comparator A match interrupt request flag
0: No request
1: Interrupt request

Bit 6 **T3PF:** TM3 Comparator P match interrupt request flag
0: No request
1: Interrupt request

Bit 5 **T2AF:** TM2 Comparator A match interrupt request flag
0: No request
1: Interrupt request

Bit 4 **T2PF:** TM2 Comparator P match interrupt request flag
0: No request
1: Interrupt request

Bit 3 **T3AE:** TM3 Comparator A match interrupt control
0: Disable
1: Enable

Bit 2 **T3PE:** TM3 Comparator P match interrupt control
0: Disable
1: Enable

Bit 1 **T2AE:** TM2 Comparator A match interrupt control
0: Disable
1: Enable

Bit 0 **T2PE:** TM2 Comparator P match interrupt control
0: Disable
1: Enable

MFI2 Register

Bit	7	6	5	4	3	2	1	0
Name	—	ADF	—	LVF	—	ADE	—	LVE
R/W	—	R/W	—	R/W	—	R/W	—	R/W
POR	—	0	—	0	—	0	—	0

Bit 7 Unimplemented

Bit 6 **ADF:** ADC Converter interrupt request flag
0: No request
1: Interrupt request

Bit 5 Unimplemented

Bit 4 **LVF:** LVD interrupt request flag
0: No request
1: Interrupt request

Bit 3 Unimplemented

Bit 2 **ADE:** ADC Converter Interrupt Control
0: Disable
1: Enable

Bit 1 Unimplemented

Bit 0 **LVE:** LVD Interrupt Control
0: Disable
1: Enable

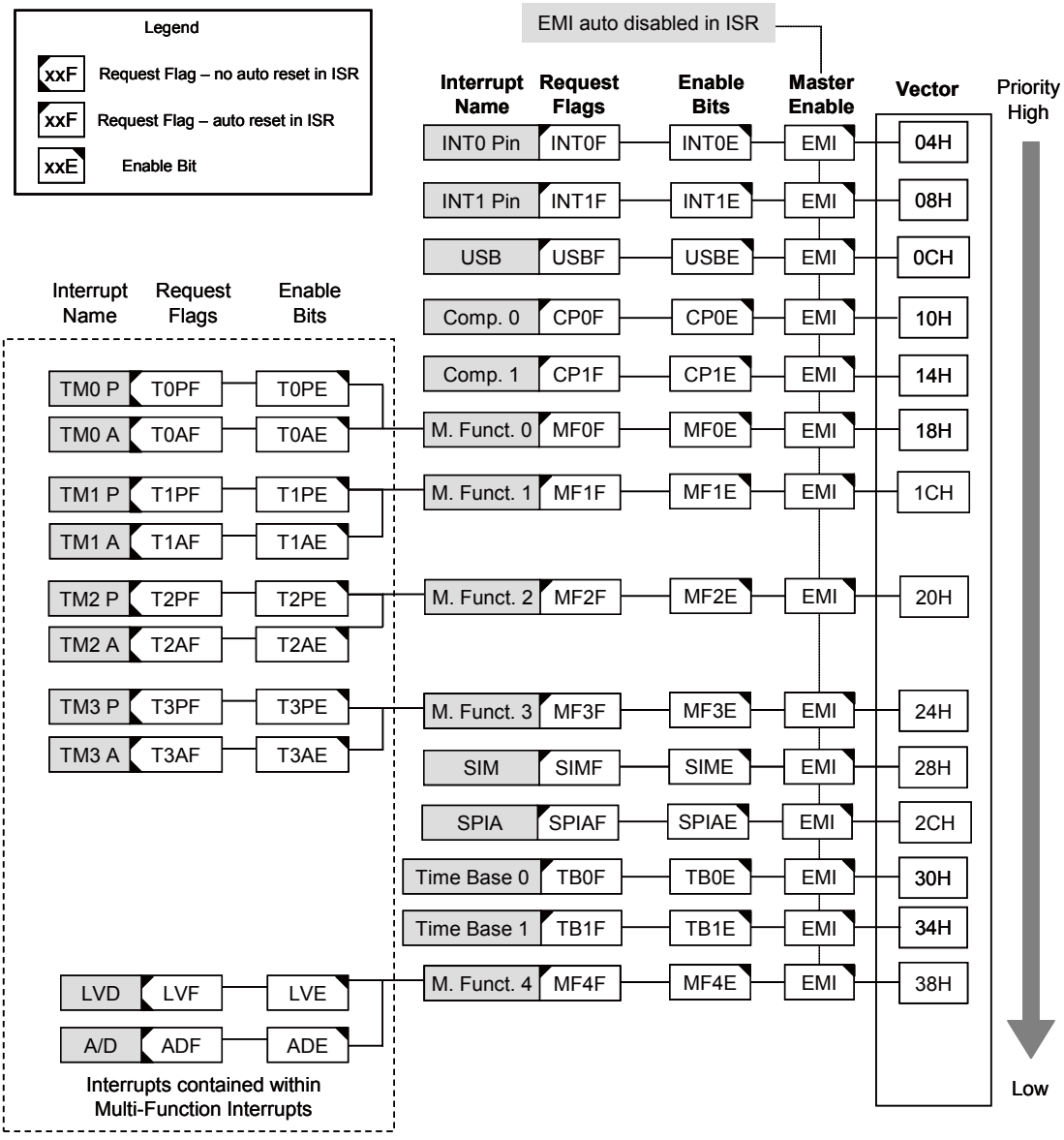
Interrupt Operation

When the conditions for an interrupt event occur, such as a TM Compare P, Compare A or Compare B match or A/D conversion completion etc, the relevant interrupt request flag will be set. Whether the request flag actually generates a program jump to the relevant interrupt vector is determined by the condition of the interrupt enable bit. If the enable bit is set high then the program will jump to its relevant vector; if the enable bit is zero then although the interrupt request flag is set an actual interrupt will not be generated and the program will not jump to the relevant interrupt vector. The global interrupt enable bit, if cleared to zero, will disable all interrupts.

When an interrupt is generated, the Program Counter, which stores the address of the next instruction to be executed, will be transferred onto the stack. The Program Counter will then be loaded with a new address which will be the value of the corresponding interrupt vector. The microcontroller will then fetch its next instruction from this interrupt vector. The instruction at this vector will usually be a “JMP” which will jump to another section of program which is known as the interrupt service routine. Here is located the code to control the appropriate interrupt. The interrupt service routine must be terminated with a “RETI”, which retrieves the original Program Counter address from the stack and allows the microcontroller to continue with normal execution at the point where the interrupt occurred.

The various interrupt enable bits, together with their associated request flags, are shown in the accompanying diagrams with their order of priority. Some interrupt sources have their own individual vector while others share the same multi-function interrupt vector. Once an interrupt subroutine is serviced, all the other interrupts will be blocked, as the global interrupt enable bit, EMI bit will be cleared automatically. This will prevent any further interrupt nesting from occurring. However, if other interrupt requests occur during this interval, although the interrupt will not be immediately serviced, the request flag will still be recorded.

If an interrupt requires immediate servicing while the program is already in another interrupt service routine, the EMI bit should be set after entering the routine, to allow interrupt nesting. If the stack is full, the interrupt request will not be acknowledged, even if the related interrupt is enabled, until the Stack Pointer is decremented. If immediate service is desired, the stack must be prevented from becoming full. In case of simultaneous requests, the accompanying diagram shows the priority that is applied. All of the interrupt request flags when set will wake-up the device if it is in SLEEP or IDLE Mode, however to prevent a wake-up from occurring the corresponding flag should be set before the device is in SLEEP or IDLE Mode.



External Interrupt

The external interrupts are controlled by signal transitions on the pins INT0 and INT1. An external interrupt request will take place when the external interrupt request flags, INT0F, INT1F, are set, which will occur when a transition, whose type is chosen by the edge select bits, appears on the external interrupt pins. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and respective external interrupt enable bit, INT0E, INT1E, must first be set. Additionally the correct interrupt edge type must be selected using the INTEG register to enable the external interrupt function and to choose the trigger edge type. As the external interrupt pins are pin-shared with I/O pins, they can only be configured as external interrupt pins if their external interrupt enable bit in the corresponding interrupt register has been set. The pin must also be setup as an input by setting the corresponding bit in the port control register. When the interrupt is enabled, the stack is not full and the correct transition type appears on the external interrupt pin, a subroutine call to the external interrupt vector, will take place. When the interrupt is serviced, the external interrupt request flags, INT0F, INT1F, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts. Note that any pull-high resistor selections on the external interrupt pins will remain valid even if the pin is used as an external interrupt input.

The INTEG register is used to select the type of active edge that will trigger the external interrupt. A choice of either rising or falling or both edge types can be chosen to trigger an external interrupt. Note that the INTEG register can also be used to disable the external interrupt function.

Comparator Interrupt

The comparator interrupts are controlled by the two internal comparators. A comparator interrupt request will take place when the comparator interrupt request flags, CP0F or CP1F, are set, a situation that will occur when the comparator output changes state. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and comparator interrupt enable bits, CP0E and CP1E, must first be set. When the interrupt is enabled, the stack is not full and the comparator inputs generate a comparator output transition, a subroutine call to the comparator interrupt vector, will take place. When the interrupt is serviced, the comparator interrupt request flags, CP0F, CP1F, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts.

USB Interrupt

A USB interrupt request will take place when the USB interrupt request flags, USBF, is set, a situation that will occur when an endpoint is accessed. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and USB interrupt enable bit, USBE, must first be set. When the interrupt is enabled, the stack is not full and an endpoint is accessed, a subroutine call to the USB interrupt vector, will take place. When the interrupt is serviced, the USB interrupt request flag, USBF, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts.

Multi-function Interrupt

Within these devices there are up to five Multi-function interrupts. Unlike the other independent interrupts, these interrupts have no independent source, but rather are formed from other existing interrupt sources, namely the TM Interrupts, SIM Interrupt, SPIA Interrupt, ADC Interrupt and LVD Interrupt.

A Multi-function interrupt request will take place when any of the Multi-function interrupt request flags, MF0F~MF4F are set. The Multi-function interrupt flags will be set when any of their included functions generate an interrupt request flag. To allow the program to branch to its respective interrupt vector address, when the Multi-function interrupt is enabled and the stack is not full, and either one of the interrupts contained within each of Multi-function interrupt occurs, a subroutine call to one of the Multi-function interrupt vectors will take place. When the interrupt is serviced, the related Multi-Function request flag will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts.

However, it must be noted that, although the Multi-function Interrupt flags will be automatically reset when the interrupt is serviced, the request flags from the original source of the Multi-function interrupts, namely the TM Interrupts, ADC Interrupt and LVD interrupt will not be automatically reset and must be manually reset by the application program.

A/D Converter Interrupt

The A/D Converter Interrupt is contained within the Multi-function Interrupt. An A/D Converter Interrupt request will take place when the A/D Converter Interrupt request flag, ADF, is set, which occurs when the A/D conversion process finishes. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and A/D Interrupt enable bit, ADE, and associated Multi-function interrupt enable bit, must first be set. When the interrupt is enabled, the stack is not full and the A/D conversion process has ended, a subroutine call to the Multi-function Interrupt vector, will take place. When the A/D Converter Interrupt is serviced, the EMI bit will be automatically cleared to disable other interrupts, however only the Multi-function interrupt request flag will be also automatically cleared. As the ADF flag will not be automatically cleared, it has to be cleared by the application program.

Time Base Interrupts

The function of the Time Base Interrupts is to provide regular time signal in the form of an internal interrupt. They are controlled by the overflow signals from their respective timer functions. When these happens their respective interrupt request flags, TB0F or TB1F will be set. To allow the program to branch to their respective interrupt vector addresses, the global interrupt enable bit, EMI and Time Base enable bits, TB0E or TB1E, must first be set. When the interrupt is enabled, the stack is not full and the Time Base overflows, a subroutine call to their respective vector locations will take place. When the interrupt is serviced, the respective interrupt request flag, TB0F or TB1F, will be automatically reset and the EMI bit will be cleared to disable other interrupts.

The purpose of the Time Base Interrupt is to provide an interrupt signal at fixed time periods. Their clock sources originate from the internal clock source f_{TB}. This f_{TB} input clock passes through a divider, the division ratio of which is selected by programming the appropriate bits in the TBC register to obtain longer interrupt periods whose value ranges. The clock source that generates f_{TB}, which in turn controls the Time Base interrupt period, can originate from several different sources, as shown in the System Operating Mode section.

TBC Register

Bit	7	6	5	4	3	2	1	0
Name	TBON	TBCK	TB11	TB10	LXTLP	TB02	TB01	TB00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	1	1	0	1	1	1

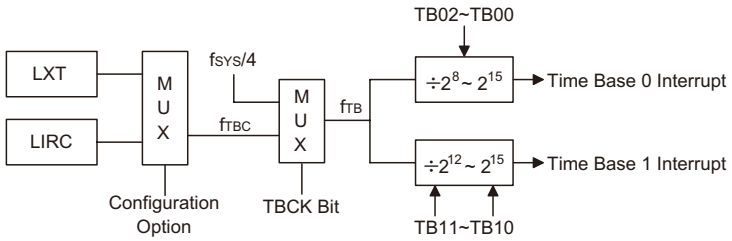
Bit 7 **TBON:** TB0 and TB1 Control
0: Disable
1: Enable

Bit 6 **TBCK:** Select f_{TB} Clock
0: f_{TBC}
1: $f_{SYS}/4$

Bit 5~4 **TB11~TB10:** Select Time Base 1 Time-out Period
00: $4096/f_{TB}$
01: $8192/f_{TB}$
10: $16384/f_{TB}$
11: $32768/f_{TB}$

Bit 3 **LXTLP:** LXT Low Power Control
0: Disable
1: Enable

Bit 2~0 **TB02~TB00:** Select Time Base 0 Time-out Period
000: $256/f_{TB}$
001: $512/f_{TB}$
010: $1024/f_{TB}$
011: $2048/f_{TB}$
100: $4096/f_{TB}$
101: $8192/f_{TB}$
110: $16384/f_{TB}$
111: $32768/f_{TB}$



Time Base Interrupts

Serial Interface Module Interrupts – SIM Interrupt

The Serial Interface Module Interrupt, also known as the SIM interrupt, will take place when the SIM Interrupt request flag, SIMF, is set, which occurs when a byte of data has been received or transmitted by the SIM interface. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and the Serial Interface Interrupt enable bit, SIME, must first be set. When the interrupt is enabled, the stack is not full and a byte of data has been transmitted or received by the SIM interface, a subroutine call to the respective Interrupt vector, will take place. When the interrupt is serviced, the Serial Interface Interrupt flag, SIMF, will be automatically cleared. The EMI bit will also be automatically cleared to disable other interrupts.

Serial Peripheral Interface Interrupt – SPIA Interrupt

The Serial Peripheral Interface Interrupt, also known as the SPIA interrupt, will take place when the SPIA Interrupt request flag, SPIAF, is set, which occurs when a byte of data has been received or transmitted by the SPIA interface. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, and the Serial Interface Interrupt enable bit, SPIAE, must first be set. When the interrupt is enabled, the stack is not full and a byte of data has been transmitted or received by the SPIA interface, a subroutine call to the respective Interrupt vector, will take place. When the interrupt is serviced, the Serial Interface Interrupt flag, SPIAF, will be automatically cleared. The EMI bit will also be automatically cleared to disable other interrupts.

LVD Interrupt

The Low Voltage Detector Interrupt is contained within the Multi-function Interrupt. An LVD Interrupt request will take place when the LVD Interrupt request flag, LVF, is set, which occurs when the Low Voltage Detector function detects a low power supply voltage. To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, Low Voltage Interrupt enable bit, LVE, and associated Multi-function interrupt enable bit, must first be set. When the interrupt is enabled, the stack is not full and a low voltage condition occurs, a subroutine call to the Multi-function Interrupt vector, will take place. When the Low Voltage Interrupt is serviced, the EMI bit will be automatically cleared to disable other interrupts, however only the Multi-function interrupt request flag will be also automatically cleared. As the LVF flag will not be automatically cleared, it has to be cleared by the application program.

TM Interrupts

The Compact and Standard Type TMs have two interrupts each. All of the TM interrupts are contained within the Multi-function Interrupts. For each of the Compact and Standard Type TMs there are two interrupt request flags TnPF and TnAF and two enable bits TnPE and TnAE. A TM interrupt request will take place when any of the TM request flags are set, a situation which occurs when a TM comparator P or A match situation happens.

To allow the program to branch to its respective interrupt vector address, the global interrupt enable bit, EMI, respective TM Interrupt enable bit, and relevant Multi-function Interrupt enable bit, MFnE, must first be set. When the interrupt is enabled, the stack is not full and a TM comparator match situation occurs, a subroutine call to the relevant Multi-function Interrupt vector locations, will take place. When the TM interrupt is serviced, the EMI bit will be automatically cleared to disable other interrupts, however only the related MFnF flag will be automatically cleared. As the TM interrupt request flags will not be automatically cleared, they have to be cleared by the application program.

Interrupt Wake-up Function

Each of the interrupt functions has the capability of waking up the microcontroller when in the SLEEP or IDLE Mode. A wake-up is generated when an interrupt request flag changes from low to high and is independent of whether the interrupt is enabled or not. Therefore, even though the device is in the SLEEP or IDLE Mode and its system oscillator stopped, situations such as external edge transitions on the external interrupt pins, a low power supply voltage or comparator input change may cause their respective interrupt flag to be set high and consequently generate an interrupt. Care must therefore be taken if spurious wake-up situations are to be avoided. If an interrupt wake-up function is to be disabled then the corresponding interrupt request flag should be set high before the device enters the SLEEP or IDLE Mode. The interrupt enable bits have no effect on the interrupt wake-up function.

Programming Considerations

By disabling the relevant interrupt enable bits, a requested interrupt can be prevented from being serviced, however, once an interrupt request flag is set, it will remain in this condition in the interrupt register until the corresponding interrupt is serviced or until the request flag is cleared by the application program.

Where a certain interrupt is contained within a Multi-function interrupt, then when the interrupt service routine is executed, as only the Multi-function interrupt request flags, MF0F~MF4F, will be automatically cleared, the individual request flag for the function needs to be cleared by the application program.

It is recommended that programs do not use the "CALL" instruction within the interrupt service subroutine. Interrupts often occur in an unpredictable manner or need to be serviced immediately. If only one stack is left and the interrupt is not well controlled, the original control sequence will be damaged once a CALL subroutine is executed in the interrupt subroutine.

Every interrupt has the capability of waking up the microcontroller when it is in the SLEEP or IDLE Mode, the wake up being generated when the interrupt request flag changes from low to high. If it is required to prevent a certain interrupt from waking up the microcontroller then its respective request flag should be first set high before enter SLEEP or IDLE Mode.

As only the Program Counter is pushed onto the stack, then when the interrupt is serviced, if the contents of the accumulator, status register or other registers are altered by the interrupt service program, their contents should be saved to the memory at the beginning of the interrupt service routine.

To return from an interrupt subroutine, either a RET or RETI instruction may be executed. The RETI instruction in addition to executing a return to the main program also automatically sets the EMI bit high to allow further interrupts. The RET instruction however only executes a return to the main program leaving the EMI bit in its present zero state and therefore disabling the execution of further interrupts.

Low Voltage Detector – LVD

Each device has a Low Voltage Detector function, also known as LVD. This enabled the device to monitor the power supply voltage, V_{DD}, and provide a warning signal should it fall below a certain level. This function may be especially useful in battery applications where the supply voltage will gradually reduce as the battery ages, as it allows an early warning battery low signal to be generated. The Low Voltage Detector also has the capability of generating an interrupt signal.

LVD Register

The Low Voltage Detector function is controlled using a single register with the name LVDC. Three bits in this register, VLVD2~VLVD0, are used to select one of eight fixed voltages below which a low voltage condition will be determined. A low voltage condition is indicated when the LVDO bit is set. If the LVDO bit is low, this indicates that the V_{DD} voltage is above the preset low voltage value. The LVDEN bit is used to control the overall on/off function of the low voltage detector. Setting the bit high will enable the low voltage detector. Clearing the bit to zero will switch off the internal low voltage detector circuits. As the low voltage detector will consume a certain amount of power, it may be desirable to switch off the circuit when not in use, an important consideration in power sensitive battery powered applications.

LVDC Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	LVDO	LVDEN	—	VLVD2	VLVD1	VLVD0
R/W	R	R	R	R/W	R	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 Unimplemented

Bit 5 **LVDO:** LVD Output Flag
0: No Low Voltage Detect
1: Low Voltage Detect

Bit 4 **LVDEN:** Low Voltage Detector Control
0: Disable
1: Enable

Bit 3 Unimplemented

Bit 2~0 **VLVD2~VLVD0:** Select LVD Voltage
000: 2.0V
001: 2.2V
010: 2.4V
011: 2.7V
100: 3.0V
101: 3.3V
110: 3.6V
111: 4.0V

LVD Operation

The Low Voltage Detector function operates by comparing the power supply voltage, V_{DD}, with a pre-specified voltage level stored in the LVDC register. This has a range of between 2.0V and 4.0V. When the power supply voltage, V_{DD}, falls below this pre-determined value, the LVDO bit will be set high indicating a low power supply voltage condition. The Low Voltage Detector function is supplied by a reference voltage which will be automatically enabled. When the device is powered down the low voltage detector will remain active if the LVDEN bit is high. After enabling the Low Voltage Detector, a time delay t_{LVDS} should be allowed for the circuitry to stabilise before reading the LVDO bit. Note also that as the V_{DD} voltage may rise and fall rather slowly, at the voltage nears that of V_{LVD}, there may be multiple bit LVDO transitions.

The Low Voltage Detector also has its own interrupt which is contained within one of the Multi-function interrupts, providing an alternative means of low voltage detection, in addition to polling the LVDO bit. The interrupt will only be generated after a delay of t_{LVD} after the LVDO bit has been set high by a low voltage condition. When the device is powered down the Low Voltage Detector will remain active if the LVDEN bit is high. In this case, the LVF interrupt request flag will be set, causing an interrupt to be generated if V_{DD} falls below the preset LVD voltage. This will cause the device to wake-up from the SLEEP or IDLE Mode, however if the Low Voltage Detector wake up function is not required then the LVF flag should be first set high before the device enters the SLEEP or IDLE Mode.

USB Interface

The USB interface is a 4-wire serial bus that allows communication between a host device and up to 127 max peripheral devices on the same bus. A token based protocol method is used by the host device for communication control. Other advantages of the USB bus include live plugging and unplugging and dynamic device configuration. As the complexity of USB data protocol does not permit comprehensive USB operation information to be provided in this datasheet, the reader should therefore consult other external information for a detailed USB understanding.

The devices include a USB interface function allowing for the convenient design of USB peripheral products.

The USB disable/enable control bit “USBdis” is in the SYSC Register. If the USB is disabled, then V33O will be floating, the UDP/UDN lines will become I/O functions, and the USB SIE will be disabled.

Power Plane

There are three power planes for HT66FB540/HT66FB550/HT66FB560: USB SIE VDD, VDDIO and the MCU VDD.

For the USB SIE VDD will supply all circuits related to USB SIE and be sourced from pin “UBUS”. Once the USB is removed from the USB and there is no power in the USB BUS, the USB SIE circuit is no longer operational.

For the PA port, it can be configured using the PAPS1 and PAPS0 registers to define the pins PA0~PA7 are supplied by either the MCU VDD, the V33O or the power pin VDDIO.

The PE0 is pin-shared with VDDIO and VREF pins .The VDDIO function can be selected by configuration option and the VREF function can be selected by the VREFS bit in the ADCR1 register. However, the ADREF has the highest priority. If the VREF function has been selected, the PE0 pin function will be disabled as well the VDDIO function, even though the VDDIO is selected.

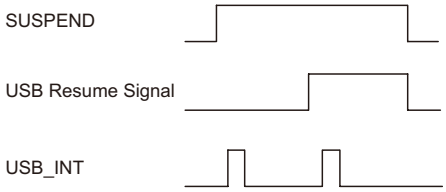
For the MCU VDD, it supplies all the HT66FB540/HT66FB550/HT66FB560 circuits except the USB SIE which is supply by UBUS.

The PE1 is pin shared with UBUS pin and it's "input" only.

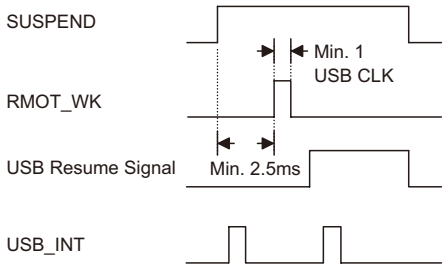
USB Suspend Wake-Up Remote Wake-Up

If there is no signal on the USB bus for over 3ms, the devices will go into a suspend mode. The Suspend flag, SUSP, in the USC register, will then be set high and an USB interrupt will be generated to indicate that the devices should jump to the suspend state to meet the requirements of the USB suspend current spec. In order to meet the requirements of the suspend current, the firmware should disable the USB clock by clearing the USBCKEN bit to "0".

The suspend current can be further decreased by setting the SUSP2 bit in the UCC register. When the resume signal is sent out by the host, the devices will be woken up the by the USB interrupt and the Resume bit in the USC register will be set. To ensure correct device operation, the program must set the USBCKEN bit in the UCC register high and clear the SUSP2 bit in the UCC register. The Resume signal will be cleared before the Idle signal is sent out by the host and the Suspend line in the USC register will change to zero. So when the MCU detects the Suspend bit in the USC register, the condition of the Resume line should be noted and taken into consideration.



The devices have a remote wake up function which can wake-up the USB Host by sending a wake-up pulse through RMWK in the USC register. Once the USB Host receives a wake-up signal from the device it will send a Resume signal to the devices.



USB Interface Operation

The HT66FB540, HT66FB550 and HT66FB560 have 4 Endpoints (EP0~EP3), 6 Endpoints (EP0~EP5), and 8 Endpoints (EP0~EP7) respectively. The EP0 supports Control transfer. All EP1~EP7 support Interrupt or Bulk transfer.

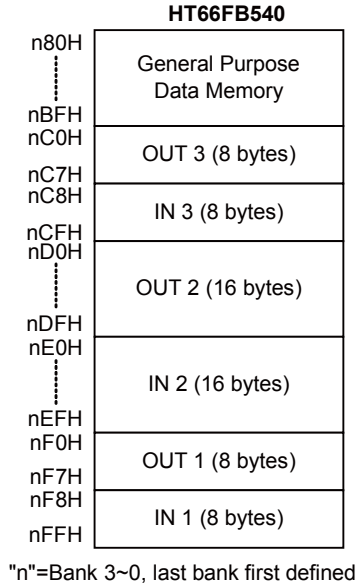
All endpoints except EP0 can be configure as 8, 16, 32, 64 FIFO size by the register UFC0 and UFC1. EP0 has 8-byte FIFO size.

The Total FIFO size is 384+8 bytes for the HT66FB540, 640+8 bytes for the HT66FB550 and 896+8 bytes for the HT66FB560.

As the USB FIFO is assigned from the last bank of the Data RAM and has a start address of 0FFH to the upper address, dependent on the FIFO size, if the corresponding data RAM bank is used for both general purpose RAM and the USB FIFO, special care should be taken that the RAM EQU definition should not overlap with the USB FIFO RAM address.

The URD in the USC register is the USB reset signal control function definition bit.

The USB FIFO size definition for IN/OUT control depends on the UFC, UFIEN and UFOEN registers. If OUT 1 not used, then the OUT 1 FIFO will not be defined and IN 2 will be defined as IN 1 afterwards.



USB FIFO Size Define

USB Interface Registers

The USB interface has a series of registers associated with its operation.

SYSC Register

Bit	7	6	5	4	3	2	1	0
Name	CLK_ADJ	USBdis	RUBUS	—	—	HFV	—	—
R/W	R/W	R/W	R/W	—	—	R/W	—	—
POR	0	0	0	—	—	0	—	—

Bit 7 **CLK_ADJ:** PLL Clock Automatic Adjustment function
PLL related control bit, described elsewhere

Bit 6 **USBdis:** USB SIE control bit
0: Enable
1: Disable

Bit 5 **RUBUS:** UBUS pin pull low resistor
0: Enable
1: Disable

Bit 4~3 "—": unimplemented, read as "0"

Bit 2 **HFV**: Non-USB mode high frequency voltage control
0: For USB mode - bit must be cleared to zero.
1: For non-USB mode - bit must be set high. Ensures that the higher frequency can work at lower voltages.
A higher frequency is >8MHz and is used for the system clock f_H.

Bit 1~0 "—": unimplemented, read as "0"

USB_STAT Register

Bit	7	6	5	4	3	2	1	0
Name	PS2_CKO	PS2_DAO	PS2_CKI	PS2_DAI	SE1	SE0	PU	ESD
R/W	W	W	R	R	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **PS2_CKO:** Output for driving UDP/GPIO pin, when work under 3D PS2 mouse function. Default value is “1”.

Bit 6 **PS2_DAO:** Output for driving UDN/GPIO pin, when work under 3D PS2 mouse function. Default value is “1”.

Bit 5 **PS2_CKI:** UDP/GPIO input

Bit 4 **PS2_DAI:** UDN/GPIO input

Bit 3 **SE1** : This bit is used to indicate the SIE has detected a SE1 noise in the USB bus.
This bit is set by SIE and clear by F/W.

Bit 2 **SE0** : This bit is used to indicate the SIE has detected a SE0 noise in the USB bus.
This bit is set by SIE and clear by F/W.

Bit 1 **PU:**
Bit1=1, UDP and UDN have a 600kΩ pull-high
Bit1=0, no pull-high (default on MCU reset)

Bit 0 This bit will set to “1” when there is ESD issue.
This bit is set by SIE and cleared by F/W.

UINT Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	EP3EN	EP2EN	EP1EN	EP0EN
R/W	R	R	R	R	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~4 Unimplemented

Bit 3 **EP3EN:** USB endpoint3 interrupt control bit.
0: Disable
1: Enable

Bit 2 **EP2EN:** USB endpoint2 interrupt control bit.
0: Disable
1: Enable

Bit 1 **EP1EN:** USB endpoint1 interrupt control bit.
0: Disable
1: Enable

Bit 0 **EP0EN:** USB endpoint0 interrupt control bit.
0: Disable
1: Enable

- **HT66FB550**

Bit	7	6	5	4	3	2	1	0
Name	—	—	EP5EN	EP4EN	EP3EN	EP2EN	EP1EN	EP0EN
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 Unimplemented

Bit 5 **EP5EN:** USB endpoint5 interrupt control bit
0: Disable
1: Enable

Bit 4 **EP4EN:** USB endpoint4 interrupt control bit
0: Disable
1: Enable

Bit 3 **EP3EN:** USB endpoint3 interrupt control bit
0: Disable
1: Enable

Bit 2 **EP2EN:** USB endpoint2 interrupt control bit
0: Disable
1: Enable

Bit 1 **EP1EN:** USB endpoint1 interrupt control bit
0: Disable
1: Enable

Bit 0 **EP0EN:** USB endpoint0 interrupt control bit
0: Disable
1: Enable

- **HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	EP7EN	EP6EN	EP5EN	EP4EN	EP3EN	EP2EN	EP1EN	EP0EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **EP7EN:** USB endpoint7 interrupt control bit
0: Disable
1: Enable

Bit 6 **EP6EN:** USB endpoint6 interrupt control bit
0: Disable
1: Enable

Bit 5 **EP5EN:** USB endpoint5 interrupt control bit
0: Disable
1: Enable

Bit 4 **EP4EN:** USB endpoint4 interrupt control bit
0: Disable
1: Enable

Bit 3 **EP3EN:** USB endpoint3 interrupt control bit
0: Disable
1: Enable

Bit 2 **EP2EN:** USB endpoint2 interrupt control bit
0: Disable
1: Enable

Bit 1 **EP1EN:** USB endpoint1 interrupt control bit
0: Disable
1: Enable

Bit 0 **EP0EN:** USB endpoint0 interrupt control bit
0: Disable
1: Enable

USC Register

Bit	7	6	5	4	3	2	1	0
Name	URD	SELPS2	PLL	SELUSB	RESUME	URST	RMWK	SUSP
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R
POR	1	0	0	0	0	0	0	0

Bit 7 **URD:** USB reset signal control function definition
0: USB reset signal cannot MCU
1: USB reset signal will reset MCU

Bit 6 **SELPS2:** PS2 mode select bit
0: Not PS2 mode
1: PS2 mode
When the SELPS2 bit is set high, the PS2 function is selected and the pin-shared pins, UDN/GPIO0 and UDP/GPIO1, will become the GPIO0 and GPIO1 general purpose I/O functions which can be used to be the DATA and CLK pins for the PS2.

Bit 5 **PLL:** PLL control bit
0: Turn-on PLL
1: Turn-off PLL

Bit 4 **SELUSB:** USB mode and V33O on/off select bit
0: Not USB mode, Turn-off V33O
1: USB mode, Turn-on V33O
When the SELUSB bit is set high, the USB and V33O functions are selected and the pin-share pins, UDN/GPIO0 and UDP/GPIO1, will become the UDN and UDP pins for the USB.

Bit 3 **RESUME:** USB resume indication bit
0: SUSP bit goes to "0"
1: Leave the suspend mode
When the USB leaves the suspend mode, this bit is set to "1" (set by SIE). When the RESUME is set by SIE, an interrupt will be generated to wake-up the MCU. In order to detect the suspend state, the MCU should set USBCKEN and clear SUSP2 (in the UCC register) to enable the SIE detect function. RESUME will be cleared when the SUSP goes to "0". When the MCU is detecting the SUSP, the condition of RESUME (causes the MCU to wake-up) should be noted and taken into consideration.

Bit 2 **URST:** USB reset indication bit
0: No USB reset
1: USB reset occurred
This bit is set/cleared by the USB SIE. This bit is used to detect a USB reset event on the USB bus. When this bit is set to "1", this indicates that a USB reset has occurred and that a USB interrupt will be initialized.

Bit 1 **RMWK:** USB remote wake-up command
0: No remote wake-up
1: Remote wake-up
It is set by MCU to leave the USB host leaving the suspend mode. Indicate that the This bit is set to produce a high pulse width of 4μs to indicate that the USB host has left the suspend mode.

Bit 0 **SUSP:** USB suspend indication
0: Not in the suspend mode
1: Enter the suspend mode
When this bit is set to 1 (set by SIE), it indicates that the USB bus has entered the suspend mode. The USB interrupt is also triggered when this bit changes from low to high.

SELUSB	SELPS2	USB and PS2 mode description
0	0	1. No mode supported 2. V33O pin not output and it will floating 3. UDN/GPIO0 and UDP/GPIO1 pins cann't output
0	1	1. PS2 mode 2. V33O pin output VDD 3. UDN/GPIO0 and UDP/GPIO1 pins will become the GPIO0 and GPIO1 pins, which can output by firmware
1	x	1. USB mode 2. V33O output 3.3V 3. UDN/GPIO0 and UDP/GPIO1 pins will become the UDN and UDP pins

x: don't care

USR Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	EP3F	EP2F	EP1F	EP0F
R/W	R	R	R	R	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~4 Unimplemented

Bit 3 **EP3F:** Endpoint 3 accessed detection
0: Not accessed
1: Accessed

Bit 2 **EP2F:** Endpoint 2 accessed detection
0: Not accessed
1: Accessed

Bit 1 **EP1F:** Endpoint 1 accessed detection
0: Not accessed
1: Accessed

Bit 0 **EP0F:** Endpoint 0 accessed detection
0: Not accessed
1: Accessed

- **HT66FB550**

Bit	7	6	5	4	3	2	1	0
Name	—	—	EP5F	EP4F	EP3F	EP2F	EP1F	EP0F
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 Unimplemented

Bit 5 **EP5F:** Endpoint 5 accessed detection
0: Not accessed
1: Accessed

Bit 4 **EP4F:** Endpoint 4 accessed detection
0: Not accessed
1: Accessed

Bit 3 **EP3F:** Endpoint 3 accessed detection
0: Not accessed
1: Accessed

Bit 2 **EP2F:** Endpoint 2 accessed detection
0: Not accessed
1: Accessed

Bit 1 **EP1F:** Endpoint 1 accessed detection
0: Not accessed
1: Accessed

Bit 0 **EP0F:** Endpoint 0 accessed detection
0: Not accessed
1: Accessed

- **HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	EP7F	EP6F	EP5F	EP4F	EP3F	EP2F	EP1F	EP0F
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **EP7F:** Endpoint 7 accessed detection
0: Not accessed
1: Accessed

Bit 6 **EP6F:** Endpoint 6 accessed detection
0: Not accessed
1: Accessed

Bit 5 **EP5F:** Endpoint 5 accessed detection
0: Not accessed
1: Accessed

Bit 4 **EP4F:** Endpoint 4 accessed detection
0: Not accessed
1: Accessed

Bit 3 **EP3F:** Endpoint 3 accessed detection
0: Not accessed
1: Accessed

Bit 2 **EP2F:** Endpoint 2 accessed detection
0: Not accessed
1: Accessed

Bit 1 **EP1F:** Endpoint 1 accessed detection
0: Not accessed
1: Accessed

Bit 0 **EP0F:** Endpoint 0 accessed detection
0: Not accessed
1: Accessed

UCC Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	Rctrl	SYSCLK	Fsys16MHZ	SUSP2	USBCKEN	—	EPS1	EPS0
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **Rctrl:** 7.5kΩ resistor between UDP and Ubus control bit
0: No 7.5kΩ resistor between UDP and Ubus
1: Has 7.5kΩ resistor between UDP and Ubus

Bit 6 **SYSCLK:** Specify MCU oscillator frequency indication bit
0: 12MHz crystal oscillator or resonator, clear this bit to "0"
1: 6MHz crystal oscillator or resonator, set this bit to "1"

Bit 5 **Fsys16MHZ:** MCU system clock source control bit
0: From OSC
1: From PLL output 16MHz

Bit 4 **SUSP2:** Reduce power consumption in suspend mode control bit
0: In normal mode
1: In halt mode, set this bit to "1" for reducing power consumption

Bit 3 **USBCKEN:** USB clock control bit
0: Disable
1: Enable

Bit 2 Unimplemented

Bit 1~0 **EPS1, EPS0:** Accessing endpoint FIFO selection
00: Select endpoint 0 FIFO (control)
01: Select endpoint 1 FIFO
10: Select endpoint 2 FIFO
11: Select endpoint 3 FIFO

- **HT66FB550**

Bit	7	6	5	4	3	2	1	0
Name	Rctrl	SYSCLK	Fsys16MHZ	SUSP2	USBCKEN	EPS2	EPS1	EPS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **Rctrl:** 7.5kΩ resistor between UDP and Ubus control bit
0: No 7.5kΩ resistor between UDP and Ubus
1: Has 7.5kΩ resistor between UDP and Ubus

Bit 6 **SYSCLK:** Specify MCU oscillator frequency indication bit
0: 12MHz crystal oscillator or resonator, clear this bit to "0"
1: 6MHz crystal oscillator or resonator, set this bit to "1"

Bit 5 **Fsys16MHZ:** MCU system clock source control bit
0: From OSC
1: From PLL output 16MHz

Bit 4 **SUSP2:** Reduce power consumption in suspend mode control bit
0: In normal mode
1: In halt mode, set this bit to "1" for reducing power consumption

Bit 3 **USBCKEN:** USB clock control bit
0: Disable
1: Enable

Bit 2~0 **EPS2, EPS1, EPS0:** Accessing endpoint FIFO selection
000: Select endpoint 0 FIFO (control)
001: Select endpoint 1 FIFO
010: Select endpoint 2 FIFO
011: Select endpoint 3 FIFO
100: Select endpoint 4 FIFO
101~111: Select endpoint 5 FIFO

• **HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	Rctrl	SYSCLK	Fsys16MHZ	SUSP2	USBCKEN	EPS2	EPS1	EPS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **Rctrl:** 7.5kΩ resistor between UDP and Ubus control bit
0: No 7.5kΩ resistor between UDP and Ubus
1: Has 7.5kΩ resistor between UDP and Ubus

Bit 6 **SYSCLK:** Specify MCU oscillator frequency indication bit
0: 12MHz crystal oscillator or resonator, clear this bit to "0"
1: 6MHz crystal oscillator or resonator, set this bit to "1"

Bit 5 **Fsys16MHZ:** MCU system clock source control bit
0: From OSC
1: From PLL output 16MHz

Bit 4 **SUSP2:** Reduce power consumption in suspend mode control bit
0: In normal mode
1: In halt mode, set this bit to "1" for reducing power consumption

Bit 3 **USBCKEN:** USB clock control bit
0: Disable
1: Enable

Bit 2~0 **EPS2, EPS1, EPS0:** Accessing endpoint FIFO selection
000: Select endpoint 0 FIFO (control)
001: Select endpoint 1 FIFO
010: Select endpoint 2 FIFO
011: Select endpoint 3 FIFO
100: Select endpoint 4 FIFO
101: Select endpoint 5 FIFO
110: Select endpoint 6 FIFO
111: Select endpoint 7 FIFO

AWR Register

Bit	7	6	5	4	3	2	1	0
Name	AD6	AD5	AD4	AD3	AD2	AD1	AD0	WKEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~1 **AD6~AD0:** USB device address

Bit 0 **WKEN:** USB remote-wake-up control bit
0: Disable
1: Enable

The AWR register contains the current address and a remote wake up function control bit. The initial value of AWR is "00H". The address value extracted from the USB command has not to be loaded into this register until the SETUP stage has finished.

STLO Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	STLO3	STLO2	STLO1	STLO0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~4 Unimplemented

Bit 3~0 **STLO3~STLO0:** FIFO OUT stall endpoints indication bits
0: Not stall
1: Stall

The STALL register shows if the corresponding endpoint has worked properly or not. As soon as endpoint improper operation occurs, the related bit in the STALL register has to be set high. The STALL register bits will be cleared by a USB reset signal and a setup token event.

- **HT66FB550**

Bit	7	6	5	4	3	2	1	0
Name	—	—	STLO5	STLO4	STLO3	STLO2	STLO1	STLO0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 Unimplemented

Bit 5~0 **STLO5~STLO0:** FIFO OUT stall endpoints indication bits
0: Not stall
1: Stall

The STALL register shows if the corresponding endpoint has worked properly or not. As soon as endpoint improper operation occurs, the related bit in the STALL register has to be set high. The STALL register bits will be cleared by a USB reset signal and a setup token event.

- **HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	STLO7	STLO6	STLO5	STLO4	STLO3	STLO2	STLO1	STLO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **STLO7~STLO0:** FIFO OUT stall endpoints indication bits
0: Not stall
1: Stall
The STALL register shows if the corresponding endpoint has worked properly or not. As soon as endpoint improper operation occurs, the related bit in the STALL register has to be set high. The STALL register bits will be cleared by a USB reset signal and a setup token event.

STLI Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	STLI3	STLI2	STLI1	STLI0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~4 Unimplemented

Bit 3~0 **STLI3~STLI0:** FIFO IN stall endpoints indication bits
0: Not stall
1: Stall
The STALL register shows if the corresponding endpoint has worked properly or not. As soon as endpoint improper operation occurs, the related bit in the STALL register has to be set high. The STALL register bits will be cleared by a USB reset signal and a setup token event.

- **HT66FB550**

Bit	7	6	5	4	3	2	1	0
Name	—	—	STLI5	STLI4	STLI3	STLI2	STLI1	STLI0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 Unimplemented

Bit 5~0 **STLI5~STLI0:** FIFO IN stall endpoints indication bits
0: Not stall
1: Stall
The STALL register shows if the corresponding endpoint has worked properly or not. As soon as endpoint improper operation occurs, the related bit in the STALL register has to be set high. The STALL register bits will be cleared by a USB reset signal and a setup token event.

- **HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	STLI7	STLI6	STLI5	STLI4	STLI3	STLI2	STLI1	STLI0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **STLI7~STLI0:** FIFO IN stall endpoints indication bits
0: Not stall
1: Stall
The STALL register shows if the corresponding endpoint has worked properly or not. As soon as endpoint improper operation occurs, the related bit in the STALL register has to be set high. The STALL register bits will be cleared by a USB reset signal and a setup token event.

SIES Register

Bit	7	6	5	4	3	2	1	0
Name	NMI	CRCF	—	NAK	IN	OUT	ERR	ASET
R/W	R/W	R/W	R	R	R	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **NMI:** NAK token interrupt mask flag
0: Interrupt enable
1: Interrupt disable
If this bit set, when the device sent a NAK token to the host, an interrupt will be disabled. Otherwise if this bit is cleared, when the device sends a NAK token to the host, it will enter the interrupt sub-routine. This bit is used for all endpoint.

Bit 6 **CRCF:** CRC error detection flag
0: No error
1: Error
This bit will be set to "1" when there are the following three conditions happened: CRC error, PID error, Bit stuffing error. This bit is set by SIE and cleared by F/W.

Bit 5 Unimplemented

Bit 4 **NAK:** ACK error detection flag
0: No error
1: Error
This bit will set to "1" once SIE discover there are some error condition so the SIE is not response (NAK or ACK or DATA) for the USB token. This bit is set by SIE and cleared by F/W.

Bit 3 **IN:** Current USB receiving signal indicator
0: Low
1: High
This bit is used to indicate the current USB receiving signal from PC host is IN token.

Bit 2 **OUT:** USB OUT token indicator
0: Low
1: High
This bit is used to indicate the OUT token (except the OUT zero length token) has been received. The firmware clears this bit after the OUT data has been read. Also, this bit will be cleared by SIE after the next valid SETUP token is received.

Bit 1 **ERR:** FIFO accessed error indicator
0: No error
1: Error
This bit is used to indicate that some errors have occurred when the FIFO is accessed. This bit is set by SIE and should be cleared by firmware. This bit is used for all endpoint.

Bit 0 **ASET:** device address updated method control bit
0: Update address after an written address to the AWR register
1: Update address after PC host read out data
This bit is used to configure the SIE to automatically change the device address by the value stored in the AWR register. When this bit is set to "1" by firmware, the SIE will update the device address by the value stored in the AWR register after the PC host has successfully read the data from he device by an IN operation. Otherwise, when this bit is cleared to "0", the SIE will update the device address immediately after an address is written to the AWR register. So, in order to work properly, the firmware has to clear this bit after a next valid SETUP token is received.

MISC Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	LEN0	READY	SETCMD	—	E3IDF	CLEAR	TX	REQUEST
R/W	R	R	R/W	R	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **LEN0:** 0-sized packet indication flag
0: Not 0-sized packet
1: 0-sized packet
This bit is used to show that the host sent a 0-sized packet to the MCU. This bit must be cleared by a read action to the corresponding FIFO.

Bit 6 **READY:** Desired FIFO ready indication flag
0: Not ready
1: Ready

Bit 5 **SETCMD:** Setup command indication flag
0: Not setup command
1: Setup command
This bit is used to show that the data in the FIFO is a setup command. This bit is set by Hardware and cleared by Firmware.

Bit 4 Unimplemented

Bit 3 **E3IDF:** endpoint 3 input FIFO selection
0: Single buffer
1: Double buffer

Bit 2 **CLEAR:** Clear FIFO function control bit
0: Disable
1: Enable
MCU requests to clear the FIFO, even if the FIFO is not ready. After clearing the FIFO, the USB interface will send force_tx_err to tell the Host that data under-run if the Host wants to read data.

Bit 1 **TX:** data writing to FIFO status indication flag
0: Data writing finished
1: Data writing to FIFO
To represent the direction and transition end MCU access. When set to logic 1, the MCU desires to write data to the FIFO. After finishing, this bit must be set to logic 0 before terminating request to represent transition end. For an MCU read operation, this bit must be set to logic 0 and set to logic 1 after finishing.

Bit 0 **REQUEST:** Desired FIFO request status indication flag
0: No request
1: Request
After setting the status of the desired one, FIFO can be requested by setting this bit high. After finishing, this bit must be set low.

- **HT66FB550/HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	LEN0	READY	SETCMD	E4ODF	E3IDF	CLEAR	TX	REQUEST
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **LEN0:** 0-sized packet indication flag
0: Not 0-sized packet
1: 0-sized packet
This bit is used to show that the host sent a 0-sized packet to the MCU. This bit must be cleared by a read action to the corresponding FIFO.

Bit 6 **READY:** Desired FIFO ready indication flag
0: Not ready
1: Ready

Bit 5 **SETCMD:** Setup command indication flag
0: Not setup command
1: Setup command
This bit is used to show that the data in the FIFO is a setup command. This bit is set by Hardware and cleared by Firmware.

Bit 4 **E4ODF:** endpoint 4 output FIFO selection
0: Single buffer
1: Double buffer

Bit 3 **E3IDF:** endpoint 3 input FIFO selection
0: Single buffer
1: Double buffer

Bit 2 **CLEAR:** Clear FIFO function control bit
0: Disable
1: Enable
MCU requests to clear the FIFO, even if the FIFO is not ready. After clearing the FIFO, the USB interface will send force_tx_err to tell the Host that data under-run if the Host wants to read data.

Bit 1 **TX:** data writing to FIFO status indication flag
0: Data writing finished
1: Data writing to FIFO
To represent the direction and transition end MCU access. When set to logic 1, the MCU desires to write data to the FIFO. After finishing, this bit must be set to logic 0 before terminating request to represent transition end. For an MCU read operation, this bit must be set to logic 0 and set to logic 1 after finishing.

Bit 0 **REQUEST:** Desired FIFO request status indication flag
0: No request
1: Request
After setting the status of the desired one, FIFO can be requested by setting this bit high. After finishing, this bit must be set low.

UFOEN Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	SETO3	SETO2	SETO1	DATATG
R/W	R	R	R	R	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~4 Unimplemented

Bit 3 **SETO3:** EP3 output FIFO control bit
0: Disable
1: Enable

Bit 2 **SETO2:** EP2 output FIFO control bit
0: Disable
1: Enable

Bit 1 **SETO1:** EP1 output FIFO control bit
0: Disable
1: Enable

Bit 0 **DATATG:** DATA token toggle bit
0: Low
1: High

- **HT66FB550**

Bit	7	6	5	4	3	2	1	0
Name	—	—	SETO5	SETO4	SETO3	SETO2	SETO1	DATATG
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 Unimplemented

Bit 5 **SETO5:** EP5 output FIFO control bit
0: Disable
1: Enable

Bit 4 **SETO4:** EP4 output FIFO control bit
0: Disable
1: Enable

Bit 3 **SETO3:** EP3 output FIFO control bit
0: Disable
1: Enable

Bit 2 **SETO2:** EP2 output FIFO control bit
0: Disable
1: Enable

Bit 1 **SETO1:** EP1 output FIFO control bit
0: Disable
1: Enable

Bit 0 **DATATG:** DATA token toggle bit
0: Low
1: High

• **HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	SETO7	SETO6	SETO5	SETO4	SETO3	SETO2	SETO1	DATATG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **SETO7:** EP7 output FIFO control bit
0: Disable
1: Enable

Bit 6 **SETO6:** EP6 output FIFO control bit
0: Disable
1: Enable

Bit 5 **SETO5:** EP5 output FIFO control bit
0: Disable
1: Enable

Bit 4 **SETO4:** EP4 output FIFO control bit
0: Disable
1: Enable

Bit 3 **SETO3:** EP3 output FIFO control bit
0: Disable
1: Enable

Bit 2 **SETO2:** EP2 output FIFO control bit
0: Disable
1: Enable

Bit 1 **SETO1:** EP1 output FIFO control bit
0: Disable
1: Enable

Bit 0 **DATATG:** DATA token toggle bit
0: Low
1: High

UFIEN Register

- **HT66FB540**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	SETI3	SETI2	SETI1	FIFO_def
R/W	R	R	R	R	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~4 Unimplemented

Bit 3 **SETI3:** EP3 input FIFO control bit
0: Disable
1: Enable

Bit 2 **SETI2:** EP2 input FIFO control bit
0: Disable
1: Enable

Bit 1 **SETI1:** EP1 input FIFO control bit
0: Disable
1: Enable

Bit 0 **FIFO_def:** FIFO configuration redefined control bit
0: Disable
1: Enable
If this bit is set to "1", the SIE should redefine the FIFO configuration. This bit will be automatically cleared by SIE.

- **HT66FB550**

Bit	7	6	5	4	3	2	1	0
Name	—	—	SETI5	SETI4	SETI3	SETI2	SETI1	FIFO_def
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 Unimplemented

Bit 5 **SETI5:** EP5 input FIFO control bit
0: Disable
1: Enable

Bit 4 **SETI4:** EP4 input FIFO control bit
0: Disable
1: Enable

Bit 3 **SETI3:** EP3 input FIFO control bit
0: Disable
1: Enable

Bit 2 **SETI2:** EP2 input FIFO control bit
0: Disable
1: Enable

Bit 1 **SETI1:** EP1 input FIFO control bit
0: Disable
1: Enable

Bit 0 **FIFO_def:** FIFO configuration redefined control bit
0: Disable
1: Enable
If this bit is set to "1", the SIE should redefine the FIFO configuration. This bit will be automatically cleared by SIE.

- **HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	SETI7	SETI6	SETI5	SETI4	SETI3	SETI2	SETI1	FIFO_def
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **SETI7:** EP7 input FIFO control bit
0: Disable
1: Enable

Bit 6 **SETI6:** EP6 input FIFO control bit
0: Disable
1: Enable

Bit 5 **SETI5:** EP5 input FIFO control bit
0: Disable
1: Enable

Bit 4 **SETI4:** EP4 input FIFO control bit
0: Disable
1: Enable

Bit 3 **SETI3:** EP3 input FIFO control bit
0: Disable
1: Enable

Bit 2 **SETI2:** EP2 input FIFO control bit
0: Disable
1: Enable

Bit 1 **SETI1:** EP1 input FIFO control bit
0: Disable
1: Enable

Bit 0 **FIFO_def:** FIFO configuration redefined control bit
0: Disable
1: Enable
If this bit is set to "1", the SIE should redefine the FIFO configuration. This bit will be automatically cleared by SIE.

UFC0 Register

Bit	7	6	5	4	3	2	1	0
Name	E3FS1	E3FS0	E2FS1	E2FS0	E1FS1	E1FS0	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R
POR	0	0	0	0	0	0	0	0

Bit 7, 6 **E3FS1, E3SF0:** endpoint 3 FIFO size selection
00: 8-byte
01: 16-byte
10: 32-byte
11: 64-byte

Bit 5, 4 **E2FS1, E2SF0:** endpoint 2 FIFO size selection
00: 8-byte
01: 16-byte
10: 32-byte
11: 64-byte

Bit 3, 2 **E1FS1, E1SF0:** endpoint 1 FIFO size selection
00: 8-byte
01: 16-byte
10: 32-byte
11: 64-byte

Bit 1~0 Unimplemented

UFC1 Register

- **HT66FB550**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	E5FS1	E5FS0	E4FS1	E4FS0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~4 Unimplemented

Bit 3, 2 **E5FS1, E5SF0:** endpoint 5 FIFO size selection
00: 8-byte
01: 16-byte
10: 32-byte
11: 64-byte

Bit 1, 0 **E4FS1, E4SF0:** endpoint 4 FIFO size selection
00: 8-byte
01: 16-byte
10: 32-byte
11: 64-byte

- **HT66FB560**

Bit	7	6	5	4	3	2	1	0
Name	E7FS1	E7FS0	E6FS1	E6FS0	E5FS1	E5FS0	E4FS1	E4FS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7, 6 **E7FS1, E7SF0:** endpoint 7 FIFO size selection
00: 8-byte
01: 16-byte
10: 32-byte
11: 64-byte

Bit 5, 4 **E6FS1, E6SF0:** endpoint 6 FIFO size selection
00: 8-byte
01: 16-byte
10: 32-byte
11: 64-byte

Bit 3, 2 **E5FS1, E5SF0:** endpoint 5 FIFO size selection
00: 8-byte
01: 16-byte
10: 32-byte
11: 64-byte

Bit 1, 0 **E4FS1, E4SF0:** endpoint 4 FIFO size selection
00: 8-byte
01: 16-byte
10: 32-byte
11: 64-byte

USB endpoint accessing registers

- **HT66FB540**

Register Name	Bit							
	7	6	5	4	3	2	1	0
FIFO0	D7	D6	D5	D4	D3	D2	D1	D0
FIFO1	D7	D6	D5	D4	D3	D2	D1	D0
FIFO2	D7	D6	D5	D4	D3	D2	D1	D0
FIFO3	D7	D6	D5	D4	D3	D2	D1	D0

- **HT66FB550**

Register Name	Bit							
	7	6	5	4	3	2	1	0
FIFO0	D7	D6	D5	D4	D3	D2	D1	D0
FIFO1	D7	D6	D5	D4	D3	D2	D1	D0
FIFO2	D7	D6	D5	D4	D3	D2	D1	D0
FIFO3	D7	D6	D5	D4	D3	D2	D1	D0
FIFO4	D7	D6	D5	D4	D3	D2	D1	D0
FIFO5	D7	D6	D5	D4	D3	D2	D1	D0

- **HT66FB560**

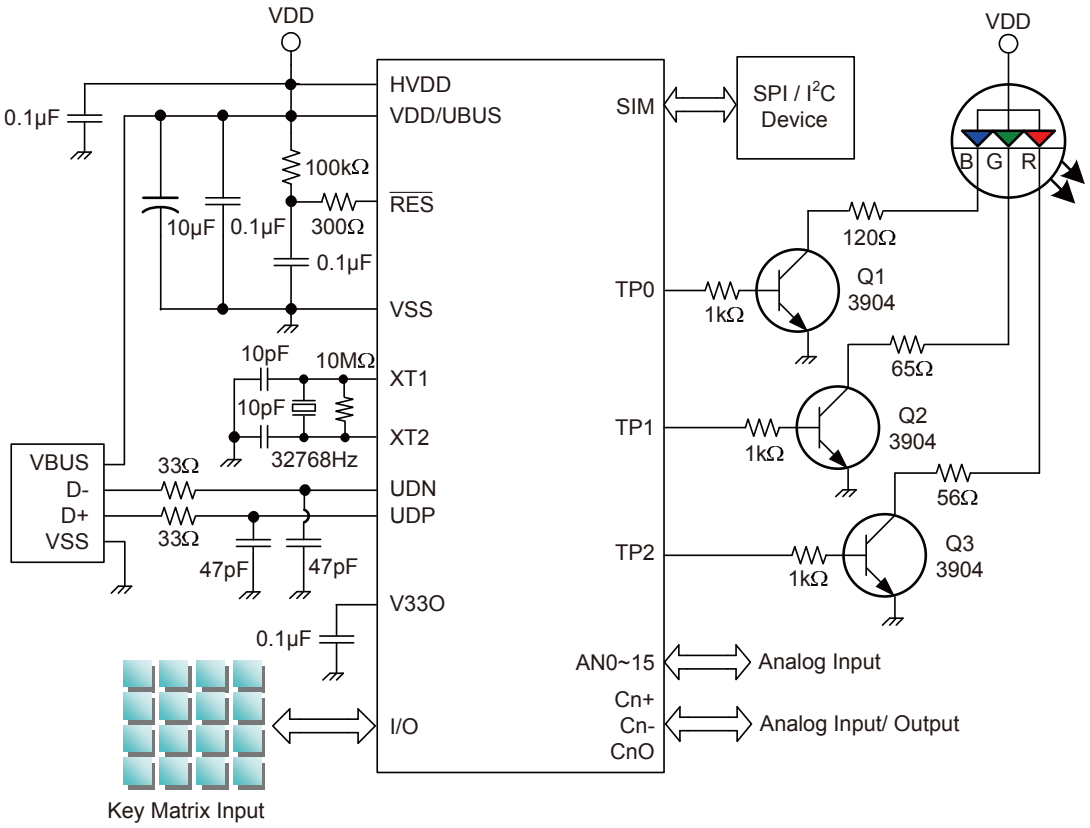
Register Name	Bit							
	7	6	5	4	3	2	1	0
FIFO0	D7	D6	D5	D4	D3	D2	D1	D0
FIFO1	D7	D6	D5	D4	D3	D2	D1	D0
FIFO2	D7	D6	D5	D4	D3	D2	D1	D0
FIFO3	D7	D6	D5	D4	D3	D2	D1	D0
FIFO4	D7	D6	D5	D4	D3	D2	D1	D0
FIFO5	D7	D6	D5	D4	D3	D2	D1	D0
FIFO6	D7	D6	D5	D4	D3	D2	D1	D0
FIFO7	D7	D6	D5	D4	D3	D2	D1	D0

Configuration Options

Configuration options refer to certain options within the MCU that are programmed into the devices during the programming process. During the development process, these options are selected using the HT-IDE software development tools. As these options are programmed into the devices using the hardware programming tools, once they are selected they cannot be changed later using the application program. All options must be defined for proper system function, the details of which are shown in the table.

No.	Options
Oscillator Options	
1	High Speed System Oscillator Selection – f_H: 1. HIRC (Default) 2. HXT
2	Low Speed System Oscillator Selection – f_L: 1. LIRC (Default) 2. LXT
3	f_{SUB} Clock Selection: 1. LIRC (Default) 2. LXT
4	Time Base Clock Selection – f_{TBC}: 1. LIRC (Default) 2. LXT
Crystal Mode Frequency Option	
5	Clock Mode frequency: 1. 12MHz 2. 6MHz
I/O or VDDIO Option	
6	I/O or VDDIO pin control bit: 1. VDDIO (Default) 2. I/O (PE0)

Application Circuits



Instruction Set

Introduction

Central to the successful operation of any microcontroller is its instruction set, which is a set of program instruction codes that directs the microcontroller to perform certain operations. In the case of Holtek microcontroller, a comprehensive and flexible set of over 60 instructions is provided to enable programmers to implement their application with the minimum of programming overheads.

For easier understanding of the various instruction codes, they have been subdivided into several functional groupings.

Instruction Timing

Most instructions are implemented within one instruction cycle. The exceptions to this are branch, call, or table read instructions where two instruction cycles are required. One instruction cycle is equal to 4 system clock cycles, therefore in the case of an 8MHz system oscillator, most instructions would be implemented within 0.5μs and branch or call instructions would be implemented within 1μs. Although instructions which require one more cycle to implement are generally limited to the JMP, CALL, RET, RETI and table read instructions, it is important to realize that any other instructions which involve manipulation of the Program Counter Low register or PCL will also take one more cycle to implement. As instructions which change the contents of the PCL will imply a direct jump to that new address, one more cycle will be required. Examples of such instructions would be “CLR PCL” or “MOV PCL, A”. For the case of skip instructions, it must be noted that if the result of the comparison involves a skip operation then this will also take one more cycle, if no skip is involved then only one cycle is required.

Moving and Transferring Data

The transfer of data within the microcontroller program is one of the most frequently used operations. Making use of three kinds of MOV instructions, data can be transferred from registers to the Accumulator and vice-versa as well as being able to move specific immediate data directly into the Accumulator. One of the most important data transfer applications is to receive data from the input ports and transfer data to the output ports.

Arithmetic Operations

The ability to perform certain arithmetic operations and data manipulation is a necessary feature of most microcontroller applications. Within the Holtek microcontroller instruction set are a range of add and subtract instruction mnemonics to enable the necessary arithmetic to be carried out. Care must be taken to ensure correct handling of carry and borrow data when results exceed 255 for addition and less than 0 for subtraction. The increment and decrement instructions INC, INCA, DEC and DECA provide a simple means of increasing or decreasing by a value of one of the values in the destination specified.

Logical and Rotate Operation

The standard logical operations such as AND, OR, XOR and CPL all have their own instruction within the Holtek microcontroller instruction set. As with the case of most instructions involving data manipulation, data must pass through the Accumulator which may involve additional programming steps. In all logical data operations, the zero flag may be set if the result of the operation is zero. Another form of logical data manipulation comes from the rotate instructions such as RR, RL, RRC and RLC which provide a simple means of rotating one bit right or left. Different rotate instructions exist depending on program requirements. Rotate instructions are useful for serial port programming applications where data can be rotated from an internal register into the Carry bit from where it can be examined and the necessary serial bit set high or low. Another application which rotate data operations are used is to implement multiplication and division calculations.

Branches and Control Transfer

Program branching takes the form of either jumps to specified locations using the JMP instruction or to a subroutine using the CALL instruction. They differ in the sense that in the case of a subroutine call, the program must return to the instruction immediately when the subroutine has been carried out. This is done by placing a return instruction "RET" in the subroutine which will cause the program to jump back to the address right after the CALL instruction. In the case of a JMP instruction, the program simply jumps to the desired location. There is no requirement to jump back to the original jumping off point as in the case of the CALL instruction. One special and extremely useful set of branch instructions are the conditional branches. Here a decision is first made regarding the condition of a certain data memory or individual bits. Depending upon the conditions, the program will continue with the next instruction or skip over it and jump to the following instruction. These instructions are the key to decision making and branching within the program perhaps determined by the condition of certain input switches or by the condition of internal data bits.

Bit Operations

The ability to provide single bit operations on Data Memory is an extremely flexible feature of all Holtek microcontrollers. This feature is especially useful for output port bit programming where individual bits or port pins can be directly set high or low using either the "SET [m].i" or "CLR [m].i" instructions respectively. The feature removes the need for programmers to first read the 8-bit output port, manipulate the input data to ensure that other bits are not changed and then output the port with the correct new data. This read-modify-write process is taken care of automatically when these bit operation instructions are used.

Table Read Operations

Data storage is normally implemented by using registers. However, when working with large amounts of fixed data, the volume involved often makes it inconvenient to store the fixed data in the Data Memory. To overcome this problem, Holtek microcontrollers allow an area of Program Memory to be setup as a table where data can be directly stored. A set of easy to use instructions provides the means by which this fixed data can be referenced and retrieved from the Program Memory.

Other Operations

In addition to the above functional instructions, a range of other instructions also exist such as the "HALT" instruction for Power-down operations and instructions to control the operation of the Watchdog Timer for reliable program operations under extreme electric or electromagnetic environments. For their relevant operations, refer to the functional related sections.

Instruction Set Summary

The following table depicts a summary of the instruction set categorised according to function and can be consulted as a basic instruction reference using the following listed conventions.

Table Conventions

x: Bits immediate data
m: Data Memory address
A: Accumulator
i: 0~7 number of bits
addr: Program memory address

Mnemonic	Description	Cycles	Flag Affected
Arithmetic			
ADD A,[m]	Add Data Memory to ACC	1	Z, C, AC, OV
ADDM A,[m]	Add ACC to Data Memory	1Note	Z, C, AC, OV
ADD A,x	Add immediate data to ACC	1	Z, C, AC, OV
ADC A,[m]	Add Data Memory to ACC with Carry	1	Z, C, AC, OV
ADCM A,[m]	Add ACC to Data memory with Carry	1Note	Z, C, AC, OV
SUB A,x	Subtract immediate data from the ACC	1	Z, C, AC, OV
SUB A,[m]	Subtract Data Memory from ACC	1	Z, C, AC, OV
SUBM A,[m]	Subtract Data Memory from ACC with result in Data Memory	1Note	Z, C, AC, OV
SBC A,[m]	Subtract Data Memory from ACC with Carry	1	Z, C, AC, OV
SBCM A,[m]	Subtract Data Memory from ACC with Carry, result in Data Memory	1Note	Z, C, AC, OV
DAA [m]	Decimal adjust ACC for Addition with result in Data Memory	1Note	C
Logic Operation			
AND A,[m]	Logical AND Data Memory to ACC	1	Z
OR A,[m]	Logical OR Data Memory to ACC	1	Z
XOR A,[m]	Logical XOR Data Memory to ACC	1	Z
ANDM A,[m]	Logical AND ACC to Data Memory	1Note	Z
ORM A,[m]	Logical OR ACC to Data Memory	1Note	Z
XORM A,[m]	Logical XOR ACC to Data Memory	1Note	Z
AND A,x	Logical AND immediate Data to ACC	1	Z
OR A,x	Logical OR immediate Data to ACC	1	Z
XOR A,x	Logical XOR immediate Data to ACC	1	Z
CPL [m]	Complement Data Memory	1Note	Z
CPLA [m]	Complement Data Memory with result in ACC	1	Z
Increment & Decrement			
INCA [m]	Increment Data Memory with result in ACC	1	Z
INC [m]	Increment Data Memory	1Note	Z
DECA [m]	Decrement Data Memory with result in ACC	1	Z
DEC [m]	Decrement Data Memory	1Note	Z
Rotate			
RRA [m]	Rotate Data Memory right with result in ACC	1	None
RR [m]	Rotate Data Memory right	1Note	None
RRCA [m]	Rotate Data Memory right through Carry with result in ACC	1	C
RRC [m]	Rotate Data Memory right through Carry	1Note	C
RLA [m]	Rotate Data Memory left with result in ACC	1	None
RL [m]	Rotate Data Memory left	1Note	None
RLCA [m]	Rotate Data Memory left through Carry with result in ACC	1	C
RLC [m]	Rotate Data Memory left through Carry	1Note	C

Mnemonic	Description	Cycles	Flag Affected
Data Move			
MOV A,[m]	Move Data Memory to ACC	1	None
MOV [m],A	Move ACC to Data Memory	1Note	None
MOV A,x	Move immediate data to ACC	1	None
Bit Operation			
CLR [m].i	Clear bit of Data Memory	1Note	None
SET [m].i	Set bit of Data Memory	1Note	None
Branch			
JMP addr	Jump unconditionally	2	None
SZ [m]	Skip if Data Memory is zero	1Note	None
SZA [m]	Skip if Data Memory is zero with data movement to ACC	1Note	None
SZ [m].i	Skip if bit i of Data Memory is zero	1Note	None
SNZ [m].i	Skip if bit i of Data Memory is not zero	1Note	None
SIZ [m]	Skip if increment Data Memory is zero	1Note	None
SDZ [m]	Skip if decrement Data Memory is zero	1Note	None
SIZA [m]	Skip if increment Data Memory is zero with result in ACC	1Note	None
SDZA [m]	Skip if decrement Data Memory is zero with result in ACC	1Note	None
CALL addr	Subroutine call	2	None
RET	Return from subroutine	2	None
RET A,x	Return from subroutine and load immediate data to ACC	2	None
RETI	Return from interrupt	2	None
Table Read			
TABRD [m]	Read table to TBLH and Data Memory	2Note	None
TABRDL [m]	Read table (last page) to TBLH and Data Memory	2Note	None
Miscellaneous			
NOP	No operation	1	None
CLR [m]	Clear Data Memory	1Note	None
SET [m]	Set Data Memory	1Note	None
CLR WDT	Clear Watchdog Timer	1	TO, PDF
CLR WDT1	Pre-clear Watchdog Timer	1	TO, PDF
CLR WDT2	Pre-clear Watchdog Timer	1	TO, PDF
SWAP [m]	Swap nibbles of Data Memory	1Note	None
SWAPA [m]	Swap nibbles of Data Memory with result in ACC	1	None
HALT	Enter power down mode	1	TO, PDF

Note: 1. For skip instructions, if the result of the comparison involves a skip then two cycles are required, if no skip takes place only one cycle is required.

2. Any instruction which changes the contents of the PCL will also require 2 cycles for execution.

3. For the “CLR WDT1” and “CLR WDT2” instructions the TO and PDF flags may be affected by the execution status. The TO and PDF flags are cleared after both “CLR WDT1” and “CLR WDT2” instructions are consecutively executed. Otherwise the TO and PDF flags remain unchanged.

Instruction Definition

ADC A,[m] Add Data Memory to ACC with Carry

Description: The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the Accumulator.

Operation: ACC ← ACC + [m] + C

Affected flag(s): OV, Z, AC, C

ADCM A,[m] Add ACC to Data Memory with Carry

Description: The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the specified Data Memory.

Operation: [m] ← ACC + [m] + C

Affected flag(s): OV, Z, AC, C

ADD A,[m] Add Data Memory to ACC

Description: The contents of the specified Data Memory and the Accumulator are added. The result is stored in the Accumulator.

Operation: ACC ← ACC + [m]

Affected flag(s): OV, Z, AC, C

ADD A,x Add immediate data to ACC

Description: The contents of the Accumulator and the specified immediate data are added. The result is stored in the Accumulator.

Operation: AC ← ACC + x

Affected flag(s): OV, Z, AC, C

ADDM A,[m] Add ACC to Data Memory

Description: The contents of the specified Data Memory and the Accumulator are added. The result is stored in the specified Data Memory.

Operation: [m] ← ACC + [m]

Affected flag(s): OV, Z, AC, C

AND A,[m] Logical AND Data Memory to ACC

Description: Data in the Accumulator and the specified Data Memory perform a bitwise logical AND operation. The result is stored in the Accumulator.

Operation: ACC ← ACC "AND" [m]

Affected flag(s): Z

AND A,x Logical AND immediate data to ACC

Description: Data in the Accumulator and the specified immediate data perform a bitwise logical AND operation. The result is stored in the Accumulator.

Operation: ACC ← ACC "AND"x

Affected flag(s): Z

ANDM A,[m] Logical AND ACC to Data Memory

Description: Data in the specified Data Memory and the Accumulator perform a bitwise logical AND operation. The result is stored in the Data Memory.

Operation: [m] ← ACC "AND" [m]

Affected flag(s): Z

CALL addr	Subroutine call
Description	Unconditionally calls a subroutine at the specified address. The Program Counter then increments by 1 to obtain the address of the next instruction which is then pushed onto the stack. The specified address is then loaded and the program continues execution from this new address. As this instruction requires an additional operation, it is a two cycle instruction.
Operation	Stack ← Program Counter + 1 Program Counter ← addr
Affected flag(s)	None

CLR [m]	Clear Data Memory
Description	Each bit of the specified Data Memory is cleared to 0.
Operation	[m] ← 00H
Affected flag(s)	None

CLR [m].i	Clear bit of Data Memory
Description	Bit i of the specified Data Memory is cleared to 0.
Operation	[m].i ← 0
Affected flag(s)	None

CLR WDT	Clear Watchdog Timer
Description	The TO, PDF flags and the WDT are all cleared.
Operation	WDT cleared TO ← 0 PDF ← 0
Affected flag(s)	TO, PDF

CLR WDT1	Pre-clear Watchdog Timer
Description	The TO, PDF flags and the WDTare all cleared. Note that this instruction works in conjunction with CLR WDT2 and must be executed alternately with CLR WDT2 to have effect. Repetitively executing this instruction without alternately executing CLR WDT2 will have no effect.
Operation	WDT cleared TO ← 0 PDF ← 0
Affected flag(s)	TO, PDF

CLR WDT2	Pre-clear Watchdog Timer
Description	The TO, PDF flags and the WDTare all cleared. Note that this instruction works in conjunction with CLR WDT1 and must be executed alternately with CLR WDT1 to have effect. Repetitively executing this instruction without alternately executing
Operation	WDT cleared TO ← 0 PDF ← 0
Affected flag(s)	TO, PDF

CPL [m] Complement Data Memory

Description Each bit of the specified Data Memory is logically complemented (1's complement). Bits which previously contained a 1 are changed to 0 and vice versa.

Operation [m] ← $\overline{[m]}$

Affected flag(s) Z

CPLA [m] Complement Data Memory with result in ACC

Description Each bit of the specified Data Memory is logically complemented (1's complement). Bits which previously contained a 1 are changed to 0 and vice versa. The complemented result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation ACC ← $\overline{[m]}$

Affected flag(s) Z

DAA [m] Decimal-Adjust ACC for addition with result in Data Memory

Description Convert the contents of the Accumulator value to a BCD (Binary Coded Decimal) value resulting from the previous addition of two BCD variables. If the low nibble is greater than 9 or if AC flag is set, then a value of 6 will be added to the low nibble. Otherwise the low nibble remains unchanged. If the high nibble is greater than 9 or if the C flag is set, then a value of 6 will be added to the high nibble. Essentially, the decimal conversion is performed by adding 00H, 06H, 60H or 66H depending on the Accumulator and flag conditions. Only the C flag may be affected by this instruction which indicates that if the original BCD sum is greater than 100, it allows multiple precision decimal addition.

Operation [m] ← ACC + 00H or
[m] ← ACC + 06H or
[m] ← ACC + 60H or
[m] ← ACC + 66H

Affected flag(s) C

DEC [m] Decrement Data Memory

Description Data in the specified Data Memory is decremented by 1.

Operation [m] ← [m] — 1

Affected flag(s) Z

DECA [m] Decrement Data Memory with result in ACC

Description Data in the specified Data Memory is decremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.

Operation ACC ← [m] — 1

Affected flag(s) Z

HALT	Enter power down mode
Description	This instruction stops the program execution and turns off the system clock. The contents of the Data Memory and registers are retained. The WDT and prescaler are cleared. The power down flag PDF is set and the WDT time-out flag TO is cleared.
Operation	TO ← 0 PDF ← 0
Affected flag(s)	TO, PDF

INC [m]	Increment Data Memory
Description	Data in the specified Data Memory is incremented by 1.
Operation	[m] ← [m]+1
Affected flag(s)	Z

INCA [m]	Increment Data Memory with result in ACC
Description	Data in the specified Data Memory is incremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	ACC ← [m]+1
Affected flag(s)	Z

JMP addr	Jump unconditionally
Description	The contents of the Program Counter are replaced with the specified address. Program execution then continues from this new address. As this requires the insertion of a dummy instruction while the new address is loaded, it is a two cycle instruction.
Operation	Program Counter ← addr
Affected flag(s)	None

MOV A,[m]	Move Data Memory to ACC
Description	The contents of the specified Data Memory are copied to the Accumulator.
Operation	ACC ← [m]
Affected flag(s)	None

MOV A,x	Move immediate data to ACC
Description	The immediate data specified is loaded into the Accumulator.
Operation	ACC ← x
Affected flag(s)	None

MOV [m],A	Move ACC to Data Memory
Description	The contents of the Accumulator are copied to the specified Data Memory.
Operation	[m] ← ACC
Affected flag(s)	None

NOP	No operation
Description	No operation is performed. Execution continues with the next instruction.
Operation	No operation
Affected flag(s)	None

OR A,[m] Logical OR Data Memory to ACC

Description: Data in the Accumulator and the specified Data Memory perform a bitwise logical OR operation. The result is stored in the Accumulator.

Operation: ACC ← ACC "OR" [m]

Affected flag(s): Z

OR A,x Logical OR immediate data to ACC

Description: Data in the Accumulator and the specified immediate data perform a bitwise logical OR operation. The result is stored in the Accumulator.

Operation: ACC ← ACC "OR" x

Affected flag(s): Z

ORM A,[m] Logical OR ACC to Data Memory

Description: Data in the specified Data Memory and the Accumulator perform a bitwise logical OR operation. The result is stored in the Data Memory.

Operation: [m] ← ACC "OR" [m]

Affected flag(s): Z

RET Return from subroutine

Description: The Program Counter is restored from the stack. Program execution continues at the restored address.

Operation: Program Counter ← Stack

Affected flag(s): None

RET A,x Return from subroutine and load immediate data to ACC

Description: The Program Counter is restored from the stack and the Accumulator loaded with the specified immediate data. Program execution continues at the restored address.

Operation: Program Counter ← Stack
ACC ← x

Affected flag(s): None

RETI Return from interrupt

Description: The Program Counter is restored from the stack and the interrupts are re-enabled by setting the EMI bit. EMI is the master interrupt global enable bit. If an interrupt was pending when the RETI instruction is executed, the pending Interrupt routine will be processed before returning to the main program.

Operation: Program Counter ← Stack
EMI ← 1

Affected flag(s): None

RL [m] Rotate Data Memory left

Description: The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0.

Operation: [m].(i+1) ← [m].i; (i=0~6)
[m].0 ← [m].7

Affected flag(s): None

RLA [m]	Rotate Data Memory left with result in ACC
Description	The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	ACC.(i+1) ← [m].i; (i=0~6) ACC.0 ← [m].7
Affected flag(s)	None

RLC [m]	Rotate Data Memory left through Carry
Description	The contents of the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into bit 0.
Operation	[m].(i+1) ← [m].i; (i=0~6) [m].0 ← C C ← [m].7
Affected flag(s)	C

RLCA [m]	Rotate Data Memory left through Carry with result in ACC
Description	Data in the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into the bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	ACC.(i+1) ← [m].i; (i=0~6) ACC.0 ← C C ← [m].7
Affected flag(s)	C

RR [m]	Rotate Data Memory right
Description	The contents of the specified Data Memory are rotated right by 1 bit with bit 0 rotated into bit 7.
Operation	[m].i ← [m].(i+1); (i=0~6) [m].7 ← [m].0
Affected flag(s)	None

RRA [m]	Rotate Data Memory right with result in ACC
Description	Data in the specified Data Memory and the carry flag are rotated right by 1 bit with bit 0 rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	ACC.i ← [m].(i+1); (i=0~6) ACC.7 ← [m].0
Affected flag(s)	None

RRC [m]	Rotate Data Memory right through Carry
Description	The contents of the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7.
Operation	[m].i ← [m].(i+1); (i=0~6) [m].7 ← C C ← [m].0
Affected flag(s)	C

RRCA [m] Rotate Data Memory right through Carry with result in ACC

Description: Data in the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation:
ACC.i ← [m].(i+1); (i=0~6)
ACC.7 ← C
C ← [m].0

Affected flag(s): C

SBC A,[m] Subtract Data Memory from ACC with Carry

Description: The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation: ACC ← ACC — [m] — $\overline{C}$

Affected flag(s): OV, Z, AC, C

SBCM A,[m] Subtract Data Memory from ACC with Carry and result in Data Memory

Description: The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation: ACC ← ACC — [m] — $\overline{C}$

Affected flag(s): OV, Z, AC, C

SDZ [m] Skip if decrement Data Memory is 0

Description: The contents of the specified Data Memory are first decremented by 1. If the result is 0 the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.

Operation:
[m] ← [m] — 1
Skip if [m]=0

Affected flag(s): None

SDZA [m] Skip if decrement Data Memory is zero with result in ACC

Description: The contents of the specified Data Memory are first decremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction.

Operation:
ACC ← [m] — 1

Affected flag(s):
Skip if ACC=0
None

SET [m]	Set Data Memory
Description	Each bit of the specified Data Memory is set to 1.
Operation	[m] ← FFH
Affected flag(s)	None

SET [m].i	Set bit of Data Memory
Description	Bit i of the specified Data Memory is set to 1.
Operation	[m].1 ← 1
Affected flag(s)	None

SIZ [m]	Skip if increment Data Memory is 0
Description	The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	[m] ← [m] + 1 Skip if [m]=0
Affected flag(s)	None

SIZA [m]	Skip if increment Data Memory is zero with result in ACC
Description	The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	ACC ← [m] + 1 Skip if ACC=0
Affected flag(s)	None

SNZ [m].i	Skip if bit i of Data Memory is not 0
Description	If bit i of the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is 0 the program proceeds with the following instruction.
Operation	Skip if [m].i ≠ 0
Affected flag(s)	None

SUB A,[m]	Subtract Data Memory from ACC
Description	The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	ACC ← ACC — [m]
Affected flag(s)	OV, Z, AC, C

SUBM A,[m] Subtract Data Memory from ACC with result in Data Memory

Description The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation [m] ← ACC — [m]

Affected flag(s) OV, Z, AC, C

SUB A,x Subtract immediate data from ACC

Description The immediate data specified by the code is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation ACC ← ACC — x

Affected flag(s) OV, Z, AC, C

SWAP [m] Swap nibbles of Data Memory

Description The low-order and high-order nibbles of the specified Data Memory are interchanged.

Operation [m].3~[m].0↔[m].7~[m].4

Affected flag(s) None

SWAPA [m] Swap nibbles of Data Memory with result in ACC

Description The low-order and high-order nibbles of the specified Data Memory are interchanged. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.

Operation ACC.3~ACC.0 ← [m].7~[m].4
ACC.7~ACC.4 ← [m].3~[m].0

Affected flag(s) None

SZ [m] Skip if Data Memory is 0

Description If the contents of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.

Operation Skip if [m]=0

Affected flag(s) None

SZA [m] Skip if Data Memory is 0 with data movement to ACC

Description The contents of the specified Data Memory are copied to the Accumulator. If the value is zero, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.

Operation ACC ← [m]
Skip if [m]=0

Affected flag(s) None

SZ [m].i	Skip if bit i of Data Memory is 0
Description	If bit i of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction.
Operation	Skip if [m].i=0
Affected flag(s)	None
TABRD [m]	Read table to TBLH and Data Memory
Description	The low byte of the program code addressed by the table pointer (TBLP/TBHP) is moved to the specified data memory and the high byte transferred to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None
TABRDL [m]	Read table (last page) to TBLH and Data Memory
Description	The low byte of the program code (last page) addressed by the table pointer (TBLP/TBHP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None
XOR A,[m]	Logical XOR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC "XOR" [m]
Affected flag(s)	Z
XORM A,[m]	Logical XOR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical XOR operation. The result is stored in the Data Memory.
Operation	[m] ← ACC "XOR" [m]
Affected flag(s)	Z
XOR A,x	Logical XOR immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC "XOR" x
Affected flag(s)	Z

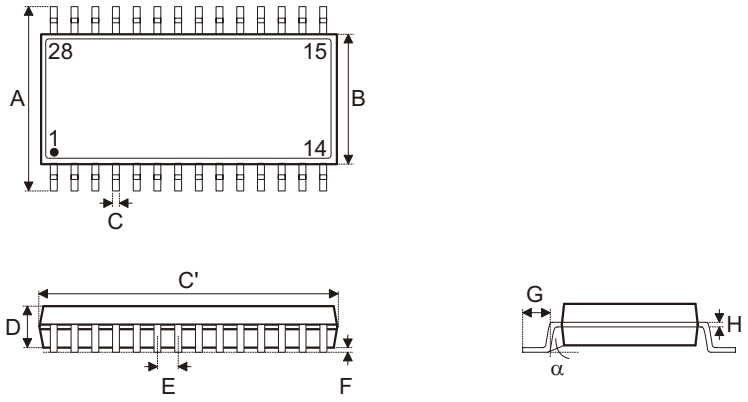
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the package information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information
- PB FREE Products
- Green Packages Products

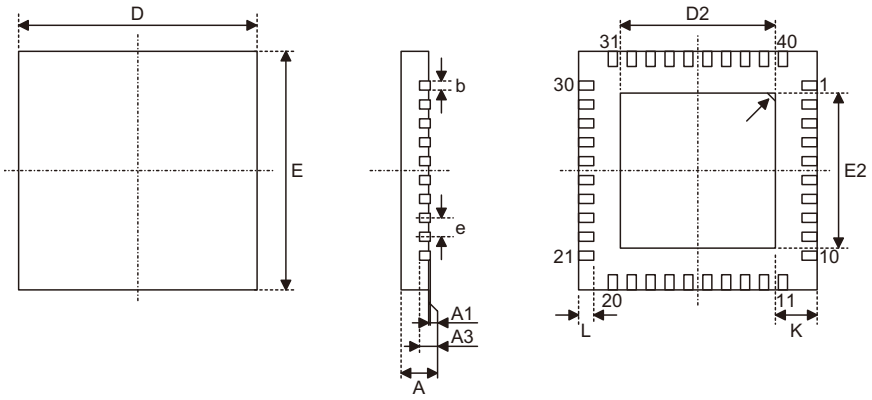
28-pin SSOP(150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.228	—	0.244
B	0.150	—	0.157
C	0.008	—	0.012
C’	0.386	—	0.394
D	0.054	—	0.060
E	—	0.025	—
F	0.004	—	0.010
G	0.022	—	0.028
H	0.007	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	5.79	—	6.20
B	3.81	—	3.99
C	0.20	—	0.30
C’	9.80	—	10.01
D	1.37	—	1.52
E	—	0.64	—
F	0.10	—	0.25
G	0.56	—	0.71
H	0.18	—	0.25
α	0°	—	8°

SAW Type 40-pin (6mm×6mm for 0.75mm) QFN Outline Dimensions

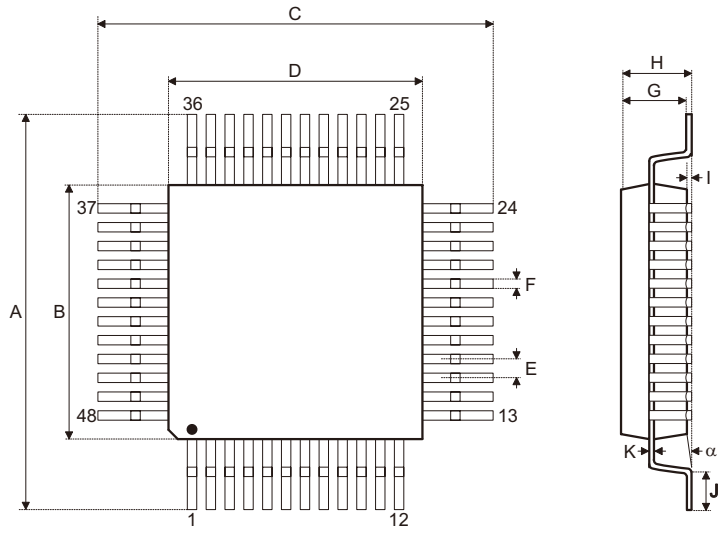


GTK

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008	—
b	0.007	0.010	0.012
D	—	0.236	—
E	—	0.236	—
e	—	0.020	—
D2	0.173	0.177	0.179
E2	0.173	0.177	0.179
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	—	0.20	—
b	0.18	0.25	0.30
D	—	6.00	—
E	—	6.00	—
e	—	0.50	—
D2	4.40	4.50	4.55
E2	4.40	4.50	4.55
L	0.35	0.40	0.45
K	0.20	—	—

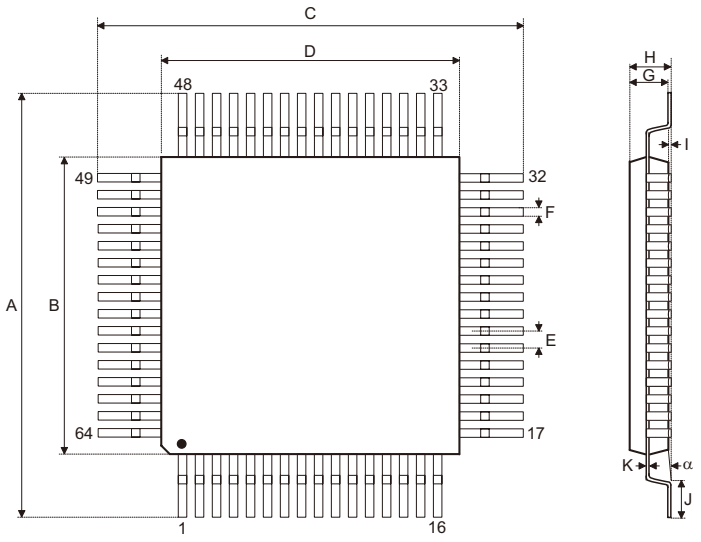
48-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.350	—	0.358
B	0.272	—	0.280
C	0.350	—	0.358
D	0.272	—	0.280
E	—	0.020	—
F	—	0.008	—
G	0.053	—	0.057
H	—	—	0.063
I	—	0.004	—
J	0.018	—	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	8.90	—	9.10
B	6.90	—	7.10
C	8.90	—	9.10
D	6.90	—	7.10
E	—	0.50	—
F	—	0.20	—
G	1.35	—	1.45
H	—	—	1.60
I	—	0.10	—
J	0.45	—	0.75
K	0.10	—	0.20
α	0°	—	7°

64-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.350	—	0.358
B	0.272	—	0.280
C	0.350	—	0.358
D	0.272	—	0.280
E	—	0.016	—
F	0.005	—	0.009
G	0.053	—	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	—	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	8.90	—	9.10
B	6.90	—	7.10
C	8.90	—	9.10
D	6.90	—	7.10
E	—	0.40	—
F	0.13	—	0.23
G	1.35	—	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	—	0.75
K	0.09	—	0.20
α	0°	—	7°