



5N70K

Preliminary

Power MOSFET

5A, 700V N-CHANNEL POWER MOSFET

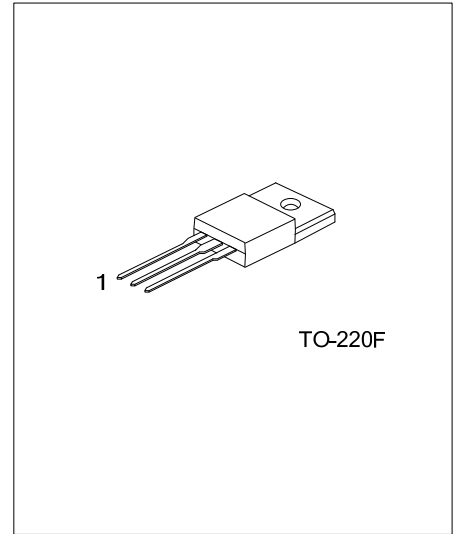
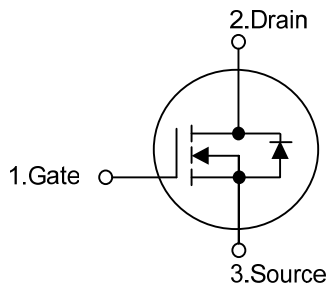
DESCRIPTION

The UTC **5N70K** is a high voltage power MOSFET designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and high rugged avalanche characteristics. This power MOSFET is usually used in high speed switching applications at power supplies, PWM motor controls, high efficient DC to DC converters and bridge circuits.

FEATURES

- * $R_{DS(ON)} = 2.4\Omega @ V_{GS} = 10V$
- * Ultra Low Gate Charge (Typical 15 nC)
- * Low Reverse Transfer Capacitance ($C_{RSS} = \text{Typical } 6.5 \text{ pF}$)
- * Fast Switching Capability
- * Improved dv/dt Capability, High Ruggedness

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
5N70KL-TF3-T	5N70KG-TF3-T	TO-220F	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>5N70KL-TF3-T</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Lead Free</p>	<p>(1) T: Tube</p> <p>(2) TF3: TO-220F</p> <p>(3) L: Lead Free, G: Halogen Free</p>
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■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	700	V
Gate-Source Voltage	V_{GSS}	± 30	V
Avalanche Current (Note 2)	I_{AR}	5	A
Continuous Drain Current	I_D	5	A
Pulsed Drain Current (Note 2)	I_{DM}	20	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	100
	Repetitive (Note 2)	E_{AR}	10
Peak Diode Recovery dv/dt (Note 4)	dv/dt	4.5	V/ns
Power Dissipation	P_D	36	W
Junction Temperature	T_J	+150	$^\circ\text{C}$
Operation Temperature	T_{OPR}	-55~+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~+150	$^\circ\text{C}$

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Pulse width limited by $T_{J(MAX)}$

3. $L = 8\text{mH}$, $I_{AS} = 5\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 5\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	3.47	$^\circ\text{C}/\text{W}$

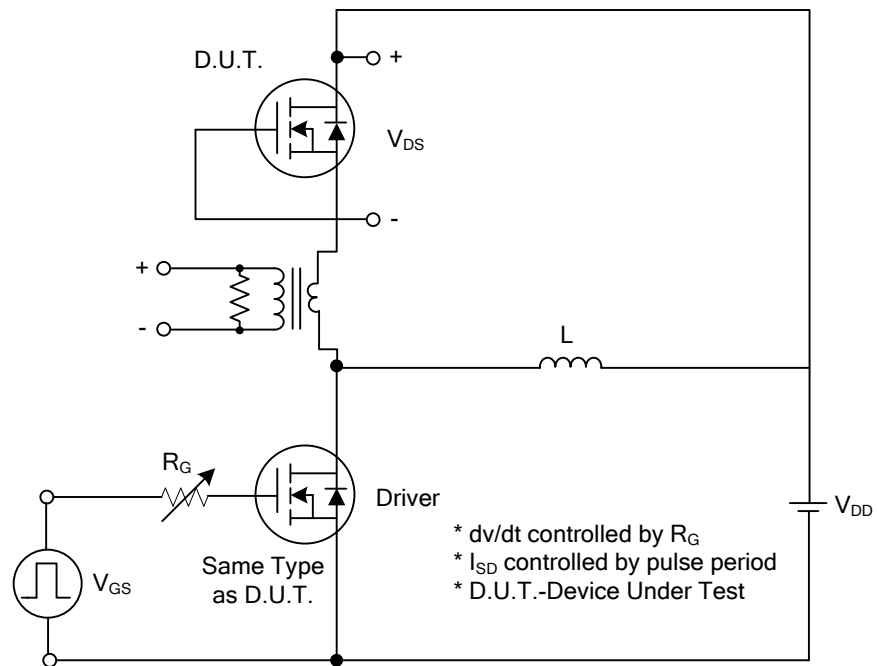
■ ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	700			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS} = 700V, V_{GS} = 0V$			1	μA
Gate-Source Leakage Current	Forward	I_{GSS}			100	nA
	Reverse				-100	
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	$I_D = 250\mu A$, Referenced to 25°C		0.6		$V/^\circ\text{C}$
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 2.5A$		2.0	2.4	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$		515	670	pF
Output Capacitance	C_{OSS}			55	72	pF
Reverse Transfer Capacitance	C_{RSS}			6.5	8.5	pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD} = 325V, I_D = 5A,$ $R_G = 25\Omega$ (Note 1, 2)		10	30	ns
Turn-On Rise Time	t_R			60	90	ns
Turn-Off Delay Time	$t_{D(OFF)}$			38	85	ns
Turn-Off Fall Time	t_F			50	100	ns
Total Gate Charge	Q_G	$V_{DS} = 520V, I_D = 5A,$ $V_{GS} = 10V$ (Note 1, 2)		15	19	nC
Gate-Source Charge	Q_{GS}			2.5		nC
Gate-Drain Charge	Q_{GD}			6.6		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS} = 0V, I_S = 5A$			1.4	V
Maximum Continuous Drain-Source Diode Forward Current	I_S				5	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				20	A
Reverse Recovery Time	t_{rr}	$V_{GS} = 0V, I_S = 5A,$ $dI_F / dt = 100 A/\mu s$ (Note 1)		300		ns
Reverse Recovery Charge	Q_{RR}			2.2		μC

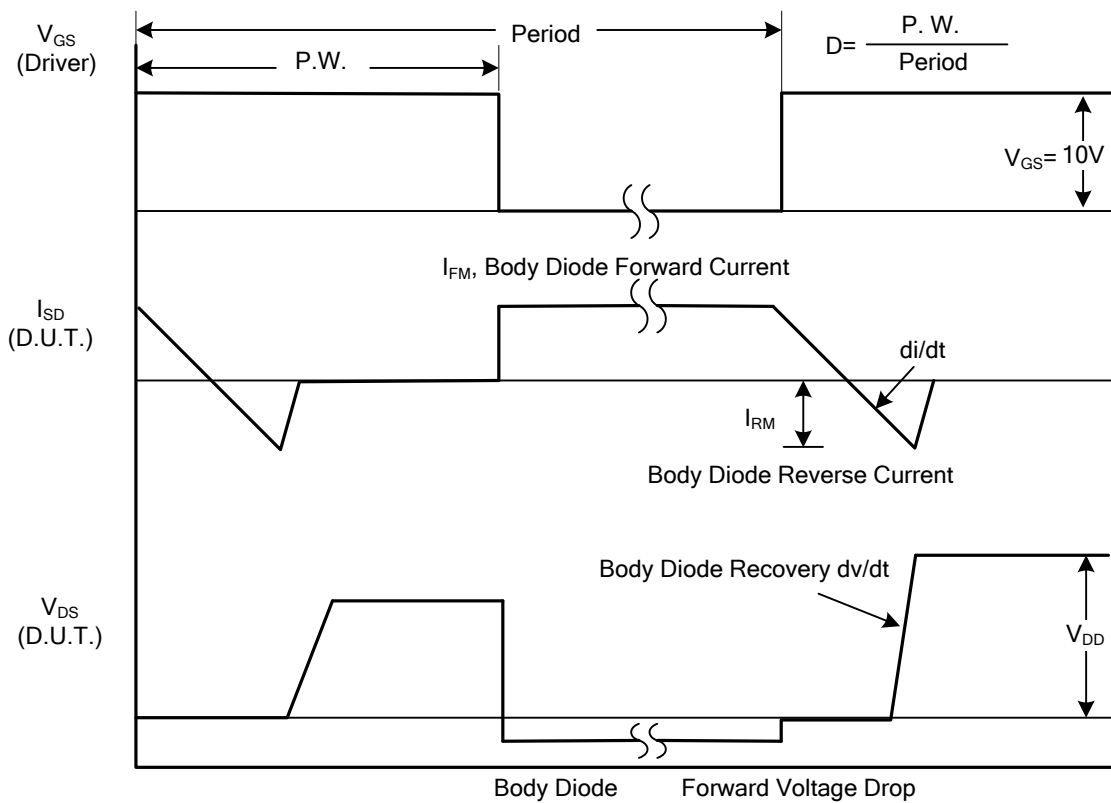
Notes: 1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$

2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

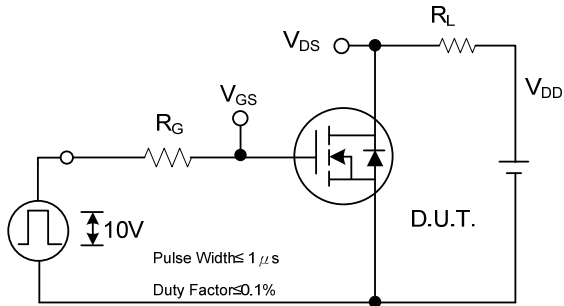


Peak Diode Recovery dv/dt Test Circuit

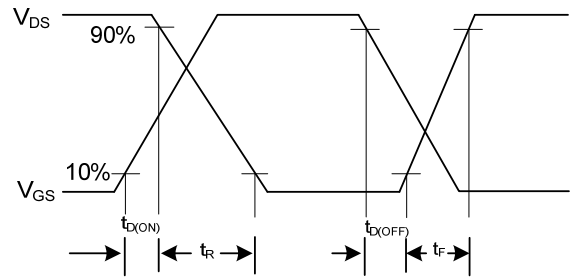


Peak Diode Recovery dv/dt Waveforms

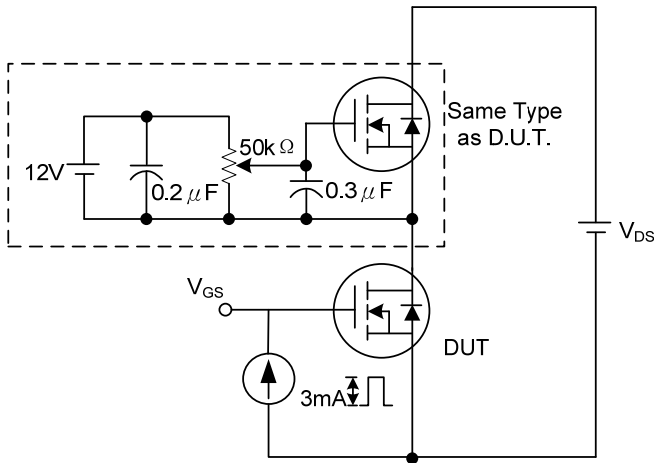
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



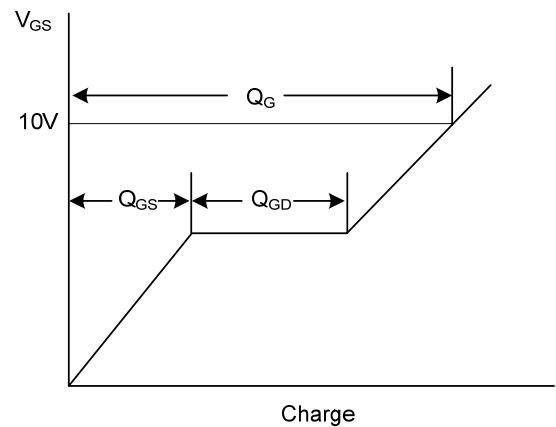
Switching Test Circuit



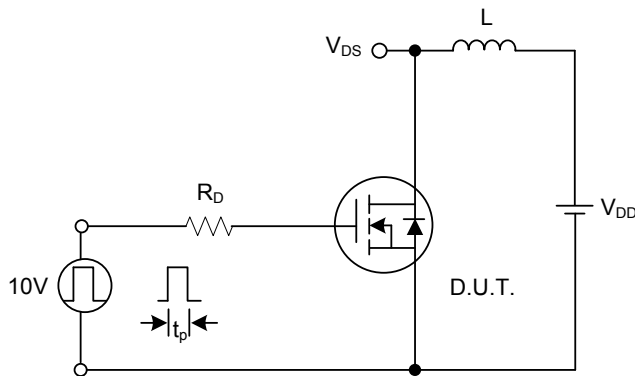
Switching Waveforms



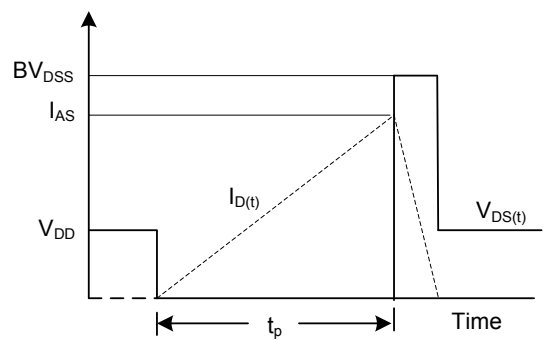
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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