



## UPS1702

Preliminary

LINEAR INTEGRATED CIRCUIT

### HIGH PERFORMANCE CURRENT MODE POWER SWITCH

#### DESCRIPTION

The UTC **UPS1702** is an integrated PWM controller and Power MOSFET specifically designed for current mode operation with minimal external components. The UTC **UPS1702** is designed to provide several special enhancements to satisfy the needs, for example, Power-Saving mode for low standby power (<0.3W), Frequency Hopping , Constant Output Power Limiting , Over Current Protection (OCP), Over Voltage Protection (OVP), Under Voltage Lock Out (UVLO), and Over Temperature Protection (OTP) etc. IC will be shutdown or can auto-restart in certain situations.

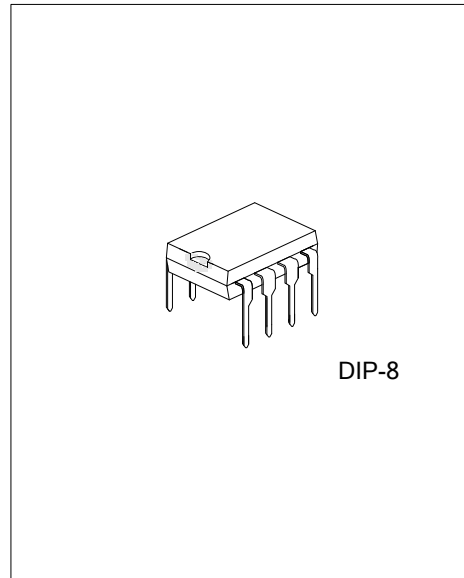
#### FEATURE

- \* Internal High Voltage Start-up Circuit
- \* Internal 700V Power MOSFET
- \* Lower than 0.3W Standby Power Design
- \* Gate Output Maximum Voltage Clamp(15V)
- \* Over temperature protection
- \* Over voltage protection
- \* Leading edge blanking
- \* Cycle-by-Cycle current limiting
- \* Under Voltage Lock Out

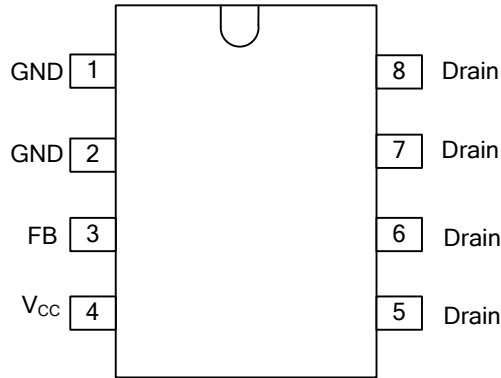
#### ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UPS1702L-D08-T	UPS1702G-D08-T	DIP-8	Tube

<p>UPS1702L-D08-T</p> <p>(1) Packing Type (2) Package Type (3) Lead Free</p>	<p>(1) T: Tube (2) D08: DIP-8 (3) L: Lead Free, G: Halogen Free</p>
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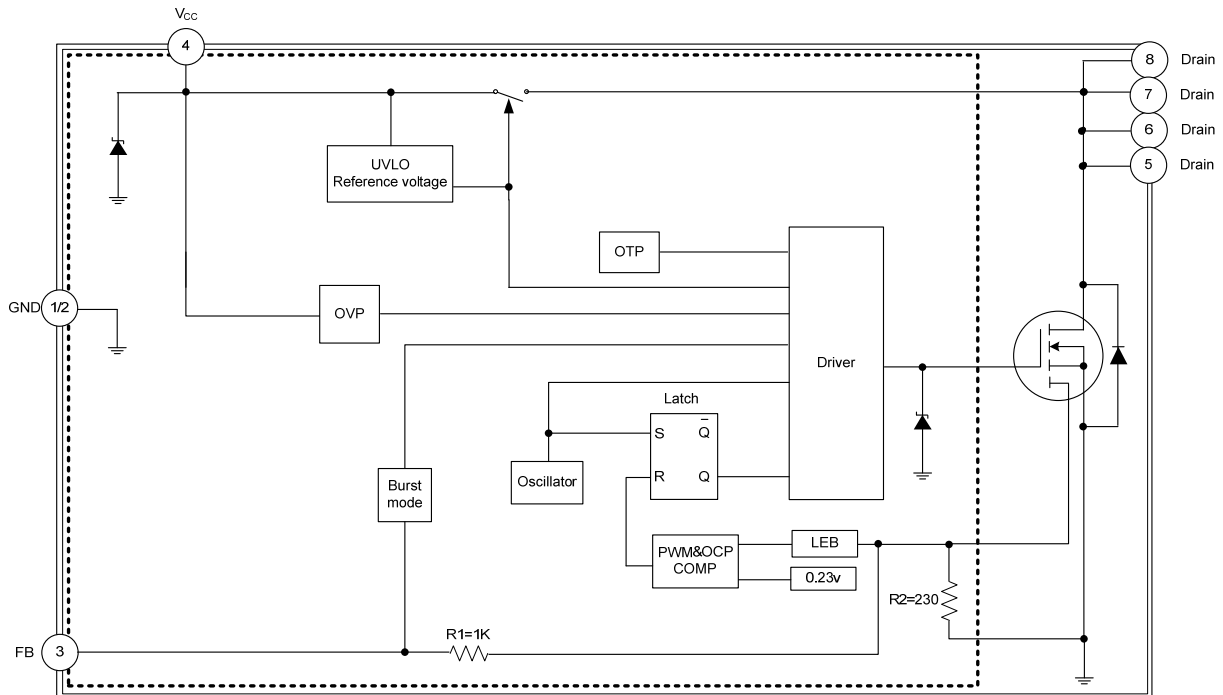
### PIN CONFIGURATION



### PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1、 2	GND	Ground
3	FB	Feedback
4	V <sub>CC</sub>	Supply voltage
5-8	Drain	Power MOSFET drain

### BLOCK DIAGRAM



- Notes: OTP (Over Temperature Protection)  
 OVP (Over Voltage Protection)  
 OCP (Over Current Protection)  
 UVLO (Under Voltage Latch-Out)  
 LEB (Led Edge Blanking)

■ ABSOLUTE MAXIMUM RATING ( $T_A=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Switching Drain Source Voltage	$V_{DS(SW)}$	700	V
Supply Voltage	$V_{CC}$	30	V
Feedback Current	$I_{FB}$	3	mA
Junction Temperature	$T_J$	+150	$^{\circ}\text{C}$
Operating Temperature	$T_{OPR}$	-40 ~ +125	$^{\circ}\text{C}$
Storage Temperature	$T_{STG}$	-50 ~ +150	$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ OPERATING RANGE

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{CC}$	8.6 ~ 22	V

■ ELECTRICAL CHARACTERISTICS ( $T_A=25^{\circ}\text{C}$ ,  $V_{CC}=15\text{V}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY SECTION</b>						
Start Up Charge Current	$I_{CH}$	$V_{DS}=100\text{V}$ , $V_{CC}=0\sim V_{CCON}$			1	mA
Start Up Current	$I_{ST}$	$V_{CC} = V_{CCON}-0.2\text{V}$		6	45	$\mu\text{A}$
Supply Current with switch	$I_{OP}$	$I_{FB}=0.5\text{mA}$ , $I_D=50\text{mA}$		2	6.5	mA
<b>UNDER-VOLTAGE LOCKOUT SECTION</b>						
Start Threshold Voltage	$V_{CCON}$		13.5	15	16.5	V
Min. Operating Voltage	$V_{CCOFF}$		8	9	10	V
<b>INTERNAL VOLTAGE REFERENCE</b>						
<b>CONTROL SECTION</b>						
$I_{FB}$ to $I_D$ Current Gain	$G_{FB-D}$			560		
Feedback Source Shutdown Current	$I_{FBSD}$			900		$\mu\text{A}$
FB Pin Input Impedance	$R_{FB}$			1200		$\Omega$
Burst-Mode Out FB Voltage	$V_{FB(OUT)}$			0.94		V
Burst-Mode Enter FB Voltage	$V_{FB(IN)}$			1.05		V
Normal initial Switching frequency	$F_{(SW)}$		54	60	66	kHz
Frequency Deviation VS $V_{CC}$	$F_{DV}$	$V_{CC}=10$ to $22\text{V}$			5	%
Frequency Deviation VS Temperature	$F_{DT}$	$T_A = -40$ to $105^{\circ}\text{C}$			5	%
<b>PROTECTION SECTION</b>						
OVP threshold	$V_{OVP}$			23		V
OTP threshold	$T_{(THR)}$		130	150	170	$^{\circ}\text{C}$
<b>CURRENT LIMITING SECTION</b>						
Peak Current Limitation	$I_{LIM}$	$V_{FB}=0\text{V}$	0.56	0.7	0.84	A
Minimum Turn On Time	$t_{ON(MIN)}$			680		nS
<b>POWER MOSFET SECTION</b>						
Drain-Source Breakdown Voltage	$V_{DSS}$	$V_{FB}=2\text{V}$ , $I_D=250\mu\text{A}$	700			V
Turn-on voltage between gate and source	$V_{TH}$	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	2		4	V
Off State Drain Current	$I_{DSS}$	$V_{DS}=500\text{V}$ , $V_{FB}=2\text{V}$			100	$\mu\text{A}$
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=0.4\text{A}$			5	$\Omega$
Rise Time	$t_R$	$V_{DD} = 300\text{V}$ , $I_D = 4.0\text{A}$ $RG=25\Omega$ (Note 1, 2)		45	100	ns
Fall Time	$t_F$			35	80	ns
Drain Capacitance	$C_{OSS}$	$V_{DS}=25\text{V}$		40		pF

Note: 1. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$   
2. Essentially independent of operating temperature

■ FUNCTIONAL DESCRIPTION

The internal reference voltages and bias circuit work at  $V_{CC} > V_{THD(ON)}$ , and shutdown at  $V_{CC} < V_{CC(MIN)}$ .

(1) High Voltage Start up switch Circuit

At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor connected to the  $V_{CC}$  pin. When  $V_{CC}$  reaches  $V_{THD(ON)}$ , the IC begins switching and the internal high-voltage current source is disabled. The IC continues its normal switching operation and the power is supplied from the auxiliary transformer winding unless  $V_{CC}$  goes below the stop voltage of  $V_{CC(MIN)}$ .

(2) Switching Frequency Limit

The UTC UPS1702 have a constant switching frequency of 60kHz.

(3) Protection section

The IC takes on more protection functions such as OVP and OTP etc. In case of those failure modes for continual blanking time, the driver is shut down. At the same time, IC enters auto-restart,  $V_{CC}$  power on and driver is reset after  $V_{CC}$  power on again.

OVP

OVP will shutdown the switching of the power MOSFET whenever  $V_{CC} > V_{OVP}$ . The OVP case as followed Fig. 1 the test circuit as followed Fig. 2.

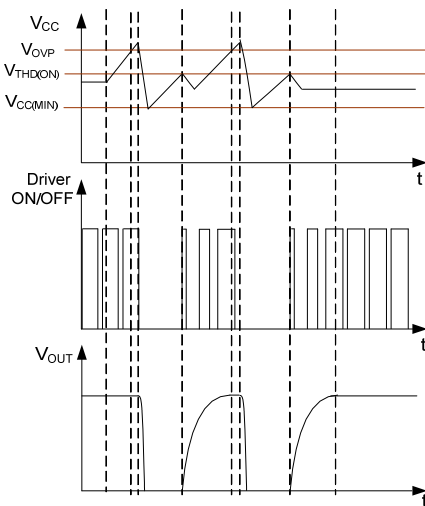


Fig.1 OVP case

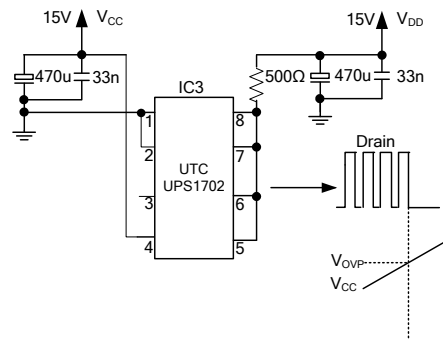


Fig.2 OVP test circuit

OTP

OTP will shut down driver and latch-off when junction temperature  $T_J > T_{(THR)}$ , and IC will be release on when temperature decreasing under  $T_{(THR)} - 30$  and powering on again.

(4) The Gain of FB pin to Drain Current Limiting

$$I_{LIM} = G_{FB-D} \times 0.23V \times (R2 || R1)$$

(5) Driver Output Section

The driver-stage drives the gate of the MOSFET and is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch on slope when reaching the MOSFET threshold. This is achieved by a slope control of the rising edge at the driver's output. The output driver is clamped by an internal 15V Zener diode in order to protect power MOSFET transistors against undesirable gate over voltage.

(6) Inside Power MOSFET

Specific Power MOSFET parameter is as "Power MOSFET SECTION" in electrical characteristics table.

■ TYPICAL APPLICATION CIRCUIT

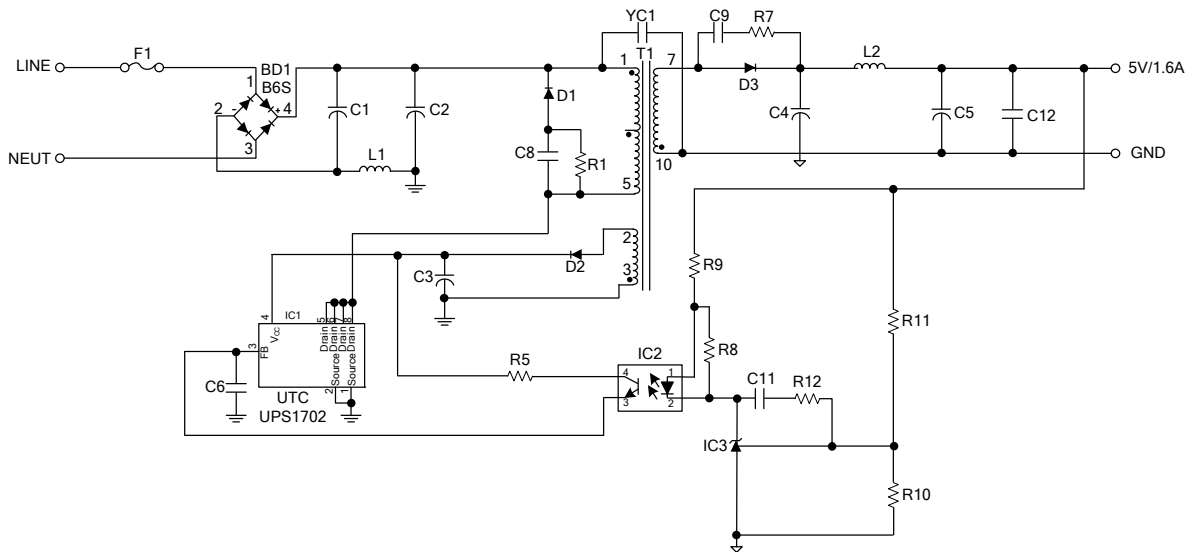


Fig. 3 UTC UPS1702 Typical Application Circuit

Table1. Components reference description for UTC UPS1702 application circuit

DESIGNATOR	PART TYPE	DESIGNATOR	PART TYPE	DESIGNATOR	PART TYPE
C1	10μF/400V	R1	100KΩ	D1	FR107
C2	10μF/400V	R5	6.8KΩ	D2	RS1D
C3	10μF/50V	R7	30Ω	D3	SR39
C4	470μF/16V	R8	2.2KΩ	IC1	UPS1702
C5	220μF/16V	R9	510Ω	IC2	PC-817
C6	103pF	R10	5.1KΩ	IC3	TL431
C8	102pF/1KV	R11	5.1KΩ	YC1	102pF/400V
C9	102pF/100V	R12	15KΩ	T1	EE-19
C11	103pF			L1	1mH
C12	103pF			L2	2μH
				F1	1A/250V
				BD1	B6S

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