TV and VTR stereo/dual sound processor with digital identification and I²C-bus

TDA9840

FEATURES

- Supply voltage 5 to 8 V
- De-emphasis
- Source selector
- Level and stereo matrix adjustment possible via the I²C-bus
- I²C-bus transceiver
- AF inputs for NICAM or AM sound (standard L)
- AF outputs for Main and SCART
- AF input and output signals selectable via the I²C-bus
- Information for identified transmission mode is readable via I²C-bus
- Software is compatible with the TDA8415/16/17
- Quartz oscillator and clock generator
- Three digital PLL, alignment-free
- Two digital integrators, alignment-free
- Stabilizer circuit for ripple rejection and constant output signals
- ESD protection of all pins.

GENERAL DESCRIPTION

The TDA9840 is a stereo/dual sound processor for TV and VTR sets. Its identification ensures safe operation by using internal digital PLL technique with extremely small bandwidth, synchronous detection and digital integration (switching time maximum 2.3 s; identification concerning the main functions).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9840	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
TDA9840T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 18)		4.5	5	8.8	V
I_P	supply current (pin 18)		15.5	16.5	20.5	mA
$V_{i(rms)}$	nominal input signal voltage (V_{i1}, V_{i2}, V_{i3}) (RMS value)	54% modulation	–	250	–	mV
$V_{o(rms)}$	nominal output signal voltage (RMS value)	THD ≤ 0.3% 54% modulation	–	500	–	mV
$V_{o(rms)}$	clipping level of the output signal voltages (RMS value)	THD ≤ 1.5%				
		V_P = 5 V	1.4	1.6	–	V
		V_P = 8 V	2.4	2.65	–	V
ΔG_v	stereo control range for V_{i1} (0.1 dB steps)		+2.4	+2.5	+2.6	dB
			−2.3	−2.4	−2.5	dB
	level control range for V_{i2} (0.5 dB steps)		+2.4	+2.5	+2.6	dB
			−1.9	−2.0	−2.1	dB
$V_{i\,pil}$	input voltage sensitivity of pilot frequency	unmodulated	5	–	100	mV
S/N(W)	weighted signal-to-noise ratio	*"CCIR468-3"*	66	75	–	dB
THD	total harmonic distortion		–	0.2	0.3	%
T_{amb}	operating ambient temperature range		0	–	+70	°C
f_{ident}	identification window width	normal mode				
		STEREO	2.0	–	2.0	Hz
		DUAL	2.3	–	2.3	Hz
		fast mode				
		STEREO	3.8	–	3.8	Hz
		DUAL	5.8	–	5.8	Hz
$t_{ident\ ON}$	total identification time ON	normal mode				
		STEREO	0.35	–	2.3	s
		DUAL	0.35	–	2.0	s
		fast mode				
		STEREO	0.175	–	1.1	s
		DUAL	0.175	–	1.0	s
$V_{i\,tuner}$	identification voltage sensitivity		–	28	–	dBμV
Δf_{pil}	pull-in frequency range of pilot PLL	f_ω = 10.008 MHz				
		lower side	−296	–	−296	Hz
		upper side	302	–	302	Hz

BLOCK DIAGRAMS

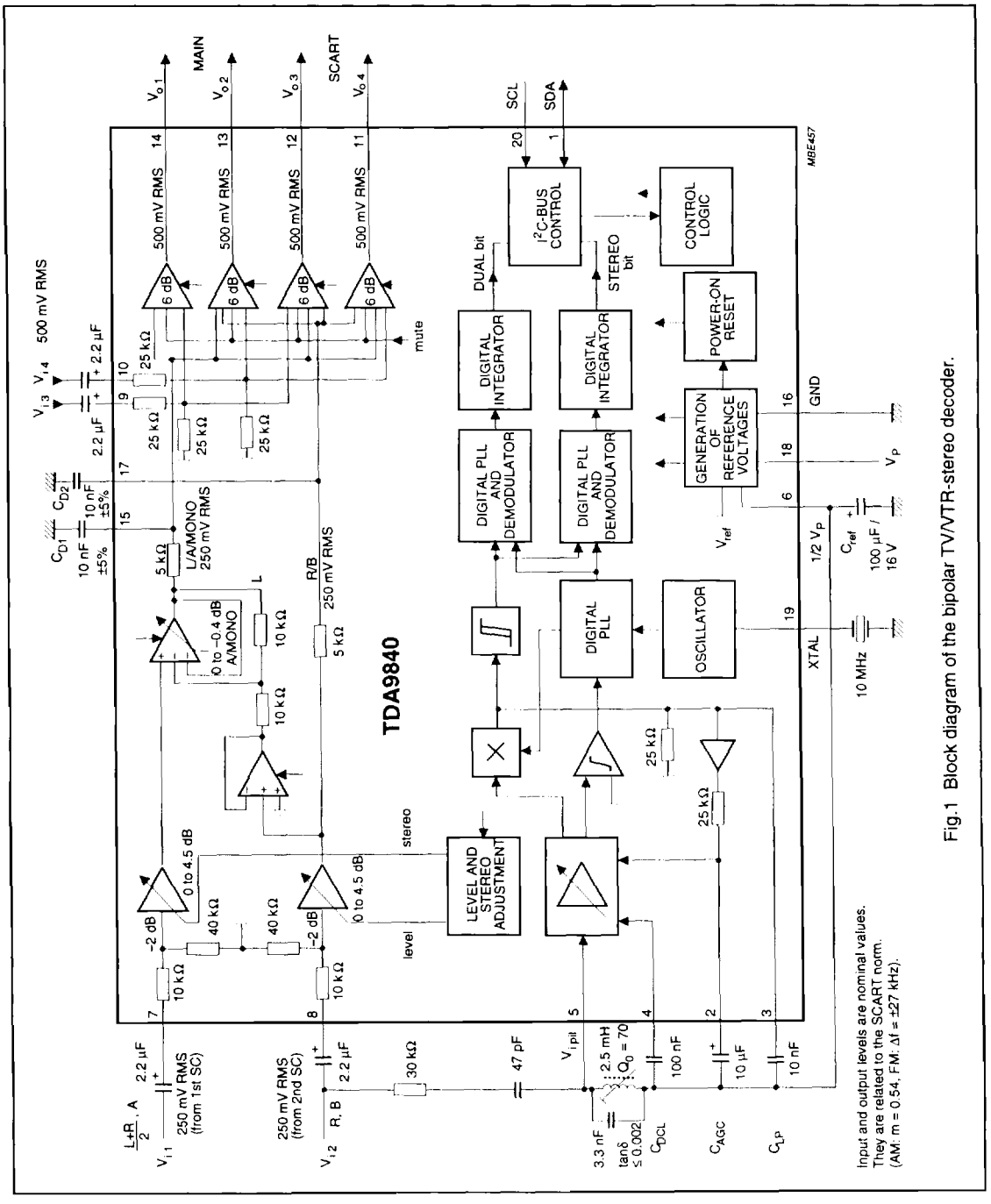
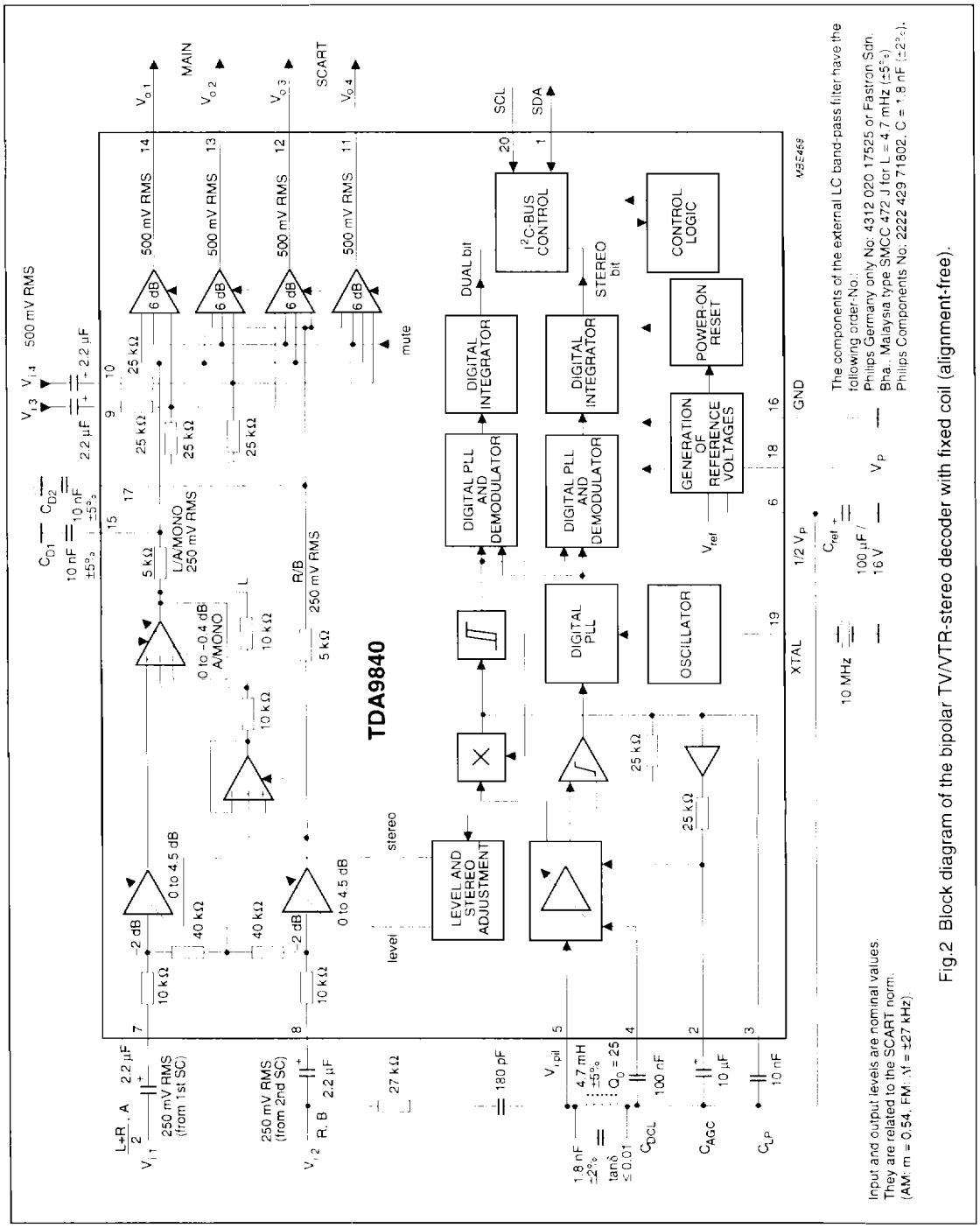


Fig.1 Block diagram of the bipolar TV/VTR-stereo decoder.

Input and output levels are nominal values. They are related to the SCART norm. (AM: m = 0.54, FM: Δf = ±27 kHz).



Input and output levels are nominal values. They are related to the SCART norm. (AM: m = 0.54, FM: Δf = ±27 kHz).

The components of the external LC band-pass filter have the following order-No.:
Philips Germany only No: 4312 020 17525 or Fastron Sdn. Bhd., Malaysia type SMCC 472 J for L = 4.7 mH (±5%) Philips Components No: 2222 429 71802, C = 1.8 nF (±2%).

Fig.2 Block diagram of the bipolar TV/VTR-stereo decoder with fixed coil (alignment-free).

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus data input/output
C_{AGC}	2	AGC capacitor of pilot frequency amplifier
C_{LP}	3	identification low-pass capacitor
C_{DCL}	4	DC loop capacitor
$V_{i\,pil}$	5	pilot frequency input voltage
C_{ref}	6	capacitor of reference voltage ($\frac{1}{2}V_P$)
$V_{i\,1}$	7	AF input signal $V_{i\,1}$ (from 1st sound carrier)
$V_{i\,2}$	8	AF input signal $V_{i\,2}$ (from 2nd sound carrier)
$V_{i\,3}$	9	AF input signal $V_{i\,3}$ (NICAM or AM sound (standard L))
$V_{i\,4}$	10	AF input signal $V_{i\,4}$ (NICAM)
$V_{o\,4}$	11	AF output signal $V_{o\,4}$ (SCART)
$V_{o\,3}$	12	AF output signal $V_{o\,3}$ (SCART)
$V_{o\,2}$	13	AF output signal $V_{o\,2}$ (main)
$V_{o\,1}$	14	AF output signal $V_{o\,1}$ (main)
C_{D1}	15	50 µs de-emphasis capacitor of AF Channel 1
GND	16	ground (0 V)
C_{D2}	17	50 µs de-emphasis capacitor of AF Channel 2
V_P	18	supply voltage (+5 to +8 V)
XTAL	19	10 MHz crystal input
SCL	20	I²C-bus clock input

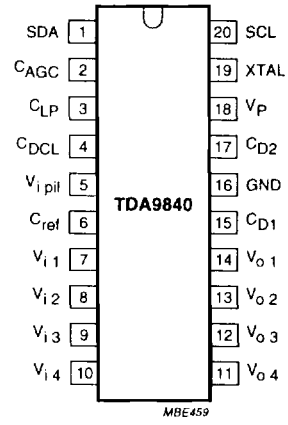


Fig.3 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA9840 (see Fig.1) receives the signals from the FM-demodulators in a TV two sound-carrier system. The circuit is realized by the H00485 bipolar process.

The IC is intended for use in economic TV and VTR receivers. Therefore optimum relationship between integration of functions and use of external components has been striven for. Additionally a new type of identification circuit has been developed.

AF signal handling

The input AF signals, derived from the two sound carriers, are processed in analog form using operational amplifiers.The circuit incorporates level- and stereo-adjustment to correct the spreading in the FM detector output levels. Dematrixing uses the technique of two amplifiers processing the AF signals. Finally, a source selector provides the facility to route the mono signal through to the outputs ('forced mono').

De-emphasis is performed by two RC low-pass filter networks with internal resistors and external capacitors. This provides a frequency response with the tolerances given in Fig.4.

A source selector, controlled via the I²C-bus, allows selection of the different modes of operation in accordance with the transmitted signal. The device was designed for a nominal input signal (FM: 54% modulation is equivalent to $\Delta f = \pm 27$ kHz / AM: m = 0.54) of 250 mV RMS ($V_{i\,1}$, $V_{i\,2}$), respectively 500 mV RMS ($V_{i\,3}$,$V_{i\,4}$). A nominal gain of 6 dB for $V_{i\,1}$ and $V_{i\,2}$ signals and 0 dB for $V_{i\,3}$ and $V_{i\,4}$ signals is built-in. By using rail-to-rail operational amplifiers, the clipping level (THD ≤1.5%) is 1.6 V RMS for V_P = 5 V and 2.65 V RMS for V_P = 8 V at outputs $V_{o\,1}$, $V_{o\,2}$,$V_{o\,3}$ and $V_{o\,4}$. Care has been taken to minimize switching plops. Also total harmonic distortion and random noise are considerably reduced.

Identification

The pilot signal is fed via an external RC high-pass filter and single tuned LC band-pass filter to the input of a gain controlled amplifier. The external LC band-pass filter in combination with the external RC high-pass filter should have a loaded Q-factor of about 40 to 50 to ensure the highest identification sensitivity. By using a fixed coil (±5%) to save the alignment (see Fig.2), a Q-factor of about 12 is proposed. This may cause a loss in sensitivity of about 2 to 3 dB. A digital PLL circuit generates a reference carrier, which is synchronized with the pilot carrier.

This reference carrier and the gain controlled pilot signal are fed to the AM-synchronous demodulator. The demodulator detects the identification signal, which is fed through a low-pass filter with external capacitor C_{LP} (pin 3) to a Schmitt-trigger for pulse shaping and suppression of low level spurious signal components. This is a measure against mis-identification.

The identification signal is amplified and fed through an AGC low-pass filter with external capacitor C_{AGC} (pin 2) to obtain the AGC voltage for controlling the gain of the pilot signal amplifier.

The identification stages consist of two digital PLL circuits with digital synchronous demodulation and digital integrators to generate the stereo or dual sound identification bits which can be read out via the I²C-bus.

A 10 MHz quartz crystal oscillator provides the reference clock frequency. The corresponding detection bandwidth is larger than ±50 Hz for the pilot carrier signal, so that f_p-variations from the transmitter can be tracked in case of missing synchronisation with the horizontal frequency f_H. However the detection bandwidth for the identification signal is made small (approximately ±1 Hz) to reduce mis-identification.

Figure 2 shows an example of the alignment-free f_p band-pass filter. To achieve the required Q_L of approximately 12, the Q_0 at f_p of the coil was chosen to be approximately 25 (effective Q_0 including PCB influence). Using coils with other Q_0, the RC-network (R_{FP}, C_{FP}) has to be adapted accordingly. It is assumed that the loss factor tanδ of the resonance capacitor is ≤0.01 at f_p.

Copper areas under the coil might influence the loaded Q and have to be taken into account. Care has also to be taken in environments with strong magnetic fields when using coils without magnetic shielding.

I²C-bus transceiver

The complete IC is controlled by a microcomputer via the I²C-bus. The built-in I²C-bus transceiver transmits the identification result to the I²C-bus and receives the control data for the source selector and level control. The I²C-bus protocol is given in Tables 2 to 12 respectively.

The data transmission between the microcontroller and the other I²C-bus controlled ICs is not disturbed, when the supply voltage of the TDA9840 is not connected or when powering up or down. Finally, a Schmitt-trigger is built-in the SDA/SCL interface to suppress spikes from the I²C-bus.

Power supply

The different supply voltages and currents required for the analog and digital circuits are derived from an internal band-gap reference circuit. The AF reference voltage is $\frac{1}{2}V_P$. For a fast setting to $\frac{1}{2}V_P$ an internal start-up circuit is added. A good ripple rejection is achieved with the external capacitor C_{ref} = 100 µF/16 V in conjunction with the high ohmic input of the $\frac{1}{2}V_P$ pin (pin 6). Additional DC-load on this pin is prohibited.

Power-on reset

When a power-on reset is activated by switching on the supply voltage or because of a supply voltage breakdown, the 117/274 Hz DPLL, the 117/274 Hz integrator and the registers will be reset. Both AF channels (Main and SCART) are muted.

Fast mode / test mode

The TDA9840 has a fast mode (test mode) to reduce the integration time of the 117/274 Hz integrator from approximately 1 to 0.5 s.

ESD protection

All pins are ESD protected. The protection circuits represent the latest state of the art.

Internal circuit

The internal pin loading diagram is given in Fig.7.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage (pin 18)		−0.3	10	V
V_i	voltage at pins 1 and 20		−0.3	5.5	V
V_i	voltage at pins 2 to 15, 17 and 19		−0.3	V_P	V
T_{stg}	storage temperature		−25	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C
V_{esd}	electrostatic handling for all pins	note 1	−	±300	V

Note

1. Charge device model class B: discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	DIP20	73	K/W
	SO20	90	K/W

CHARACTERISTICS

V_P = 5 V; T_{amb} = +25 °C; nominal input signal $V_{i\,1,2}$ = 0.25 V RMS value (FM: 54% modulation is equivalent to Δf = ±27 kHz); nominal input signal $V_{i\,3,4}$ = 0.5 V RMS value (AM: m = 0.54); nominal output signal $V_{o\,1,2,3,4}$ = 0.5 V RMS value; f_{AF} = 1 kHz; $V_{i\,pil}$ = 16 mV RMS value; f_{pil} = 54.6875 kHz (identification frequencies: stereo = 117.48 Hz, dual = 274.12 Hz), 50 µs pre-emphasis; noise measurement in accordance with *"CCIR468-3"*, working oscillator frequency f_{osc} = 10.008 MHz; currents into the IC positive; measured in test circuit according to Fig.5, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 18)		4.5	5	8.8	V
I_P	supply current (pin 18)		15.5	16.5	20.5	mA
P_{tot}	total power dissipation		69.75	82.5	180.4	mW
$V_{n(DC)}$	DC voltage (pins 7 to 15 and 17)		$\frac{1}{2}V_P - 0.1$	$\frac{1}{2}V_P$	$\frac{1}{2}V_P + 0.1$	V
$V_{ref(DC)}$	DC reference voltage (pin 6)		$\frac{1}{2}V_P - 0.1$	$\frac{1}{2}V_P$	$\frac{1}{2}V_P + 0.1$	V
$I_{L(DC)}$	DC leakage current (pin 6)		–	–	±1	µA
AF Inputs; $V_{i\,1}$ and $V_{i\,2}$ (pins 7 and 8)						
$V_{i(rms)}$	nominal input signal voltage (RMS value)	54% modulation	–	0.25	–	V
$V_{i(rms)}$	clipping voltage level (RMS value)	THD ≤ 1.5%; note 1				
		V_P = 5 V	0.625	0.715	–	V
		V_P = 8 V	1.050	1.200	–	V
		THD ≤ 1.5%; note 2				
		V_P = 5 V	0.780	0.900	–	V
		V_P = 8 V	1.300	1.500	–	V
G_v	AF signal voltage gain	$G = V_o/V_i$; note 3	5	6	7	dB
ΔG_v (V_{o1})	stereo control range	only at pin 7	+2.4	+2.5	+2.6	dB
			−2.3	−2.4	−2.5	dB
	nominal step	maximum 49 steps	–	0.1	–	dB
ΔG_v (V_{o2})	level control range	only at pin 8	+2.4	+2.5	+2.6	dB
			−1.9	−2.0	−2.1	dB
	nominal step	maximum 9 steps	–	0.5	–	dB
R_i	input resistance		40	50	60	kΩ
R_{deem}	internal de-emphasis resistor (pins 15 and 17)	see Fig.4	4.25	5.0	5.75	kΩ
Additional AF input pin (pins 9 and 10)						
$V_{i(rms)}$	nominal input signal voltage (RMS value)	54% modulation	–	0.5	–	V
$V_{i(rms)}$	clipping voltage level (RMS value)	THD ≤ 1.5%				
		V_P = 5 V	1.25	1.40	–	V
		V_P = 8 V	2.10	2.35		V
G_v	AF signal voltage gain	$G = V_o/V_i$; note 3	−1	0	1	dB
R_i	input resistance		40	50	60	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AF outputs (pins 11 to 14)						
$V_{o(rms)}$	nominal output signal voltage (RMS value)	THD ≤ 0.3%; 54% modulation	–	0.5	–	V
$V_{o(rms)}$	clipping voltage level (RMS value)	THD ≤ 1.5%				
		V_P = 5 V	1.4	1.6	–	V
		V_P = 8 V	2.4	2.65	–	V
R_o	output resistance		150	250	350	Ω
C_L	load capacitor on output		–	–	1.5	nF
R_L	load resistor on output (AC-coupled)		10	–	–	kΩ
B	frequency response (bandwidth)	f_i = 40 to 20000 Hz; note 4	−0.5	–	+0.5	dB
$B_{-3\ dB}$	frequency response	−3 dB; note 4	300	350	400	kHz
THD	total harmonic distortion	note 3	–	0.2	0.3	%
S/N(W)	weighted signal-to-noise ratio	*"CCIR468-3"* (quasi-peak)	66	75	–	dB
α_{cr}	crosstalk attenuation for	notes 3 and 5				
	DUAL	$\lvert Z_s \rvert$ ≤1 kΩ	70	75	–	dB
	STEREO	$\lvert Z_s \rvert$ ≤1 kΩ	40	45	–	dB
α_{mute}	mute attenuation	$\lvert Z_s \rvert$ ≤1 kΩ; note 3	76	80	–	dB
ΔV_{DC}	change of DC level output voltage between any two modes of operation	after switching	–	–	±10	mV
PSRR	power supply ripple rejection	f_r = 70 Hz; see Fig.6	50	65	–	dB
$I_{O(DC)}$	DC output current		–	–	±20	µA
α_{I2C}	noise from I²C-bus	note 6	–	90	80	dB
10 MHz crystal oscillator (pin 19)						
f_r	series resonant frequency of crystal (fundamental mode)	C_L = 20 pF	9.995	10.008	10.021	MHz
f_w	working oscillator frequency (running in parallel resonance mode)	over operating temperature range including ageing and influence of drive circuit	9.988	10.008	10.028	MHz
R_r	equivalent crystal series resistance	even at extremely low drive level (<1 pW) over operating temperature range with C_0 = 6 pF	–	60	200	Ω
R_n	crystal series resistance of unwanted mode		2 × R_r	–	–	Ω
C_0	crystal parallel capacitance	with R_r ≤ 100 Ω	–	6	10	pF
C_1	crystal motional capacitance		–	25	50	fF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_{XTAL}	level of drive in operation		–	–	5	μW
$V_{OSC(p-p)}$	oscillator operating voltage (peak-to-peak value)		500	550	600	mV
Pilot processing						
$V_{i\ pil(rms)}$	pilot input voltage level at pin 5 (RMS value)	unmodulated	5	–	100	mV
$R_{i\ pil}$	pilot input resistance		500	1000	–	kΩ
m	modulation depth	AM	25	50	75	%
Δf_{pil}	pilot PLL pull-in frequency range (referred to f_{pil} = 54.6875 kHz)	f_{ω} = 9.988 MHz				
		lower side	−405	–	−405	Hz
		upper side	192	–	192	Hz
		f_{ω} = 10.008 MHz				
		lower side	−296	–	−296	Hz
		upper side	302	–	302	Hz
		f_{ω} = 10.028 MHz				
		lower side	−188	–	−188	Hz
		upper side	411	–	411	Hz
t_{pil}	pilot PLL pull-in time		0	–	1.7	ms
f_{LP}	low-pass frequency response	−3 dB	450	600	750	Hz
R_3	low-pass output resistance		18.75	25	31.25	kΩ
$V_{4(rms)}$	identification threshold voltage (RMS value)		–	–	70	mV
Q_L	loaded quality factor of resonance circuit	high sensitivity	40	–	50	
	loaded quality factor of resonance circuit with fixed coil	sensitivity loss 2 to 3 dB; see Fig.2	–	12	–	
$t_{acqui\ AGC}$	AGC acquisition time	$V_{i\ pil(rms)}$ switched from 0 to 100 mV RMS value	–	–	0.1	s
Identification (internal functions)						
$V_{i\ tuner}$	identification voltage sensitivity (pin 5)	note 7	–	28	–	dBμV
C/N	pilot carrier-to-noise ratio for start of identification	note 8	–	33	–	dB/Hz
H	hysteresis	note 7	–	–	2	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{det}	pull-in frequency range of identification PLL (referred to $f_{det\ STEREO}$ = 117.48 Hz and $f_{det\ DUAL}$ = 274.12 Hz)	normal mode lower side				
		STEREO	−0.38	–	−0.38	Hz
		DUAL	−0.69	–	−0.69	Hz
		normal mode upper side				
		STEREO	0.69	–	0.69	Hz
		DUAL	0.69	–	0.69	Hz
		fast mode lower side				
		STEREO	−0.89	–	−0.89	Hz
		DUAL	−2.05	–	−2.05	Hz
		fast mode upper side				
		STEREO	1.15	–	1.15	Hz
		DUAL	2.05	–	2.05	Hz
t_{det}	pull-in time of identification PLL (referred to $f_{det\ STEREO}$ = 117.48 Hz and $f_{det\ DUAL}$ = 274.12 Hz)	normal mode				
		STEREO	0	–	1.35	s
		DUAL	0	–	0.72	s
		fast mode				
		STEREO	0	–	0.57	s
		DUAL	0	–	0.25	s
f_{ident}	identification window frequency width (referred to $f_{det\ STEREO}$ = 117.48 Hz and $f_{det\ DUAL}$ = 274.12 Hz)	normal mode; note 9				
		STEREO	2.0	–	2.0	Hz
		DUAL	2.3	–	2.3	Hz
		fast mode; note 9				
		STEREO	3.8	–	3.8	Hz
		DUAL	5.8	–	5.8	Hz
t_{integr}	integrator time constant	normal mode	0.94	–	0.94	s
		fast mode	0.47	–	0.47	s
$t_{ident(on)}$	total identification time on	normal mode; note 10				
		STEREO	0.35	–	2.3	s
		DUAL	0.35	–	2.0	s
		fast mode; note 10				
		STEREO	0.175	–	1.1	s
		DUAL	0.175	–	1.0	s
$t_{ident(off)}$	total identification time off	normal mode; note 11				
		STEREO	0.6	–	1.6	s
		DUAL	0.6	–	1.6	s
		fast mode; note 11				
		STEREO	0.3	–	0.8	s
		DUAL	0.3	–	0.8	s

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus transceiver (pins 1 and 20)						
f_{CI}	clock frequency		0	–	100	kHz
I²C-bus: SCL (pin 20)						
V_{IL}	LOW level input voltage		−0.3	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	5.5	V
t_{low}	timing LOW period		4.7	–	–	µs
t_{high}	timing HIGH period		4.0	–	–	µs
t_r	rise time		–	–	1	µs
t_f	fall time		–	–	0.3	µs
I_{IL}	LOW level input current		–	–	−10	µA
I_{IH}	HIGH level input current		–	–	10	µA
I²C-bus: SDA (pin 1)						
V_{IL}	LOW level input voltage		−0.3	–	1.5	V
V_{IH}	HIGH level input voltage		3.0	–	5.5	V
t_r	rise time		–	–	1	µs
t_f	fall time		–	–	0.3	µs
t_{su}	data set-up time		0.25	–	–	µs
I_{IL}	LOW level input current		–	–	−10	µA
I_{OL}	LOW level output current		−3	–	–	mA
I_{IH}	HIGH level input current		–	–	10	µA

Notes

1. Input control amplifiers with $\Delta G_v = 0$ dB.
2. Input control amplifiers with $\Delta G_v = -2$ dB.
3. $V_o = 0.5$ V RMS value; f = 1 kHz; input control amplifiers with $\Delta G_v = 0$ dB.
4. Without de-emphasis capacitors with respect to nominal gain.
5. In dual mode: A (B)-signal into B (A) channel.
   In stereo mode: R-signal into left channel; L-signal = 0.
6. Test procedure tbf (same as TDA9855).
7. Tuner input signal, measured with PCALH reference front end (½EMF, 75 Ω, 2T/20T/white bar, 100% video) and $PC/SC_1 = 13$ dB; $PC/SC_2 = 20$ dB. The pilot band-pass has to be aligned.
8. Bandwidth of the pilot BP-filter $B_{-3\,dB} = 1.2$ kHz. $V_{i\,2}$ input driven with identification-modulated pilot carrier and white noise.
9. Identification window is defined as total pull-in frequency range (lower plus upper side) of identification PLL (steady detection) plus window increase due to integrator (fluctuating detection).
10. The maximum total system identification time ON is equal to $t_{ident(on)}$ plus $t_{acqui\ AGC}$ plus $t_{I^2C\ read\text{-}out}$.
11. The maximum total system identification time OFF is equal to $t_{ident(off)}$ plus $t_{I^2C\ read\text{-}out}$.

I²C-BUS PROTOCOL FOR THE TV AND VTR STEREO/DUAL SOUND PROCESSOR TDA9840

The TDA9840 has an I²C-bus interface with five registers: status, test, switch, level and stereo adjustment register controlled by a microcontroller via I²C-bus. The status register can be read and the other registers are write registers. The status byte represents the transmitter status detected by the identification circuit and the power-on reset status. The switch register controls the source selectors of the AF signal part, and the level and stereo adjustment register set the input level and stereo adjustment stage. Additionally, a test register is built-in to reduce the detection time of the identification circuit (test mode, fast mode respectively).

I²C-bus transceiver and data-handling (bus specification)

The TDA9840 is controlled by a microcomputer via the bidirectional 2-line I²C-bus. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

When the bus is free, both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change, when the clock signal on the SCL line is LOW. The set-up and hold times are specified in the Chapter "Characteristics"

A HIGH-to-LOW transition of the SDA line, while SCL is HIGH, is defined as the start condition. A LOW-to-HIGH transition of the SDA line, while SCL is HIGH, is defined as the stop condition. The bus transceiver will be reset on the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

Data format transmitter mode

For the data transmission no subaddress is to be transmitted, because there is only one read register implemented. So the total number of bytes reduces from three to two. The second byte represents the status of the IC.

Status register (see Table 4)

The bit D7 (PONRES) represents the status of the IC and indicates whether the power-on reset was activated by switching-on the supply voltage or a supply voltage breakdown.

If so, the I²C-bus transceiver, the digital PLLs and integrators are initialized and the PONRES bit is set to HIGH. After a successful reading of the status register, the bit D7 will be reset to LOW.

The bits D5 and D6 represent the transmitter status detected by the identification circuit (stereo, dual or mono transmission). The other bits are set to 0 (default).

Data format for the receiver

Table 1 Registers for receiver mode (see Table 6)

REGISTER	VALUE
Switch register	$(00)_{HEX}$
Port register	$(01)_{HEX}$ (without function)
Level adjustment register	$(02)_{HEX}$
Stereo adjustment register	$(03)_{HEX}$
Test register	$(04)_{HEX}$

The port register is without function, because this IC has no control ports as TDA8415/6/7. A data byte for the subaddress $(01)_{HEX}$ will not be stored in any register. An acknowledge will be sent to the microcontroller.

The first byte of the data transmission is the slave address and the second byte is the subaddress indicating the data register in which the data shall be stored. Starting from subaddress $(00)_{HEX}$ the n-th data byte will automatically be stored under subaddress n − 1.

All 8 bits of the subaddress are decoded by the device. The subaddresses from $(04)_{HEX}$ to $(FF)_{HEX}$ are forbidden for the user. If the I²C-bus transceiver receives subaddresses from $(05)_{HEX}$ to $(FF)_{HEX}$, no acknowledge will be sent back to the microcontroller.

Switch register

The source selector is controlled by the switch register. Table 7 shows the modes of operation. Note, that in the event of the external operation mode, no further selection is possible.

Level adjustment register

The information about the level adjustment of the AF channel $V_{i\,2}$ (pin 8) is stored in the level adjustment register (see Table 10). There are 10 steps (positions) of the AF level adjustment stage. The level range is from 2.5 dB up to −2.0 dB in 0.5 dB steps.

After a power-on reset, the data byte of the level adjustment register will be set to $(00)_{HEX}$: 0 dB gain at the AF input $V_{i\,2}$.

Stereo adjustment register

The information about the stereo adjustment of the AF channel $V_{i\,1}$ (pin 7) is stored in the stereo adjustment register (see Table 11). There are 50 steps (positions) of the AF stereo adjustment stage. The stereo range is from 2.5 dB up to −2.4 dB in 0.1 dB steps.

After a power-on reset, the data byte of the stereo adjustment register will be set to $(00)_{HEX}$: 0 dB gain at the AF input $V_{i\,1}$.

Test register (also used for fast mode)

Table 12 shows the meaning of the test register. The integration time of the integrator is approximately 1 s (normal mode, default). If the data byte of this register is set to HIGH, the integration time is reduced from approximately 1 to approximately 0.5 s (fast mode, test mode). The pull-in ranges of the identification PLLs are changed to:

Stereo: −0.89/+1.15 Hz

Dual: ±2.05 Hz.

If the integration time of the integrator is switched from one mode to the other (i.e. from fast mode/test mode to normal mode), the status register bits D5 and D6 might set to zero internally (MONO). Therefore, the previous status register information has to be stored by the microcontroller until the transmitter status is detected again by the identification circuit (now in the new mode) the first time.

The data byte of the test register can be reset in two different ways to $(00)_{HEX}$: integration time approximately 1 s, normal mode:

- after a power-on reset, for instance by switching the power supply V_p off and on again
- data transmission via I²C-bus for the test register (see Table 12).

Level and stereo adjustment

For the level and stereo adjustment of both AF channels $V_{i\,1}$ and $V_{i\,2}$, the following procedure will be recommended.

Level adjustment of the AF channel $V_{i\,2}$

- Feeds AF signal at the input $V_{i\,2}$
- Sets the data byte of the switch register (dual mode) to $(1A)_{HEX}$
- Measures the signal at the outputs $V_{o\,2}$ or $V_{o\,4}$
- Adjusts the output level with the level adjustment register.

Stereo adjustment of the AF channel $V_{i\,1}$

- Feeds AF stereo signals at the inputs $V_{i\,1}$ ((L+R)/2) and $V_{i\,2}$ (R)
- Sets the data byte of the switch register (stereo mode) to $(2A)_{HEX}$
- Measures the crosstalk attenuation between $V_{o\,1}$ and $V_{o\,2}$ or $V_{o\,3}$ and $V_{o\,4}$
- Adjusts the crosstalk attenuation with the stereo adjustment register.

During the stereo adjustment the data byte of the level adjustment register does not change.

After the level and stereo adjustment, the bytes of the level and stereo adjustment register must be stored by the microcontroller in a memory. (To avoid mis-adjustment it would be wise to compare the stored bytes with the proper adjustment bytes). If the PONRES bit of the status register will be set to HIGH (see status register) the data bytes for these both registers must be sent out of the memory to the TDA9840 via I²C-bus. Also the data byte of the switch register (see Table 7) must be changed, because the AF outputs are muted.

I²C-BUS FORMAT

X is the read/write control bit; X = 0, order to write (the circuit is slave receiver); X = 1, order to read (the circuit is slave transmitter). If more than 1 byte of DATA is transmitted, then auto-increment of the significant subaddress is performed.

Table 2 I²C-bus; SLAVE ADDRESS/SUBADDRESS/DATA format

S	SLAVE ADDRESS	A	SUBADDRESS	A	DATA	P

Table 3 Explanation of Table 2

BIT	FUNCTION
S	start condition
SLAVE ADDRESS	1000 010X
A	acknowledge, generated by the slave
SUBADDRESS	dual sound A/B
DATA	data byte, see Table 6
P	stop condition

Table 4 I²C-bus; SLAVE ADDRESS/DATA to read the status byte (X = 1 in the address byte)

FUNCTION	SLAVE ADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte	1000 0101	PONRES	ST	DS	0	0	0	0	0

Table 5 Explanation of Table 4

BIT	FUNCTION
PONRES = 0	after a successful reading of the status register
PONRES = 1	after power-on reset or after supply breakdown
ST = 0; DS = 0	MONO sound identified
ST = 0; DS = 1	DUAL sound identified
ST = 1; DS = 0	STEREO sound identified
ST = 1; DS = 1	incorrect identification

Table 6 I²C-bus; SUBADDRESS/DATA for writing (X = 0 in the address byte)

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Switching	0000 0000	0	SW6	SW5	SW4	SW3	SW2	SW1	SW0
Without function (note 1)	0000 0001	0	0	0	0	0	0	0	0
Level adjustment	0000 0010	0	0	0	0	LV3	LV2	LV1	LV0
Stereo adjustment	0000 0011	0	0	ST5	ST4	ST3	ST2	ST1	ST0

Note

1. This byte is acknowledged by the TDA9840.

Function of the bits:

- SW6 to SW0 input and output AF selection; see Table 7
- LV3 to LV0 level adjustment; see Table 9
- ST5 to ST0 stereo adjustment; see Table 11.

Table 7 Data byte to select AF inputs and AF outputs [subaddress $(00)_{HEX}$]

TRANSMISSION MODE		INPUT SIGNAL				OUTPUT SIGNAL				DATA								
		ST/DS/M		EXT		MAIN		SCART										
		V_{i1} PIN 7	V_{i2} PIN 8	V_{i3} PIN 9	V_{i4} PIN 10	V_{o1} PIN 14	V_{o2} PIN 13	V_{o3} PIN 12	V_{o4} PIN 11	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Sound mute	–	–	–	–	–	no signal				0	0	0	0	0	0	0	0	00
MONO	M	M	–	–	–	M	M	M	M	0	0	0	1	0	0	0	0	10
STEREO	ST	S	R	–	–	S	S	S	S	0	0	0	1	0	0	0	0	10
		S	R	–	–	L	R	L	R	0	0	1	0	1	0	1	0	2A
DUAL	DS	A	B	–	–	A	B	A	A	0	0	0	1	0	0	1	0	12
		A	B	–	–	A	B	A	B	0	0	0	1	1	0	1	0	1A
		A	B	–	–	A	B	B	A	0	0	0	1	0	1	1	0	16
		A	B	–	–	A	B	B	B	0	0	0	1	1	1	1	0	1E
External	–	–	–	C	D	C	D	C	D	0	1	1	1	1	0	1	0	7A

Table 8 Explanation of Table 7

SIGNAL	DESCRIPTION
R	right
L	left
S	$\frac{(L+R)}{2}$
A and B	dual sound A/B

SIGNAL	DESCRIPTION
C	NICAM or AM sound (standard L)
D	NICAM
M	mono sound
DS	dual sound
ST	stereo sound

Table 9 AF switch configuration

INPUT		OUTPUT	
TRANSMITTER STATUS	**SIGNAL**	**MAIN**	**SCART**
MONO	M	M	M
		M	M
STEREO	L	L or M	L or M
	R	R or M	R or M
DUAL	A	A	A or B
	B	B	A or B
External	C	C	C
	D	D	D

Table 10 Data byte to select level adjustment [subaddress $(02)_{HEX}$]

ΔG_V (dB)	DATA								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
+2.5	0	0	0	0	1	1	0	1	0D
+2.0	0	0	0	0	1	1	0	0	0C
+1.5	0	0	0	0	1	0	1	1	0B
+1.0	0	0	0	0	1	0	1	0	0A
+0.5	0	0	0	0	1	0	0	1	09
0	0	0	0	0	0	0	0	0	00
−0.5	0	0	0	0	0	0	0	1	01
−1.0	0	0	0	0	0	0	1	0	02
−1.5	0	0	0	0	0	0	1	1	03
−2.0	0	0	0	0	0	1	0	0	04

Table 11 Data byte to select stereo adjustment (subaddress $(03)_{HEX}$)

ΔG_V (dB)	DATA								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
+2.5	0	0	1	1	1	0	0	1	39
+2.4	0	0	1	1	1	0	0	0	38
+2.3	0	0	1	1	0	1	1	1	37
+2.2	0	0	1	1	0	1	1	0	36
+2.1	0	0	1	1	0	1	0	1	35
+2.0	0	0	1	1	0	1	0	0	34
+1.9	0	0	1	1	0	0	1	1	33
+1.8	0	0	1	1	0	0	1	0	32
+1.7	0	0	1	1	0	0	0	1	31
+1.6	0	0	1	1	0	0	0	0	30
+1.5	0	0	1	0	1	1	1	1	2F
+1.4	0	0	1	0	1	1	1	0	2E
+1.3	0	0	1	0	1	1	0	1	2D
+1.2	0	0	1	0	1	1	0	0	2C
+1.1	0	0	1	0	1	0	1	1	2B
+1.0	0	0	1	0	1	0	1	0	2A
+0.9	0	0	1	0	1	0	0	1	29
+0.8	0	0	1	0	1	0	0	0	28
+0.7	0	0	1	0	0	1	1	1	27
+0.6	0	0	1	0	0	1	1	0	26
+0.5	0	0	1	0	0	1	0	1	25
+0.4	0	0	1	0	0	1	0	0	24
+0.3	0	0	1	0	0	0	1	1	23
+0.2	0	0	1	0	0	0	1	0	22
+0.1	0	0	1	0	0	0	0	1	21

ΔG_V (dB)	DATA								
	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0	0	0	0	0	0	0	0	0	00
−0.1	0	0	0	0	0	0	0	1	01
−0.2	0	0	0	0	0	0	1	0	02
−0.3	0	0	0	0	0	0	1	1	03
−0.4	0	0	0	0	0	1	0	0	04
−0.5	0	0	0	0	0	1	0	1	05
−0.6	0	0	0	0	0	1	1	0	06
−0.7	0	0	0	0	0	1	1	1	07
−0.8	0	0	0	0	1	0	0	0	08
−0.9	0	0	0	0	1	0	0	1	09
−1.0	0	0	0	0	1	0	1	0	0A
−1.1	0	0	0	0	1	0	1	1	0B
−1.2	0	0	0	0	1	1	0	0	0C
−1.3	0	0	0	0	1	1	0	1	0D
−1.4	0	0	0	0	1	1	1	0	0E
−1.5	0	0	0	0	1	1	1	1	0F
−1.6	0	0	0	1	0	0	0	0	10
−1.7	0	0	0	1	0	0	0	1	11
−1.8	0	0	0	1	0	0	1	0	12
−1.9	0	0	0	1	0	0	1	1	13
−2.0	0	0	0	1	0	1	0	0	14
−2.1	0	0	0	1	0	1	0	1	15
−2.2	0	0	0	1	0	1	1	0	16
−2.3	0	0	0	1	0	1	1	1	17
−2.4	0	0	0	1	1	0	0	0	18

Table 12 Data byte to select integration time [subaddress $(04)_{HEX}$]

FUNCTION	SUBADDRESS	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Test byte	0000 0100	X	X	X	X	X	X	INTFU	INT1SN

Function of the bits:

- INTFU = 0 integrator function disabled
- INTFU = 1 integrator function enabled
- INT1SN = 0 integration time approximately 1 s (default)
- INT1SN = 1integration time approximately 0.5 s.

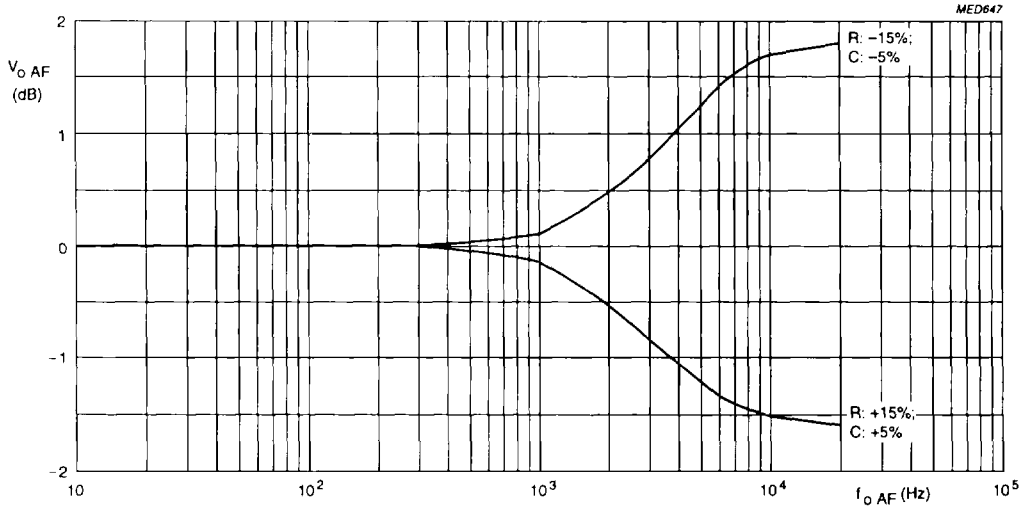


Fig.4 Tolerance scheme of AF frequency response; de-emphasis with C_{D1}, C_{D2} = 10 nF (±5%), $R_{internal}$ = 5 kΩ (±15%).

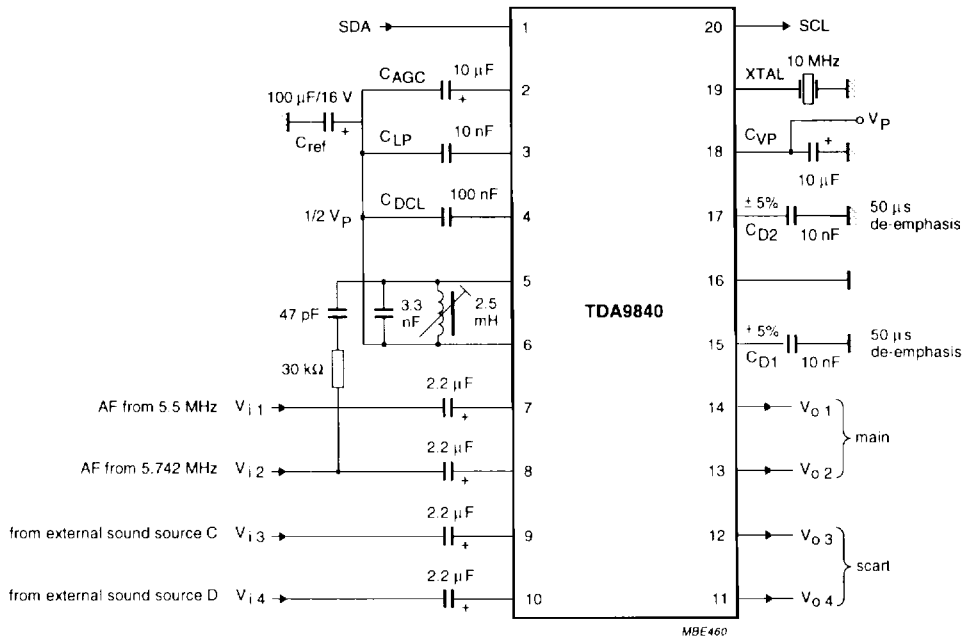


Fig.5 Test circuit of the stereo decoder TDA9840.

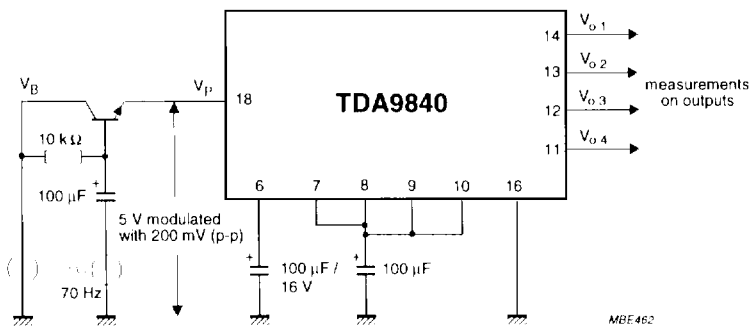
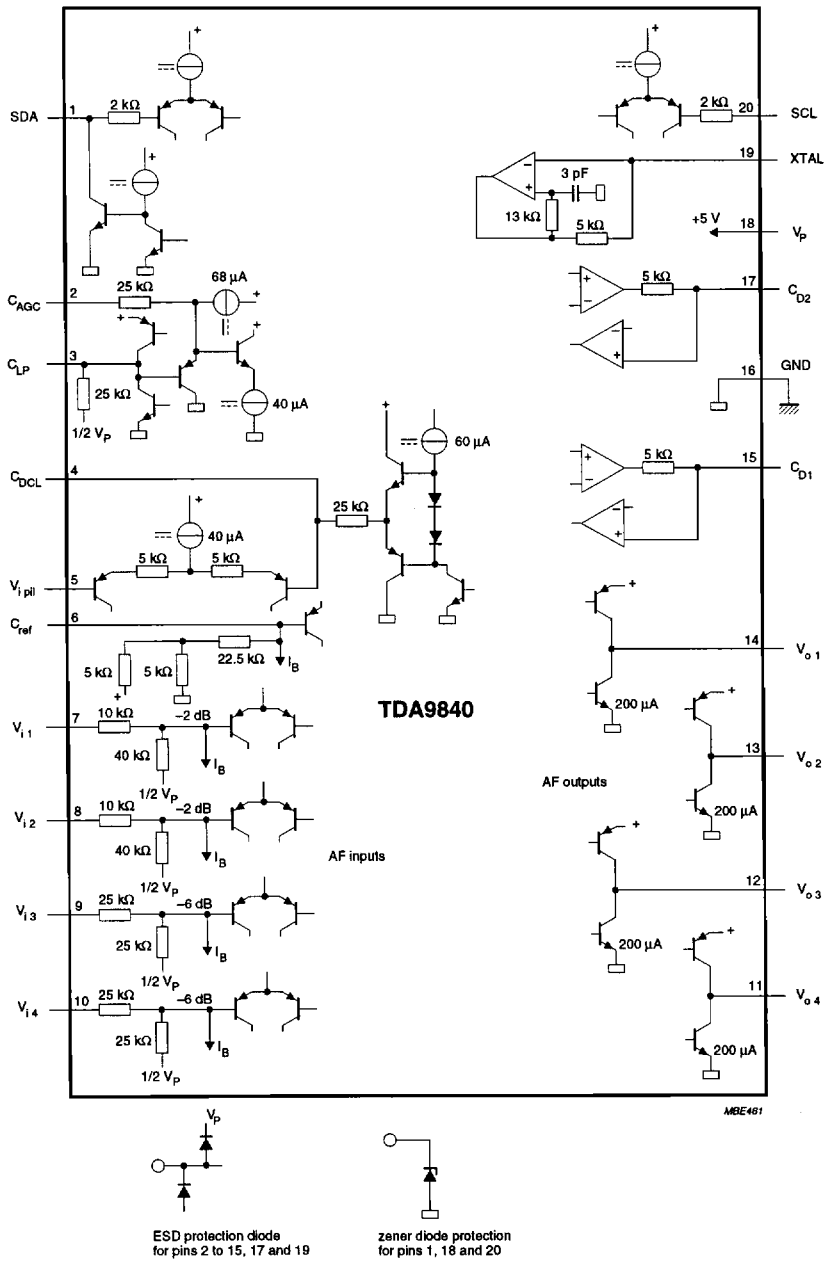


Fig.6 Test circuit for measurement of ripple rejection.

INTERNAL CIRCUITRY



ESD protection diode for pins 2 to 15, 17 and 19

zener diode protection for pins 1, 18 and 20

Fig.7 Internal circuits.