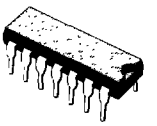
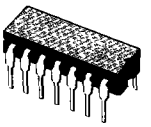
4-BIT SHIFT REGISTER WITH 3-STATE OUTPUTS

- FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS
- NEGATIVE EDGE-TRIGGERED CLOCK INPUT
- PARALLEL ENABLE MODE CONTROL INPUT
- 3-STATE BUSSABLE OUTPUT BUFFERS
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LS295A D1 T74LS295A C1
T74LS295A B1 T74LS295A M1

DESCRIPTION

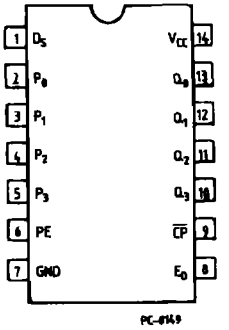
The T74LS295A is a 4-Bit Shift Register with serial and parallel synchronous operating modes, independent 3-state output buffers. The Parallel Enable input (PE) controls the shift-right or parallel load operation. All data transfer and shifting occur synchronously with the HIGH to LOW clock transition.

The 3-State output buffers are controlled by an active HIGH Output Enable input (EO).

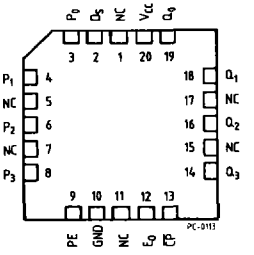
Disabling the output buffers does not affect the shifting or loading of input data, but it does inhibit serial expansion.

The LS295A is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all TTL families.

PIN CONNECTION (top view)
DUAL IN LINE



CHIP CARRIER

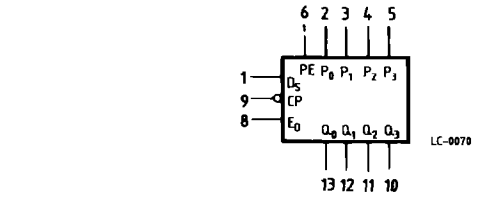


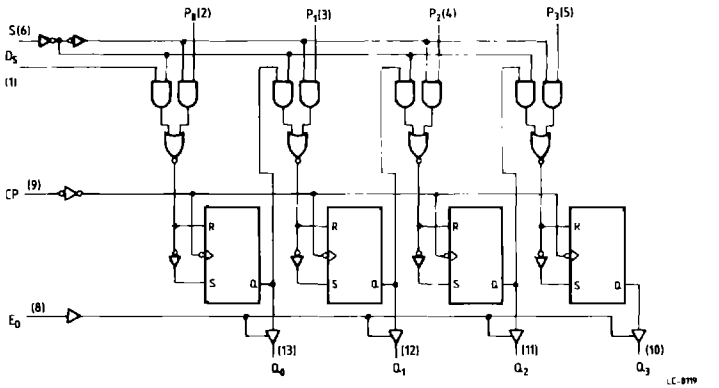
NC = No Internal Connection

PIN NAMES

PE	PARALLEL ENABLE INPUT
D_S	SERIAL DATA INPUT
P_0-P_3	PARALLEL DATA INPUTS
$\underline{E_0}$	OUTPUT ENABLE INPUT
$\overline{CP}$	CLOCK PULSE (active LOW going edge) INPUT
Q_0-Q_3	3-STATE OUTPUTS

LOGIC SYMBOL AND LOGIC DIAGRAM





V_{CC} = Pin 16
GND = Pin 7
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, Into Inputs	– 0.5 to 30	mA
I_O	Output Current, Into Outputs	60	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS295AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = Package type

TRUTH TABLE - PRESENT OUTPUT STATES AND MODE SELECTION

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS*			
	PE	$\overline{CP}$	D_S	P_n	Q_0	Q_1	Q_2	Q_3
Shift Right	l	⌐	l	X	L	q_0	q_1	q_2
	l	⌐	h	X	H	q_0	q_1	q_2
Parallel Load	h	⌐	X	P_n	P_0	P_1	P_2	P_3

* The indicated data appears at the Q outputs when E_0 is HIGH. When E_0 is LOW, the indicated data is loaded into the register, but the ouputs are all forced to the high impedance "off" state.

X = Don't Care
L = LOW Voltage Level
H = HIGH Voltage Level

Pn (Qn) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

l = LOW Voltage Level one set-up time prior to the HIGH to LOW clock transition.

h = HIGH Voltage Level one set-up time prior to the HIGH to LOW

FUNCTIONAL DESCRIPTION

The LS295A is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel Data outputs (P_0-P_3) inputs and four parallel 3-State output buffers (Q_0-Q_3). When the parallel Enable (PE) input is HIGH, data is transferred from the Parallel Data Inputs (P_0-P_3) into the register synchronously with the HIGH to LOW transition of the Clock (CP). When the PE is LOW, a HIGH to LOW transition on the clock transfers the serial data on the D_S input to register Q_0, and shifts data from Q_0 to Q_1, Q_1 to Q_2 and Q_2 to Q_3. The input data and parallel enable are fully edge-triggered and must be stable only one set-up time before the HIGH to LOW clock transition.

The 3-State Output buffers are controlled by an active HIGH Output Enable input (E_0). When the E_0 is HIGH, the four register outputs appear at the Q_0-Q_3 outputs. When E_0 is LOW, the outputs are forced to high impedance "off" state. The 3-State output buffers are completely independent of the register operation. i.e. the input transition on the E_0 input do not affect the serial or parallel data transfers of the register. If the outputs are tied together, all but one devices must be in the high impedance state to avoid high currents that would exceed the maximum rating.

Designers should ensure that Output Enable signals to 3-State devices whose outputs are tied together are designed so there is no overlap.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.4	3.4		V_{CC} = MIN, I_{OH} = - 2.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8 mA		V
I_{OZH}	Output Off Current HIGH			20	V_{CC} = MAX, V_{OUT} = 2.7 V		µA
I_{OZL}	Output Off Current LOW			- 20	V_{CC} = MAX, V_{IN} = 0.5 V		µA
I_{IH}	Input HIGH Current			20 0.1	V_{CC} = MAX, V_{IN} = 2.7 V V_{CC} = MAX, V_{IN} = 7.0 V		µA mA
I_{IL}	Input LOW Current			- 0.4	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CC}	Power Supply Current Output HIGH		14	23	V_{CC} = MAX, V_{CP} = ⎍ V_E = 4.5 V		mA
	Power Supply Current Output HIGH		14	25	V_{CC} = MAX, V_{CP} = 0 V, V_E = 0 V		mA

Notes : 1 Conditions for testing, not shown in the table are chosen to guarantee operationunder "worst case" conditions.
2 Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions		Unit
		Min.	Typ.	Max.			
f_{MAX}	Shift Frequency	30	45		Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	MHz
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		24 16	30 26	Fig. 1		ns
t_{PZH}	Output Enable Time to HIGH Level		12	18	Figs. 4, 5	C_L = 15 pF R_L = 2 kΩ	ns
t_{PZL}	Output Enable Time to LOW Level		14	20	Figs. 3, 5		ns
t_{PLZ}	Output Disable Time from LOW Level		17	24	Figs. 3, 5	C_L = 5 pF R_L = 2 kΩ	ns
t_{PHZ}	Output Disable Time from HIGH Level		15	20	Figs. 4, 5		ns
t_W(CP)	Clock Pulse Width	20			Fig. 1	V_{CC} = 5.0 V C_L = 15 pF	ns
t_s(Data)	Set-up Time, Data to Clock	20			Fig. 1		ns
t_s(Data)	Hold Time, Data to Clock	10					ns
t_s(PE)	Set-up Time, PE to Clock	20			Fig. 1		ns
t_h(PE)	Hold Time, PE to Clock	0					ns

DEFINITION OF TERMS

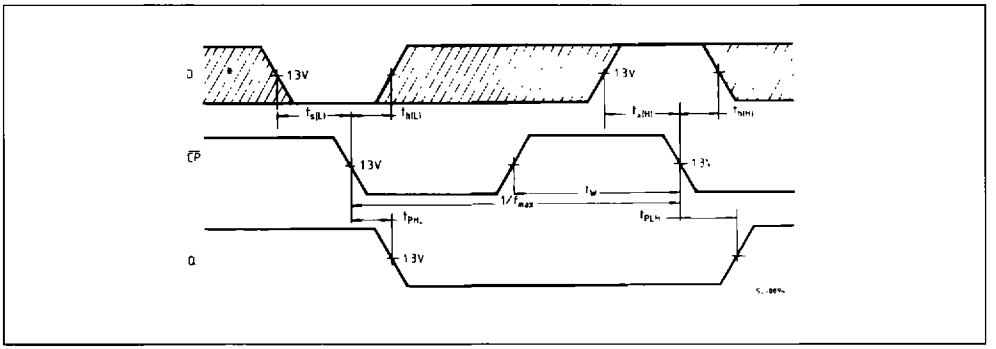
SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH to LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from HIGH to LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH to LOW and still be recognized.

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 1.



* The data input is D_S for PE = LOW and P_n for PE = HIGH.

Figure 2.