4096MB DDR3 – SDRAM unbuffered ECC VLP Mini-UDIMM

244 Pin ECC Mini-UDIMM

SGL04G72C1BB1SA-xxRT

4GByte in FBGA Technology

RoHS compliant

Options:

- Data Rate / Latency — Marking
  DDR3 1333 MT/s CL9 — -CC
  DDR3 1600 MT/s CL11 — -DC
- Module density
  4096MB with 9 dies and 1 ranks
- Standard Grade (T_A) 0°C to 70°C
  (T_C) 0°C to 85°C

Features:

- 244-pin 72-bit DDR3 ECC VLP Mini-UDIMM module
- Module organization: single rank 512M x 72
- V_{DD} = 1.5V ±0.075V, $V_{DD}Q$ 1.5V ±0.075V
- 1.5V I/O (SSTL_15 compatible)
- Fly-by-bus with termination for C/A & CLK bus
- On-board I2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- Gold-contact pad
- This module is fully pin and functional compatible to the JEDEC PC3-10600 DDR3 SDRAM Mini-UDIMM design spec. and JEDEC- Standard MO-244 R/C E. (see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification
  [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]

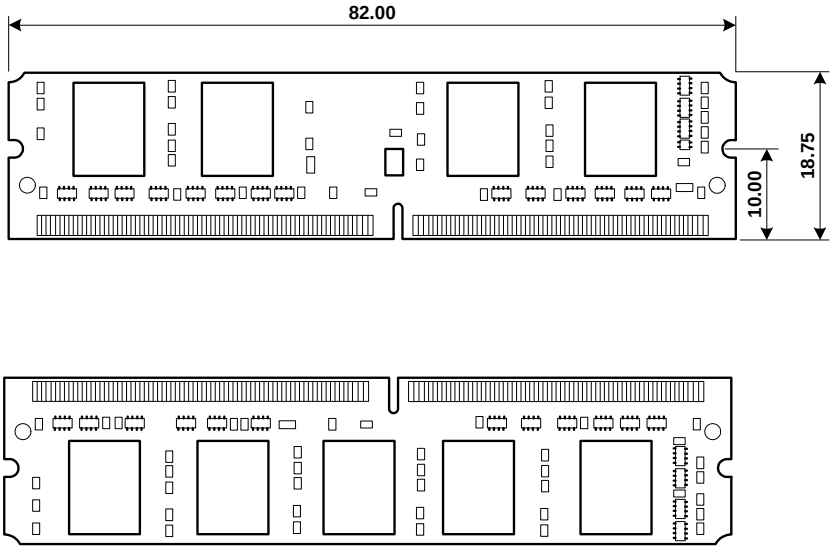
DDR3 - SDRAM component Samsung K4B4G0846B

- 512Mx8 DDR3 SDRAM in PG-TFBGA-78 package
- 8-bit prefetch architecture
- Programmable CAS Latency, CAS Write Latency, Additive Latency, Burst Length and Burst Type.
- On-Die-Termination (ODT) and Dynamic ODT for improved signal integrity.
- Refresh, Self Refresh and Power Down Modes.
- ZQ Calibration for output driver and ODT.
- System Level Timing Calibration Support via Write Leveling and Multi Purpose Register (MPR) Read Pattern.

Environmental Requirements:

- Operating temperature (ambient)
  Standard Grade 0°C to 70°C
- Operating Humidity
  10% to 90% relative humidity, noncondensing
- Operating Pressure
  105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
  -55°C to 100°C
- Storage Humidity
  5% to 95% relative humidity, noncondensing
- Storage Pressure
  1682 PSI (up to 5000 ft.) at 50°C

Figure: mechanical dimensions[1]



[1] if no tolerances specified ± 0.15mm

This Swissbit module is an industry standard 244-pin DDR3 SDRAM ECC Mini-DIMM which is organized as 512Mx72 high speed CMOS memory arrays. The module uses internally configured octal-bank DDR3 SDRAM devices. The module uses double data rate architecture to achieve high-speed operation. DDR3 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR3 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR3 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving “power-down” mode. All inputs and all full drive-strength outputs are SSTL_15 compatible.
The DDR3 SDRAM module uses the serial presence detect (SPD) function implemented via serial EEPROM using the standard I^2C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the SO-UDIMM manufacturer (Swissbit) to identify the module type, the module’s organization and several timing parameters. The second 128 bytes are available to the end user.

Module Configuration

Organization	DDR3 SDRAMs used	Row Addr.	Device Bank Select	Column Addr.	Refresh	Module Bank Select
512M x 72bit	9 x 512M x 8bit (2048Mbit)	16	BA0, BA1, BA2	10	8k	S0#

Module Dimensions in mm
82.00 (long) x 18.75 (high) x 3.80 [max]

Timing Parameters

Part Number	Module Density	Transfer Rate	Memory clock/Data bit rate	Latency
SGL04G72C1BB1SA-CCRT	4096MB	10.6 GB/s	1.5ns / 1333MT/s	9-9-9
SGL04G72C1BB1SA-DCRT	4096MB	12.8 GB/s	1.25ns / 1600MT/s	11-11-11

Label Info

Part Number	JEDEC Module Label
SGL04G72C1BB1SA-CCRT	4GB 1Rx8 PC3-10600W-9-11-E0
SGL04G72C1BB1SA-DCRT	4GB 1Rx8 PC3-12800W-11-11-E0

Pin Name

A0-9, A11 – A15	Address Inputs
A10/AP	Address Input / Autoprecharge Bit
BA0 – BA2	Bank Address Inputs
DQ0 – DQ63	Data Input / Output
CB0 – CB07	ECC check bits
DM0-DM8	Input Data Mask
DQS0 – DQS8	Data Strobe, positive line
DQS0# - DQS8#	Data Strobe, negative line (only used when differential data strobe mode is enabled)
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CKE0	Clock Enable
S0#	Chip Select
CK0	Clock Inputs, positive line
CK0#	Clock Inputs, negative line
Event#	Temperature event: The EVENT# pin is asserted by the temperature sensor when critical
Reset#	Reset signal for DDR3 SDRAMs
V_{DD}	Supply Voltage (1.5V± 0.075V)
V_{REF}DQ	Reference voltage: DQ, DM (VDD/2)
V_{REF}CA	Reference voltage: Control, command, and address (VDD/2)
V_{SS}	Ground
V_{TT}	Termination voltage: Used for control, command, and address (VDD/2).
V_{DDSPD}	Serial EEPROM Positive Power Supply
SCL	Serial Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA2	Presence Detect Address Inputs
ODT0	On-Die Termination
NC	No Connection

Pin Configuration

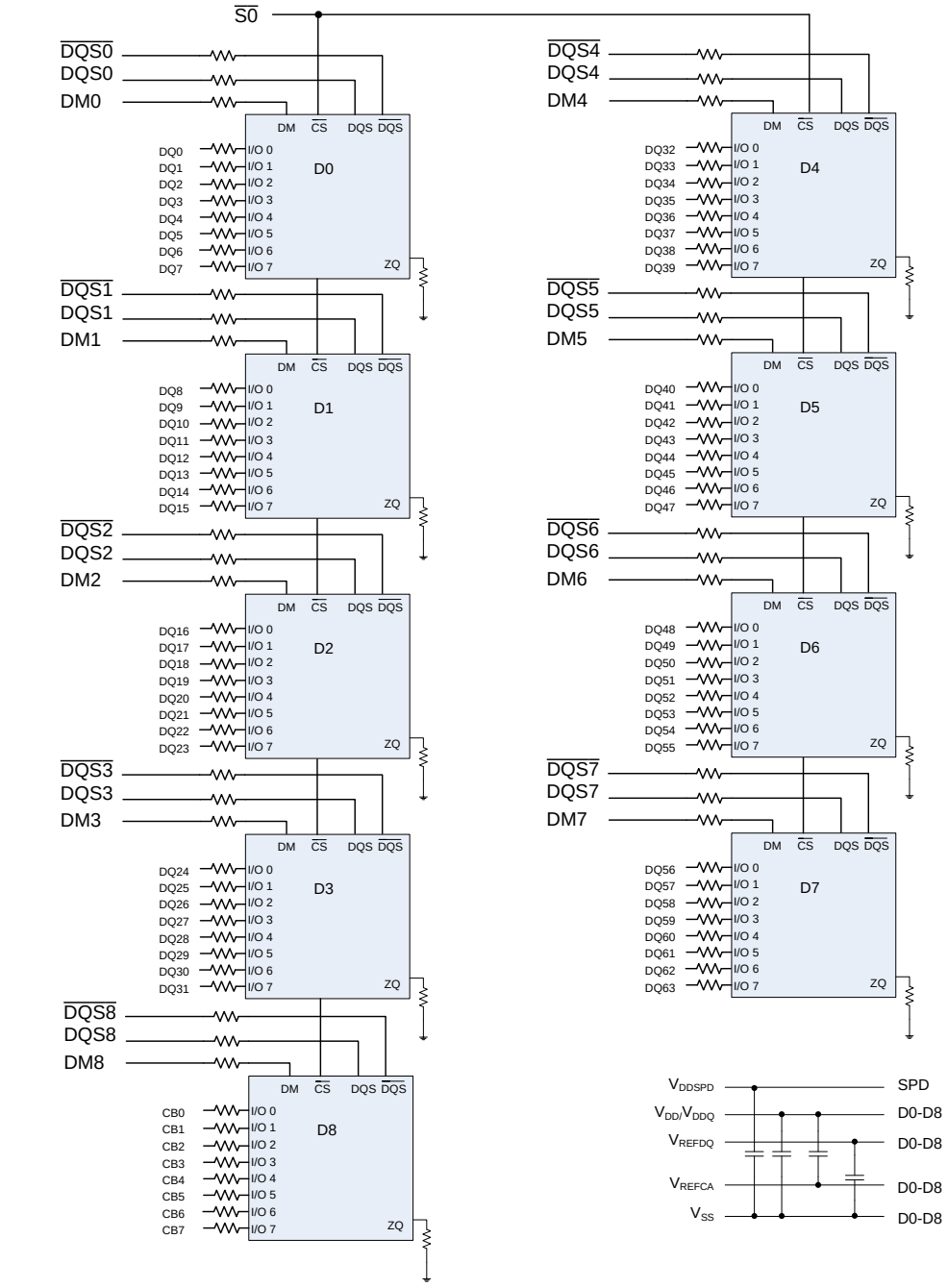
Frontside							
PIN	**Symbol**	**PIN**	**Symbol**	**PIN**	**Symbol**	**PIN**	**Symbol**
1	V_{TT}	31	DQ24	61	V_{DD}	92	DQ40
2	V_{REFDQ}	32	DQ25	62	A2	93	DQ41
3	V_{SS}	33	V_{SS}	63	V_{DD}	94	V_{SS}
4	DQ0	34	DQS3#	64	(CK1)	95	DQS5#
5	DQ1	35	DQS3	65	(CK1#)	96	DQS5
6	V_{SS}	36	V_{SS}	66	V_{DD}	97	V_{SS}
7	DQS0#	37	DQ26	67	V_{REFCA}	98	DQ42
8	DQS0	38	DQ27	68	V_{DD}	99	DQ43
9	V_{SS}	39	V_{SS}	69	(PAR_IN)	100	V_{SS}
10	DQ2	40	CB0	70	V_{DD}	101	DQ48
11	DQ3	41	CB1	71	A10	102	DQ49
12	V_{SS}	42	V_{SS}	72	BA0	103	V_{SS}
13	DQ8	43	DQS8#	73	V_{DD}	104	DQS6#
14	DQ9	44	DQS8	74	WE#	105	DQS6
15	V_{SS}	45	V_{SS}	75	CAS#	106	V_{SS}
16	DQS1#	46	CB2	76	V_{DD}	107	DQ50
17	DQS1	47	CB3	77	(S1#)	108	DQ51
18	V_{SS}	48	V_{SS}	78	(ODT1)	109	V_{SS}
19	DQ10	49	NC	79	V_{DD}	110	DQ56
20	DQ11	50	Reset#	80	(S2#)	111	DQ57
21	V_{SS}	51	CKE0	81	NC	112	V_{SS}
22	DQ16	52	V_{DD}	82	V_{SS}	113	DQS7#
23	DQ17	53	BA2	83	DQ32	114	DQS7
24	V_{SS}	54	NC	84	DQ33	115	V_{SS}
25	DQS2#	55	V_{DD}	85	V_{SS}	116	DQ58
26	DQS2	56	A11	86	DQS4#	117	DQ59
27	V_{SS}	57	A7	87	DQS4	118	V_{SS}
28	DQ18	58	V_{DD}	88	V_{SS}	119	SA0
29	DQ19	59	A5	89	DQ34	120	SCL
30	V_{SS}	60	A4	90	DQ35	121	SA2
				91	V_{SS}	122	V_{TT}

(Sig): Signal in brackets may be routed to the socket connector, but is not used on the module

Backside							
Pin	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**
123	V_{TT}	153	DQ29	183	A3	214	DQ45
124	V_{SS}	154	V_{SS}	184	A1	215	V_{SS}
125	DQ4	155	DM3	185	V_{DD}	216	DM5
126	DQ5	156	NC	186	CK0	217	NC
127	V_{SS}	157	V_{SS}	187	CK0#	218	V_{SS}
128	DM0	158	DQ30	188	V_{DD}	219	DQ46
129	NC	159	DQ31	189	V_{DD}	220	DQ47
130	V_{SS}	160	V_{SS}	190	Event#	221	V_{SS}
131	DQ6	161	CB4	191	A0	222	DQ52
132	DQ7	162	CB5	192	V_{DD}	223	DQ53
133	V_{SS}	163	V_{SS}	193	BA1	224	V_{SS}
134	DQ12	164	DM8	194	V_{DD}	225	DM6
135	DQ13	165	NC	195	RAS#	226	NC
136	V_{SS}	166	V_{SS}	196	CS0#	227	V_{SS}
137	DM1	167	CB6	197	V_{DD}	228	DQ54
138	NC	168	CB7	198	ODT0	229	DQ55
139	V_{SS}	169	V_{SS}	199	A13	230	V_{SS}
140	DQ14	170	NC	200	V_{DD}	231	DQ60
141	DQ15	171	(TEST)	201	(S3#)	232	DQ61
142	V_{SS}	172	(CKE1)	202	NC	233	V_{SS}
143	DQ20	173	V_{DD}	203	V_{SS}	234	DM7
144	DQ21	174	A15	204	DQ36	235	NC
145	V_{SS}	175	A14	205	DQ37	236	V_{SS}
146	DM2	176	V_{DD}	206	V_{SS}	237	DQ62
147	NC	177	A12/BC#	207	DM4	238	DQ63
148	V_{SS}	178	A9	208	NC	239	V_{SS}
149	DQ22	179	V_{DD}	209	V_{SS}	240	V_{DDSPD}
150	DQ23	180	A8	210	DQ38	241	SA1
151	V_{SS}	181	A6	211	DQ39	242	SDA
152	DQ28	182	V_{DD}	212	V_{SS}	243	V_{SS}
				213	DQ44	244	V_{TT}

(Sig): Signal in brackets may be routed to the socket connector, but is not used on the module

FUNCTIONAL BLOCK DIAGRAMM 4096MB DDR3 SDRAM Mini-DIMM, 1 RANK AND 9 COMPONENTS



BA0-BA2 → BA0-BA2: SDRAM D0-D8
A0-A15 → A0-A15: SDRAM D0-D8
$\overline{RAS}$ → $\overline{RAS}$: SDRAM D0-D8
$\overline{CAS}$ → $\overline{CAS}$: SDRAM D0-D8
$\overline{WE}$ → $\overline{WE}$: SDRAM D0-D8
ODT0 → ODT: SDRAM D0-D8
CKE0 → CKE: SDRAM D0-D8
CK0 → CK: SDRAM D0-D8
$\overline{CK0}$ → $\overline{CK}$: SDRAM D0-D8
$\overline{RESET}$ → $\overline{RESET}$: SDRAM D0-D8

Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/$\overline{DQS}$/ODT/DM/CKE/$\overline{S}$ relationship must be maintained as shown.
3. DQ, DM, DQS/$\overline{DQS}$ resistors: Refer to associated topology diagram.
4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of the JEDED document.
5. For each DRAM, a unique ZQ resistor is connected to GND. The ZQ resistor is 240Ω±1%.
6. Refer to associated figure for SPD details.

MAXIMUM ELECTRICAL DC CHARACTERISTICS

PARAMETER/ CONDITION		SYMBOL	MIN	MAX	UNITS
Supply Voltage		V_{DD}	-0.4	1.975	V
I/O Supply Voltage		V_{DDQ}	-0.4	1.975	V
V_{DDL} Supply Voltage		V_{DDL}	-0.4	1.975	V
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	-0.4	1.975	V
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)		I_I			µA
	Command/Address RAS#, CAS#, WE#, S#, CKE		-16	16	
	CK, CK#		-16	16	
	DM		-2	2	
OUTPUT LEAKAGE CURRENT (DQ's and ODT are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})		I_{OZ}	-5	5	µA
	DQ, DQS, DQS#				
V_{REF} LEAKAGE CURRENT ; V_{REF} is on a valid level		I_{VREF}	-8	8	µA

DC OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V_{DD}	1.425	1.5	1.575	V
I/O Supply Voltage	V_{DDQ}	1.425	1.5	1.575	V
V_{DDL} Supply Voltage	V_{DDL}	1.425	1.5	1.575	V
I/O Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.50 x V_{DDQ}	0.51x V_{DDQ}	V
I/O Termination Voltage (system)	V_{TT}	0.49 x V_{DDQ}-20mV	0.50 x V_{DDQ}	0.51x V_{DDQ}+20mV	V
Input High (Logic 1) Voltage	$V_{IH\ (DC)}$	V_{REF} + 0.1		V_{DDQ} + 0.3	V
Input Low (Logic 0) Voltage	$V_{IL\ (DC)}$	-0.3		V_{REF} – 0.1	V

AC INPUT OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH\ (AC)}$	V_{REF} + 0.175	-	V
Input Low (Logic 0) Voltage	$V_{IL\ (AC)}$	-	V_{REF} - 0.175	V

CAPACITANCE

At DDR3 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

I_{DD} Specifications and Conditions

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

Parameter & Test Condition		Symbol	max.		Unit
			12800-CL11	10600-CL9	
OPERATING CURRENT *) : One device bank Active-Precharge; t_{RC}= t_{RC} (I_{DD}); t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}	405	360	mA
OPERATING CURRENT *) : One device bank; Active-Read-Precharge; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RC}= t_{RC} (I_{DD}), t_{RAS} = t_{RAS} MIN (I_{DD}), t_{RCD} = t_{RCD} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I_{DD4W}		I_{DD1}	495	450	mA
PRECHARGE POWER-DOWN CURRENT: All device banks idle; Power-down mode; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}	Fast Exit	I_{DD2P}	135	135	mA
	Slow Exit		135	135	
PRECHARGE QUIET STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}		I_{DD2Q}	180	180	mA
PRECHARGE STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD2N}	225	225	mA
ACTIVE POWER-DOWN CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF} (always fast exit)		I_{DD3P}	180	180	mA
ACTIVE STANDBY CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD3N}	270	270	mA
OPERATING READ CURRENT: All device banks open, Continuous burst reads; One module rank active; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD4R}	900	765	mA

Parameter & Test Condition	Symbol	max.		Unit
		12800-CL11	10600-CL9	
OPERATING WRITE CURRENT: All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD4W}	990	675	mA
BURST REFRESH CURRENT: t_{CK} = t_{CK} (I_{DD}); refresh command at every t_{RFC} (I_{DD}) interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD5}	1305	1080	mA
SELF REFRESH CURRENT: CK and CK# at 0V; CKE ≤ 0.2V; All other Control and Address bus inputs are floating at V_{REF}; DQ's are floating at V_{REF}	I_{DD6}	135	135	mA
OPERATING CURRENT*) : Four device bank interleaving READs, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = t_{RCD} (I_{DD}) – 1 x t_{CK} (I_{DD}); t_{CK} = t_{CK} (I_{DD}), t_{RC} = t_{RC} (I_{DD}), t_{RRD} = t_{RRD} (I_{DD}), t_{RCD} = t_{RCD} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	I_{DD7}	1575	1170	mA

***) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.**

TIMING VALUES USED FOR I_{DD} MEASUREMENT

I_{DD} MEASUREMENT CONDITIONS			
SYMBOL	**12800-CL11**	**10600-CL9**	**Unit**
CL (I_{DD})	11	9	t_{CK}
t_{RCD} (I_{DD})	13.75	13.5	ns
t_{RC} (I_{DD})	48.75	49.5	ns
t_{RRD} (I_{DD})	6	6	ns
t_{CK} (I_{DD})	1.25	1.5	ns
t_{RAS} MIN (I_{DD})	35	36	ns
t_{RAS} MAX (I_{DD})	70'200	70'200	ns
t_{RP} (I_{DD})	13.75	13.5	ns
t_{RFC} (I_{DD})	160	160	ns

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

AC CHARACTERISTICS			12800-CL11		10600-CL9		
PARAMETER		**SYMBOL**	**MIN**	**MAX**	**Min**	**MAX**	**Unit**
Clock cycle time	CL = 11	t_{CK} (11)	1.25	-	-	-	ns
	CL = 10	t_{CK} (10)	1.5	<1.875	1.5	<1.875	
	CL = 9	t_{CK} (9)	1.5	<1.875	1.5	<1.875	
	CL = 8	t_{CK} (8)	1.875	<2.5	1.875	<2.5	
	CL = 7	t_{CK} (7)	1.875	<2.5	1.875	<2.5	
	CL = 6	t_{CK} (6)	2.5	3.3	2.5	3.3	
	CL = 5	t_{CK} (5)	3.0	3.3	3.0	3.3	
Internal READ command to first data		t_{AA}	13.75	-	13.5	-	
DQ and DM input pulse width (for each input)		t_{DIPW}	360	-	400	-	ps
CK high-level width		$t_{CH\ (AVG)}$	0.47	0.53	0.47	0.53	t_{CK}
CK low-level width		$t_{CL\ (AVG)}$	0.47	0.53	0.47	0.53	t_{CK}
Data-out high-impedance window from CK/CK#		t_{HZ}	-	225	-	250	ps
Data-out low-impedance window from CK/CK#		t_{LZ}	-450	225	-500	250	ps
DQS input high pulse width		t_{DQSH}	0.45	0.55	0.45	0.55	t_{CK}
DQS input low pulse width		t_{DQSL}	0.45	0.55	0.45	0.55	t_{CK}
DQS read preamble		t_{RPRE}	0.9	Note1	0.9	Note1	t_{CK}
DQS read postamble		t_{RPST}	0.3	Note2	0.3	Note2	t_{CK}
DQS write preamble		t_{WPRE}	0.9	-	0.9	-	t_{CK}
DQS write postamble		t_{WPST}	0.3	-	0.3	-	t_{CK}

1 The maximum preamble is bound by t_{LZDQS} (MAX)
2 The maximum postamble is bound by t_{HZDQS} (MAX)

DQ, DQS and C/A signal setup and hold times t_{DS}, t_{DH}, t_{DQSQ}, t_{DSS}, t_{DQSS}, t_{DQSCK}, t_{IS}, t_{IH} need to be calculated with the respective DRAM derating tables and the driver slew rate or determined by simulation

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

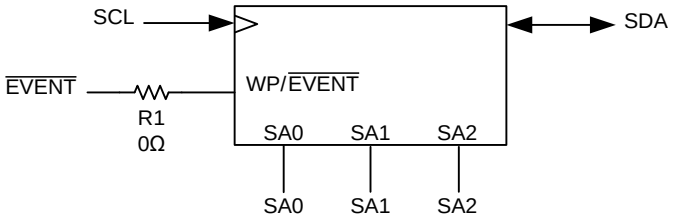
AC CHARACTERISTICS			12800-11-11-11		10600-9-9-9		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	Unit
Address and control input pulse width (for each input)		t_{IPW}	560	-	620	-	ps
CAS# to CAS# command delay		t_{CCD}	4	-	4	-	t_{CK}
ACTIVE to ACTIVE (same bank) command period		t_{RC}	48.75	-	49.5	-	ns
ACTIVE to ACTIVE minimum command period		t_{RRD}	max 4nCK,6ns	-	max 4nCK,6ns	-	ns
ACTIVE to READ or WRITE delay		t_{RCD}	13.75	-	13.5	-	ns
Four bank Activate period	1K Page size	t_{FAW}	30	-	30	-	ns
	2K Page size		40	-	45	-	
ACTIVE to PRECHARGE command		t_{RAS}	35	70’200	36	70’200	ns
Internal READ to precharge command delay		t_{RTP}	max 4nCK,7.5ns	-	max 4nCK,7.5ns	-	ns
Write recovery time		t_{WR}	15	-	15	-	ns
Auto precharge write recovery + precharge time		t_{DAL}	t_{WR} + t_{RP}/t_{CK}	-	t_{WR} + t_{RP}/t_{CK}	-	ns
Internal WRITE to READ command delay		t_{WTR}	max 4nCK,7.5ns	-	max 4nCK,7.5ns	-	ns
PRECHARGE command period		t_{RP}	13.75	-	13.5	-	ns
LOAD MODE command cycle time		t_{MRD}	4	-	4	-	t_{CK}
REFRESH to ACTIVE or REFRESH to REFRESH command interval		t_{RFC}	260	70’200	260	70’200	ns
Average periodic refresh interval 0 °C ≤ T_{CASE} ≤ 85° C		t_{REFI}	-	7.8	-	7.8	µs
85 °C < T_{CASE} ≤ 95° C		$t_{REFI (IT)}$	-	3.9	-	3.9	
RTT turn-on from ODTL on reference		t_{AON}	-225	225	-250	250	ps
RTT turn-on from ODTL off reference		t_{AOF}	0.3	0.7	0.3	0.7	t_{CK}
Asynchronous RTT turn-on delay (power Down with DLL off)		t_{AONPD}	2	8,5	2	8,5	ns
Asynchronous RTT turn-off delay (power Down with DLL off)		t_{AOFPD}	2	8,5	2	8,5	ns
RTT dynamic change skew		t_{ADC}	0.3	0.7	0.3	0.7	t_{CK}
Exit self refresh to commands not requiring a locked DLL		t_{XS}	max 5nCK,tR FC + 10ns	-	max 5nCK,tR FC + 10ns	-	ns
Write levelling setup from rising CK, CK# crossing to rising DQS, DQS# crossing		t_{WLS}	165	-	195	-	ps
Write levelling setup from rising DQS, DQS# crossing to rising CK, CK# crossing		t_{WLH}	165	-	195	-	ps
First DQS, DQS# rising edge		t_{WLMRD}	40	-	40	-	t_{CK}
DQS, DQS# delay		$t_{WLDQSEN}$	25	-	25	-	t_{CK}

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

AC CHARACTERISTICS		12800-CL11		10600-CL9		
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**Min**	**MAX**	**Unit**
Exit reset from CKE HIGH to a valid command	t_{XPR}	max 5nCK, t_{RFC} + 10ns	-	max 5nCK, t_{RFC} + 10ns	-	t_{CK}
Begin power supply ramp to power supplies stable	t_{VDDPR}	-	200	-	200	ms
RESET# LOW to power supplies stable	t_{RPS}	0	200	0	200	ms
RESET# LOW to I/O and RTT High-Z	t_{IOz}	-	20	-	20	ns
Exit precharge power-down to any non-READ command	t_{XP}	max 3nCK,6ns	-	max 3nCK,6ns	-	t_{CK}
CKE minimum high/low time	t_{CKE}	max 3nCK, 5ns	-	max 3nCK, 5.625ns	-	t_{CK}

Temperature Sensor with Serial Presence-Detect EEPROM



Temperature Sensor with Serial Presence-Detect EEPROM Operating Conditions

Parameter / Condition	Symbol	MIN	MAX	Unit
Supply voltage	V_{DDSPD}	+3	+3.6	V
Supply current: V_{DD} = 3.3V	I_{DD}		+2.0	mA
Input high voltage: Logic 1; SCL, SDA	V_{IH}	+1.45	V_{DDSPD} +1	V
Input low voltage: Logic 0; SCL, SDA	V_{IL}	-	550	mV
Output low voltage: I_{OUT} = 2.1mA	V_{OL}	-	400	mV
Input current	I_{IN}	-5.0	5.0	µA
Temperature sensing range		TBD	TBD	°C
Temperature sensor accuracy		TBD	TBD	°C

A.C. Characteristics of Temperature Sensor

V_{CC} = 3.3 V ± 10%, T_A = −40°C to +125°C

Symbol	Parameter / Condition	MIN	MAX	Unit
f_{SCL}	SCL clock frequency	10	400	kHz
t_{BUF}	Bus Free Time Between STOP and START	1300		ns
t_F	SDA fall time		300	ns
t_R	SDA rise time		300	ns
$t_{HD:DAT}$	Data hold time (accepted for Input Data)	0		ns
	Data Hold Time (guaranteed for Output Data)	300	900	ns
$t_{H:STA}$	Start condition hold time	600		ns
t_{HIGH}	High Period of SCL	600		ns
t_{LOW}	Low Period of SCL	1300		ns
$t_{SU:DAT}$	Data setup time	100		ns
$t_{SU:STA}$	Start condition setup time	600		ns
$t_{SU:STO}$	Stop condition setup time	600		ns
$t_{TIMEOUT}$	SMBus SCL Clock Low Timeout	25	35	ms
t_I	Noise Pulse Filtered at SCL and SDA Inputs		100	ns
t_{WR}	Write Cycle Time		5	ms
t_{PU}	Power-up Delay to Valid Temperature Recording		100	ms

Temperature Characteristics of Temperature Sensor

V_{CC} = 3.3 V ± 10%, T_A = −40°C to +125°C

Parameter	Test Conditions/Comments	MAX	Unit
Temperature Reading Error Class B, JC42.4 compliant	+75°C ≤ T_A ≤ +95°C, active range	±1.0	°C
	+40°C ≤ T_A ≤ +125°C, monitor range	±2.0	°C
	-40°C ≤ T_A ≤ +125°C, sensing range	±3.0	°C
ADC Resolution		12	Bits
Temperature Resolution		0.0625	°C
Conversion Time		100	Ms
Thermal Resistance[1] θ_{JA}	Junction-to-Ambient (Still Air)	92	°C/W

[1] Power Dissipation is defined as $P_J = (T_J - T_A)/\theta_{JA}$, where TJ is the junction temperature and TA is the ambient temperature. The thermal resistance value refers to the case of a package being used on a standard 2-layer PCB.

Slave Address Bits of Temperature Sensor

Device	Device Type Identifier				Select Address Signals			R/W#
	b7[1]	b6	b5	b4	b3	b2	b1	b0
EEPROM	1	0	1	0	A_2	A_1	A_0	R/W#
Temp. Sensor	0	0	1	1	A_2	A_1	A_0	R/W#

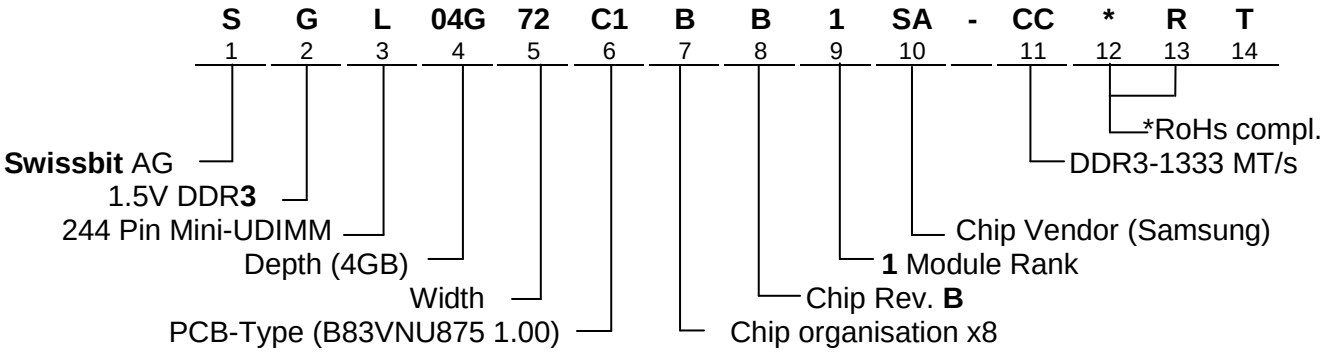
[1] The most significant bit, b7, is sent first.

SERIAL PRESENCE-DETECT MATRIX

Byte	Byte Description	12800-CL11	10600-CL9
0	CRC RANGE, EEPROM BYTES, BYTES USED	0x92	
1	SPD REVISON	0x11	
2	DRAM DEVICE TYPE	0x0B	
3	MODULE TYPE (FORM FACTOR)	0x06	
4	SDRAM DEVICE DENSITY & BANKS	0x04	
5	SDRAM DEVICE ROW & COLUMN COUNT	0x21	
6	BYTE 6 RESERVED	0x00	
7	MODULE RANKS & DEVICE DQ COUNT	0x01	
8	ECC TAG & MODULE MEMORY BUS WIDTH	0x0B	
9	FINE TIMEBASE DIVIDEND/DIVISOR	0x11	
10	MEDIUM TIMEBASE DIVIDEND	0x01	
11	MEDIUM TIMEBASE DIVISOR	0x08	
12	MIN SDRAM CYCLE TIME ($t_{CK\ MIN}$)	0x0A	0x0C
13	BYTE 13 RESERVED	0x00	
14	CAS LATENCIES SUPPORTED (CL4 => CL11)	0xFE	0x3E
15	CAS LATENCIES SUPPORTED (CL12 => CL18)	0x00	
16	MIN CAS LATENCY TIME ($t_{AA\ MIN}$)	0x69	
17	MIN WRITE RECOVERY TIME ($t_{WR\ MIN}$)	0x78	
18	MIN RAS# TO CAS# DELAY ($t_{RCD\ MIN}$)	0x69	
19	MIN ROW ACTIVE TO ROW ACTIVE DELAY ($t_{RRD\ MIN}$)	0x30	0x30
20	MIN ROW PRECHARGE DELAY ($t_{RP\ MIN}$)	0x69	
21	UPPER NIBBLE FOR t_{RAS} & t_{RC}	0x11	
22	MIN ACTIVE TO PRECHARGE DELAY ($t_{RAS\ MIN}$)	0x18	0x20
23	MIN ACTIVE TO ACTIVE/REFRESH DELAY ($t_{RC\ MIN}$)	0x81	0x89
24	MIN REFRESH RECOVERY DELAY ($t_{RFC\ MIN}$) LSB	0x20	
25	MIN REFRESH RECOVERY DELAY ($t_{RFC\ MIN}$) MSB	0x08	
26	MIN INTERNAL WRITE TO READ CMD DELAY ($t_{WTR\ MIN}$)	0x3C	
27	MIN INTERNAL READ TO PRECHARGE CMD DELAY ($t_{RTP\ MIN}$)	0x3C	
28	MIN FOUR ACTIVE WINDOW DELAY ($t_{FAW\ MIN}$) MSB	0x00	0x00
29	MIN FOUR ACTIVE WINDOW DELAY ($t_{FAW\ MIN}$) LSB	0xF0	0xF0
30	SDRAM DEVICE OUTPUT DRIVERS SUPPORTED	0x83	
31	SDRAM DEVICE THERMAL & REFRESH OPTIONS	0x05	

Byte	Byte Description	10600-999	8500-777
32	DDR3-MODULE THERMAL SENSOR	0x80	
33	DDR3-SDRAM DEVICE TYPE	0x00	
34	DDR3-FINE OFFSET FOR t_{CKMIN}	0x00	
35-59	BYTES 33-59 RESERVED	0x00	
60	MODULE HEIGHT (NOMINAL)	0x03	
61	MODULE THICKNESS (MAX)	0x11	
62	REFERENCE RAW CARD ID	0x03	
63	ADDRESS MAPPING EDGE CONECTOR TO DRAM	0x00	
64-116	BYTES 64-116 RESEVED	0x00	
117	MODULE MFR ID (LSB)	0x83	
118	MODULE MFR ID (MSB)	0xDA	
119	MODULE MFR LOCATION ID	0x01 (Switzerland) 0x02 (Germany) 0x03 (USA)	
120	MODULE MFR YEAR	X	
121	MODULE MFR WEEK	X	
122-125	MODULE SERIAL NUMBER	X	
126-127	CRC	0xA56A	0x91B5
128-145	MODULE PART NUMBER	"SGL04G72C1BB1SA-xx"	
146	MODULE DIE REV	X	
147	MODULE PCB REV	X	
148	DRAM DEVICE MFR ID (LSB)	0x80	
149	DRAM DEVICE MFR (MSB)	0xCE	
150-175	MFR RESERVED BYTES 150-175	0x00	
176-255	CUSTOMER RESERVED BYTES 176-255	0xFF	

Part Number Code



* optional / additional information
T= Thermal Sensor

Revision History		
Revision	Changes	Date
0.9	Preliminary Revision	21.06.2012
0.95	Corrected temp sensor / SPD schematics	25.06.2012
1.0	Removed setup/hold times, Release version	25.07.2012

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