Lattice Semiconductor Corporation

Data Sheet
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ORCA® ORT82G5 1.0—1.25/2.0—2.5/3.125—3.5 Gbits/s 8b/10b SERDES Backplane Interface FPSC

Introduction

Lattice has developed a next generation FPSC intended for high-speed serial backplane data transmission. Built on the Series 4 reconfigurable embedded system-on-chips (SoC) architecture, the ORT82G5 is made up of backplane transceivers containing eight channels, each operating at up to 3.5 Gbits/s (2.625 Gbits/s data rate), with a full-duplex synchronous interface with built-in Rx clock and data recovery (CDR), and Tx pre-emphasis along with up to 400k usable FPGA system gates. The CDR circuitry is a proven macrocell available from Lattice's intellectual property library, and has already been implemented in numerous applications, including ASICs, standard products, and FPSCs, to create interfaces for SONET/SDH, Fibre-channel, *Infiniband*™, and Ethernet (GbE, 10 GbE) applications. With the addition of protocol and access logic such as protocol-independent framers, asynchronous transfer mode (ATM) framers, Fibre-channel or *Infiniband* link layer capabilities, packet-over-SONET (POS) interfaces, and framers for HDLC for Internet protocol (IP), designers can build a configurable interface retaining proven backplane driver/receiver technology. Designers can also use the device to drive high-speed data transfer across buses within any generic system. For example, designers can build a 20 Gbits/s bridge for 10 Gbits/s Ethernet; the high-speed SERDES interfaces can comprise two XAUI interfaces with configurable back-end interfaces such as XGMII. The ORT82G5 can also be used to provide a full 10 Gbits/s backplane data connection with protection between a line card and switch fabric.

The ORT82G5 offers a clockless high-speed interface for interdevice communication on a board or across a backplane. The built-in clock recovery of the ORT82G5 allows for higher system performance, easier-to-design clock domains in a multiboard system, and fewer signals on the backplane. Network designers will benefit from the backplane transceiver as a network termination device. The device supports embedded 8b/10b encoding/decoding and link state machines for 10G Ethernet, and fibre-channel. The ORT82G5 is also pinout compatible to the ORSO82G5, which implements 8 channels of SERDES with SONET scrambling and cell processing.

Table 1. *ORCA* ORT82G5 Family—Available FPGA Logic

Device	PFU Rows	PFU Columns	Total PFUs	User I/O	LUTs	EBR Blocks	EBR Bits (k)	Usable* Gates (k)
ORT82G5	36	36	1296	372/432 †	10,368	12	111	380—800

* The embedded core and interface are not included in the above gate counts. The usable gate counts range from a logic-only gate count to a gate count assuming that 20% of the PFUs/SLICs are being used as RAMs. The logic-only gate count includes each PFU/SLIC (counted as 108 gates/PFU), including 12 gates per LUT/FF pair (eight per PFU), and 12 gates per SLIC/FF pair (one per PFU). Each of the four PIO groups are counted as 16 gates (three FFs, fast-capture latch, output logic, CLK, and I/O buffers). PFUs used as RAM are counted at four gates per bit, with each PFU capable of implementing a 32 x 4 RAM (or 512 gates) per PFU. Embedded block RAM (EBR) is counted as four gates per bit plus each block has an additional 25k gates. 7k gates are used for each PLL and 50k gates for the embedded system bus and microprocessor interface logic. Both the EBR and PLLs are conservatively utilized in the gate count calculations.

† 372 user I/Os out of a total of 432 user I/Os are bonded in the 680 PBGAM package.

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Embedded Function Features

- High-speed SERDES with programmable serial data rates including 1.0 Gbits/s, 1.25 Gbits/s, 2.5 Gbits/s, 3.125 Gbits/s, and 3.5 Gbits/s. Operation has been demonstrated on design tolerance devices at 4.25 Gbits/s across 20 in. of FR-4 backplane and at 3.2 Gbits/s across 40 in. of FR-4 backplane.
- Asynchronous operation per receive channel with the receiver frequency tolerance based on one reference clock per quad channels (separate PLL per channel).
- Ability to select full-rate or half-rate operation per Tx or Rx channel by setting the appropriate control registers.
- Programmable one-half amplitude transmit mode for reduced power in chip-to-chip application.
- Transmit preemphasis (programmable) for improved receive data eye opening.
- Receiver energy detector to determine if a link is active. Optional automatic power-down for inactive channels.
- 32-bit (8b/10b) or 40-bit (raw data) parallel internal bus for data processing in FPGA logic.
- Provides a 10 Gbits/s backplane interface to switch fabric with protection. Also supports port cards at 40 Gbits/s or 2.5 Gbits/s.
- 3.125 Gbits/s SERDES compliant with XAUI serial data specification for 10 Gbit Ethernet applications with protection.
- Most XAUI features for 10 Gbit Ethernet are embedded including the required link state machine.
- Compliant to fibre-channel physical layer specification.
- High-speed interface (HSI) function for clock/data recovery serial backplane data transfer without external clocks.
- Eight-channel HSI function provides 2.5 Gbits/s serial user data interface per channel for a total chip bandwidth of 20 Gbits/s (full duplex).
- SERDES has low-power CML buffers. Support for 1.5 V/1.8 V I/Os. Allows use with optical transceiver, coaxial copper media, shielded twisted pair wiring or high-speed backplanes such as FR-4.
- Powerdown option of SERDES HSI receiver or transmitter on a per-channel basis.
- Automatic lock to reference clock in the absence of valid receive data.
- Per channel PRBS generator and checker.
- High-speed (serial) and low-speed (parallel) loopback test modes.
- Requires no external component for clock recovery and frequency synthesis.
- SERDES characterization pins available to control/monitor the internal interface to one SERDES quad macro.
- SERDES HSI automatically recovers from loss-of-clock once its reference clock returns to normal operating state.
- Built-in boundary scan (*IEEE* ® 1149.1 and 1149.2 JTAG) for the programmable I/Os, not including the SERDES interface.
- FIFOs align incoming data across all eight channels (all eight channels, two groups of four channels, or four groups of two channels). Alignment is done using comma characters or /A/ character in XAUI mode. Optional ability to bypass alignment FIFOs for asynchronous operation between channels. (Each channel includes its own clock and frame pulse or comma detect.)
- Addition of two 4K X 36 dual-port RAMs with access to the programmable logic.
- Pinout compatible to the ORCA ORSO82G5 SONET backplane driver FPSC in the 680 PBGAM package.

Intellectual Property Features

Programmable logic provides a variety of yet-to-be standardized interface functions, including the following Lattice IP core functions:

- 10 Gbits/s Ethernet as defined by *IEEE* 802.3ae:
  - — XGMII for interfacing to 10 Gbits/s Ethernet MACs (media access controller). XGMII is a 156 MHz double data rate parallel short reach (typically less than 2") interconnect interface.
  - — XAUI to XGMII translator (XGXS), including support for dual XAUI ports for 1 + 1 XAUI protection.
- POS-PHY4 interface for 10 Gbits/s SONET/SDH and OTN systems and some 10 Gbits/s Ethernet systems to allow easy integration of *InfiniBand*, fibre-channel, and 10 Gbits/s Ethernet in data over fibre applications.
- Ethernet MAC functions at 10/100 Mbits/s, 1 Gbits/s, and 10 Gbits/s.
- Backplane drivers for industry standard products, including 2.5 Gbits/s and 10Gbps Network Processors and 2.5Gbps and 10Gbps Switch fabrics such as the Pi-family (Pi-X, Pi-C).
- Other functions such as fibre-channel (including fibre channel XAUI) and *InfiniBand* link layer IP cores are also planned.
- XAUI interface to emerging RPR (resilient packet ring) MAC solution.

Programmable Features

- High-performance programmable logic:
  - — 0.16 µm 7-level metal technology.
  - — Internal performance of >250 MHz.
  - — Over 400k usable system gates.
  - — Meets multiple I/O interface standards.
  - — 1.5 V operation (30% less power than 1.8 V operation) translates to greater performance.
- Traditional I/O selections:
  - — LVTTL and LVCMOS (3.3 V, 2.5 V, and 1.8 V) I/Os.
  - — Per pin-selectable I/O clamping diodes provide 3.3 V PCI compliance.
  - — Individually programmable drive capability: 24 mA sink/12 mA source, 12 mA sink/6 mA source, or 6 mA sink/3 mA source.
  - — Two slew rates supported (fast and slew-limited).
  - — Fast-capture input latch and input flip-flop (FF)/latch for reduced input setup time and zero hold time.
  - — Fast open-drain drive capability.
  - — Capability to register 3-state enable signal.
  - — Off-chip clock drive capability.
  - — Two-input function generator in output path.
- New programmable high-speed I/O:
  - — Single-ended: GTL, GTL+, PECL, SSTL3/2 (class I and II), HSTL (Class I, III, IV), ZBT, and DDR.
  - — Double-ended: LVDS, bused-LVDS, and LVPECL. Programmable, (on/off) internal parallel termination (100 Ω) is also supported for these I/Os.
- New capability to (de)multiplex I/O signals:
  - — New DDR on both input and output at rates up to 350 MHz (700 MHz effective rate).
  - — New 2x and 4x downlink and uplink capability per I/O (i.e., 50 MHz internal to 200 MHz I/O).
- Enhanced twin-quad programmable function unit (PFU):
  - — Eight 16-bit look-up tables (LUTs) per PFU.
  - — Nine user registers per PFU, one following each LUT, and organized to allow two nibbles to act independently, plus one extra for arithmetic operations.
  - — New register control in each PFU has two independent programmable clocks, clock enables, local set/reset, and data selects.
  - — New LUT structure allows flexible combinations of LUT4, LUT5, new LUT6, 4 → 1 MUX, new 8 → 1 MUX, and ripple mode arithmetic functions in the same PFU.
  - — 32 x 4 RAM per PFU, configurable as single- or dual-port. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the SLIC decoders as bank drivers.
  - — Soft-wired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU through fast internal routing which reduces routing congestion and improves speed.
  - — Flexible fast access to PFU inputs from routing.
  - — Fast-carry logic and routing to all four adjacent PFUs for nibble-wide, byte-wide, or longer arithmetic functions, with the option to register the PFU carry-out.
- Abundant high-speed buffered and nonbuffered routing resources provide 2x average speed improvements over previous architectures.
- Hierarchical routing optimized for both local and global routing with dedicated routing resources. This results in faster routing times with predictable and efficient performance.
- SLIC provides eight 3-statable buffers, up to a 10-bit decoder, and *PAL*™-like and-or-invert (AOI) in each programmable logic cell.
- New 200 MHz embedded quad-port RAM blocks, 2 read ports, 2 write ports, and 2 sets of byte lane enables. Each embedded RAM block can be configured as:
  - — 1—512 x 18 (quad-port, two read/two write) with optional built in arbitration.
  - — 1—256 x 36 (dual-port, one read/one write).
  - — 1—1k x 9 (dual-port, one read/one write).
  - — 2—512 x 9 (dual-port, one read/one write for each).
  - — 2 RAMS with arbitrary number of words whose sum is 512 or less by 18 (dual-port, one read/one write).
  - — Supports joining of RAM blocks.
  - — Two 16 x 8-bit content addressable memory (CAM) support.
  - — FIFO 512 x 18, 256 x 36, 1k x 9, or dual 512 x 9.
  - — Constant multiply (8 x 16 or 16 x 8).
  - — Dual variable multiply (8 x 8).
- Embedded 32-bit internal system bus plus 4-bit parity interconnects FPGA logic, microprocessor interface (MPI), embedded RAM blocks, and embedded standard cell blocks with 100 MHz bus performance. Included are built-in system registers that act as the control and status center for the device.

Programmable Features (continued)

- Built-in testability:
  - — Full boundary scan (*IEEE* 1149.1 and Draft 1149.2 JTAG).
  - — Programming and readback through boundary scan port compliant to *IEEE* Draft 1532:D1.7.
  - — TS_ALL testability function to 3-state all I/O pins.
  - — New temperature-sensing diode.
- Improved built-in clock management with programmable phase-locked loops (PPLLs) provide optimum clock modification and conditioning for phase, frequency, and duty cycle from 20 MHz up to 420 MHz. Multiplication of the input frequency up to 64x and division of the input frequency down to 1/64x possible.
- New cycle stealing capability allows a typical 15% to 40% internal speed improvement after final place and route. This feature also enables compliance with many setup/hold and clock to out I/O specifications and may provide reduced ground bounce for output buses by allowing flexible delays of switching output buffers.

Programmable Logic System Features

- PCI local bus compliant for FPGA I/Os.
- Improved *PowerPC* ® 860 and *PowerPC* II high-speed synchronous microprocessor interface can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA logic, RAMs, and embedded standard cell blocks. Glueless interface to synchronous *PowerPC* processors with user-configurable address space provided.
- New embedded *AMBA* ™ specification 2.0 AHB system bus (*ARM* ® processor) facilitates communication among the microprocessor interface, configuration logic, embedded block RAM, FPGA logic, and embedded standard cell blocks.
- Variable size bused readback of configuration data capability with the built-in microprocessor interface and system bus.
- Internal, 3-state, and bidirectional buses with simple control provided by the SLIC.
- New clock routing structures for global and local clocking significantly increases speed and reduces skew (<200 ps for OR4E4).
- New local clock routing structures allow creation of localized clock trees.
- Two new edge clock routing structures allow up to six high-speed clocks on each edge of the device for improved setup/hold and clock to out performance.
- New double-data rate (DDR) and zero-bus turnaround (ZBT) memory interfaces support the latest high-speed memory interfaces.
- New 2x/4x uplink and downlink I/O capabilities interface high-speed external I/Os to reduced speed internal logic.
- *ORCA* Foundry development system software. Supported by industry-standard CAE tools for design entry, synthesis, simulation, and timing analysis.
- Meets universal test and operations PHY interface for ATM (UTOPIA) levels 1, 2, and 3; as well as POS-PHY3. Also meets proposed specifications for UTOPIA level 4 and POS-PHY3 (2.5 Gbits/s) and POS-PHY4 (10 Gbits/s) interface standards for packet-over-SONET as defined by the Saturn Group.

Description

What Is an FPSC?

FPSCs, or field-programmable system chips, are devices that combine field-programmable logic with ASIC or mask-programmed logic on a single device. FPSCs provide the time to market and the flexibility of FPGAs, the design effort savings of using soft intellectual property (IP) cores, and the speed, design density, and economy of ASICs.

FPSC Overview

Lattice's Series 4 FPSCs are created from Series 4 *ORCA* FPGAs. To create a Series 4 FPSC, several columns of programmable logic cells (see FPGA Logic Overview section for FPGA logic details) are added to an embedded logic core. Other than replacing some FPGA gates with ASIC gates, at greater than 10:1 efficiency, none of the FPGA functionality is changed—all of the Series 4 FPGA capability is retained: embedded block RAMs, MPI, PCMs, boundary scan, etc. The columns of programmable logic are replaced at the right of the device, allowing pins from the replaced columns to be used as I/O pins for the embedded core. The remainder of the device pins retain their FPGA functionality.

FPSC Gate Counting

The total gate count for an FPSC is the sum of its embedded core (standard-cell/ASIC gates) and its FPGA gates. Because FPGA gates are generally expressed as a usable range with a nominal value, the total FPSC gate count is sometimes expressed in the same manner. Standard-cell ASIC gates are, however, 10 to 25 times more silicon-area efficient than FPGA gates. Therefore, an FPSC with an embedded function is gate equivalent to an FPGA with a much larger gate count.

FPGA/Embedded Core Interface

The interface between the FPGA logic and the embedded core has been enhanced to allow for a greater number of interface signals than on previous FPSC architectures. Compared to bringing embedded core signals off-chip, this on-chip interface is much faster and requires less power. All of the delays for the interface are precharacterized and accounted for in the *ORCA* Foundry Development System.

Series 4 based FPSCs expand this interface by providing a link between the embedded block and the multimaster 32-bit system bus in the FPGA logic. This system bus allows the core easy access to many of the FPGA logic functions including the embedded block RAMs and the microprocessor interface.

Clock spines also can pass across the FPGA/embedded core boundary. This allows for fast, low-skew clocking between the FPGA and the embedded core. Many of the special signals from the FPGA, such as DONE and global set/reset, are also available to the embedded core, making it possible to fully integrate the embedded core with the FPGA as a system.

For even greater system flexibility, FPGA configuration RAMs are available for use by the embedded core. This allows for user-programmable options in the embedded core, in turn allowing for greater flexibility. Multiple embedded core configurations may be designed into a single device with user-programmable control over which configurations are implemented, as well as the capability to change core functionality simply by reconfiguring the device.

ORCA Foundry Development System

The *ORCA* Foundry development system is used to process a design from a netlist to a configured FPGA. This system is used to map a design onto the *ORCA* architecture, and then place and route it using *ORCA* Foundry's timing-driven tools. The development system also includes interfaces to, and libraries for, other popular CAE tools for design entry, synthesis, simulation, and timing analysis.

The *ORCA* Foundry development system interfaces to front-end design entry tools and provides the tools to produce a configured FPGA. In the design flow, the user defines the functionality of the FPGA at two points in the design flow: design entry and the bitstream generation stage. Recent improvements in *ORCA* Foundry allow the user to provide timing requirement information through logical preferences only; thus, the designer is not required to have physical knowledge of the implementation.

Description (continued)

Following design entry, the development system's map, place, and route tools translate the netlist into a routed FPGA. A floorplanner is available for layout feedback and control. A static timing analysis tool is provided to determine device speed and a back-annotated netlist can be created to allow simulation and timing.

Timing and simulation output files from *ORCA* Foundry are also compatible with many third-party analysis tools. Its bit stream generator is then used to generate the configuration data which is loaded into the FPGAs internal configuration RAM, embedded block RAM, and/or FPSC memory.

When using the bit stream generator, the user selects options that affect the functionality of the FPGA. Combined with the front-end tools, *ORCA* Foundry produces configuration data that implements the various logic and routing options discussed in this data sheet.

FPSC Design Kit

Development is facilitated by an FPSC design kit which, together with *ORCA* Foundry and third-party synthesis and simulation engines, provides all software and documentation required to design and verify an FPSC implementation. Included in the kit are the FPSC configuration manager, *Synopsys Smart Model* ®, and/or complied *Verilog* simulation model, *HSPICE* and/or IBIS models for I/O buffers, and complete online documentation. The kit's software couples with *ORCA* Foundry, providing a seamless FPSC design environment. More information can be obtained by visiting the *ORCA* website or contacting a local sales office, both listed on the last page of this document.

FPGA Logic Overview

The *ORCA* Series 4 architecture is a new generation of SRAM-based programmable devices from Lattice. It includes enhancements and innovations geared toward today's high-speed systems on a single chip. Designed with networking applications in mind, the Series 4 family incorporates system-level features that can further reduce logic requirements and increase system speed. *ORCA* Series 4 devices contain many new patented enhancements and are offered in a variety of packages and speed grades.

The hierarchical architecture of the logic, clocks, routing, RAM, and system-level blocks create a seamless merge of FPGA and ASIC designs. Modular hardware and software technologies enable system-on-chip integration with true plug-and-play design implementation.

The architecture consists of four basic elements: programmable logic cells (PLCs), programmable I/O cells (PIOs), embedded block RAMs (EBRs), and system-level features. These elements are interconnected with a rich routing fabric of both global and local wires. An array of PLCs are surrounded by common interface blocks which provide an abundant interface to the adjacent PLCs or system blocks. Routing congestion around these critical blocks is eliminated by the use of the same routing fabric implemented within the programmable logic core. Each PLC contains a PFU, SLIC, local routing resources, and configuration RAM. Most of the FPGA logic is performed in the PFU, but decoders, *PAL*-like functions, and 3-state buffering can be performed in the SLIC. The PIOs provide device inputs and outputs and can be used to register signals and to perform input demultiplexing, output multiplexing, uplink and downlink functions, and other functions on two output signals. Large blocks of 512 x 18 quad-port RAM complement the existing distributed PFU memory. The RAM blocks can be used to implement RAM, ROM, FIFO, multiplier, and CAM. Some of the other system-level functions include the MPI, PLLs, and the embedded system bus (ESB).

PLC Logic

Each PFU within a PLC contains eight 4-input (16-bit) LUTs, eight latches/FFs, and one additional flip-flop that may be used independently or with arithmetic functions.

The PFU is organized in a twin-quad fashion; two sets of four LUTs and FFs that can be controlled independently. Each PFU has two independent programmable clocks, clock enables, local set/reset, and data selects. LUTs may also be combined for use in arithmetic functions using fast-carry chain logic in either 4-bit or 8-bit modes. The carry-out of either mode may be registered in the ninth FF for pipelining. Each PFU may also be configured as a synchronous 32 x 4 single- or dual-port RAM or ROM. The FFs (or latches) may obtain input from LUT outputs or directly from invertible PFU inputs, or they can be tied high or tied low. The FFs also have programmable clock polarity, clock enables, and local set/reset.

Description (continued)

The SLIC is connected from PLC routing resources and from the outputs of the PFU. It contains eight 3-state, bidirectional buffers, and logic to perform up to a 10-bit AND function for decoding, or an AND-OR with optional INVERT to perform *PAL*-like functions. The 3-state drivers in the SLIC and their direct connections from the PFU outputs make fast, true, 3-state buses possible within the FPGA, reducing required routing and allowing for real-world system performance.

Programmable I/O

The Series 4 PIO addresses the demand for the flexibility to select I/Os that meet system interface requirements. I/Os can be programmed in the same manner as in previous *ORCA* devices, with the additional new features which allow the user the flexibility to select new I/O types that support high-speed interfaces.

Each PIO contains four programmable I/O pads and is interfaced through a common interface block to the FPGA array. The PIO is split into two pairs of I/O pads with each pair having independent clock enables, local set/reset, and global set/reset. On the input side, each PIO contains a programmable latch/flip-flop which enables very fast latching of data from any pad. The combination provides for very low setup requirements and zero hold times for signals coming on-chip. It may also be used to demultiplex an input signal, such as a multiplexed address/data signal, and register the signals without explicitly building a demultiplexer with a PFU.

On the output side of each PIO, an output from the PLC array can be routed to each output flip-flop, and logic can be associated with each I/O pad. The output logic associated with each pad allows for multiplexing of output signals and other functions of two output signals.

The output FF, in combination with output signal multiplexing, is particularly useful for registering address signals to be multiplexed with data, allowing a full clock cycle for the data to propagate to the output. The output buffer signal can be inverted, and the 3-state control can be made active-high, active-low, or always enabled. In addition, this 3-state signal can be registered or nonregistered.

The Series 4 I/O logic has been enhanced to include modes for speed uplink and downlink capabilities. These modes are supported through shift register logic, which divides down incoming data rates or multiplies up outgoing data rates. This new logic block also supports high-speed DDR mode requirements where data is clocked into and out of the I/O buffers on both edges of the clock.

The new programmable I/O cell allows designers to select I/Os which meet many new communication standards permitting the device to hook up directly without any external interface translation. They support traditional FPGA standards as well as high-speed, single-ended, and differential-pair signaling (as shown in Table 1). Based on a programmable, bank-oriented I/O ring architecture, designs can be implemented using 3.3 V, 2.5 V, 1.8 V, and 1.5 V referenced output levels.

Routing

The abundant routing resources of the Series 4 architecture are organized to route signals individually or as buses with related control signals. Both local and global signals utilize high-speed buffered and nonbuffered routes. One PLC segmented (x1), six PLC segmented (x6), and bused half chip (xHL) routes are patterned together to provide high connectivity with fast software routing times and high-speed system performance.

Eight fully distributed primary clocks are routed on a low-skew, high-speed distribution network and may be sourced from dedicated I/O pads, PLLs, or the PLC logic. Secondary and edge-clock routing is available for fast regional clock or control signal routing for both internal regions and on device edges. Secondary clock routing can be sourced from any I/O pin, PLLs, or the PLC logic.

The improved routing resources offer great flexibility in moving signals to and from the logic core. This flexibility translates into an improved capability to route designs at the required speeds when the I/O signals have been locked to specific pins.

System-Level Features

The Series 4 also provides system-level functionality by means of its microprocessor interface, embedded system bus, quad-port embedded block RAMs, universal programmable phase-locked loops, and the addition of highly tuned networking specific phase-locked loops. These functional blocks allow for easy glueless system interfacing and the capability to adjust to varying conditions in today's high-speed networking systems.

Microprocessor Interface

The MPI provides a glueless interface between the FPGA and *PowerPC* microprocessors. Programmable in 8-, 16-, and 32-bit interfaces with optional parity to the *Motorola® PowerPC* 860 bus, it can be used for configuration and readback, as well as for FPGA control and monitoring of FPGA status. All MPI transactions utilize the Series 4 embedded system bus at 66 MHz performance.

A system-level microprocessor interface to the FPGA user-defined logic following configuration, through the system bus, including access to the embedded block RAM and general user-logic, is provided by the MPI. The MPI supports burst data read and write transfers, allowing short, uneven transmission of data through the interface by including data FIFOs. Transfer accesses can be single beat (1 x 4 bytes or less), 4-beat (4 x 4 bytes), 8-beat (8 x 2 bytes), or 16-beat (16 x 1 bytes).

System Bus

An on-chip, multimaster, 8-bit system bus with 1-bit parity facilitates communication among the MPI, configuration logic, FPGA control, and status registers, embedded block RAMs, as well as user logic. Utilizing the *AMBA* specification Rev 2.0 AHB protocol, the embedded system bus offers arbiter, decoder, master, and slave elements. Master and slave elements are also available for the user-logic and a slave interface is used for control and status of the embedded backplane transceiver portion of the ORT82G5.

The system bus control registers can provide control to the FPGA such as signaling for reprogramming, reset functions, and PLL programming. Status registers monitor INIT, DONE, and system bus errors. An interrupt controller is integrated to provide up to eight possible interrupt resources. Bus clock generation can be sourced from the microprocessor interface clock, configuration clock (for slave configuration modes), internal oscillator, user clock from routing, or from the port clock (for JTAG configuration modes).

Phase-Locked Loops

Up to eight PLLs are provided on each Series 4 device, with four PLLs generally provided for FPSCs. Programmable PLLs can be used to manipulate the frequency, phase, and duty cycle of a clock signal. Each PPLL is capable of manipulating and conditioning clocks from 20 MHz to 420 MHz. Frequencies can be adjusted from 1/8x to 8x, the input clock frequency. Each programmable PLL provides two outputs that have different multiplication factors but can have the same phase relationships. Duty cycles and phase delays can be adjusted in 12.5% of the clock period increments. An automatic input buffer delay compensation mode is available for phase delay. Each PPLL provides two outputs that can have programmable (12.5% steps) phase differences.

Additional highly tuned and characterized, dedicated phase-locked loops (DPLLs) are included to ease system designs. These DPLLs meet ITU-T G.811 primary-clocking specifications and enable system designers to very tightly target specified clock conditioning not traditionally available in the universal PPLLs. Initial DPLLs are targeted to low-speed networking DS1 and E1, and also high-speed SONET/SDH networking STS-3 and STM-1 systems. These DPLLs are not typically included on FPSC devices and are not found on the ORT82G5.

Embedded Block RAM

New 512 x 18 quad-port RAM blocks are embedded in the FPGA core to significantly increase the amount of memory and complement the distributed PFU memories. The EBRs include two write ports, two read ports, and two byte lane enables which provide four-port operation. Optional arbitration between the two write ports is available, as well as direct connection to the high-speed system bus.

Additional logic has been incorporated to allow significant flexibility for FIFO, constant multiply, and two-variable multiply functions. The user can configure FIFO blocks with flexible depths of 512k, 256k, and 1k including asynchronous and synchronous modes and programmable status and error flags. Multiplier capabilities allow a multiple of an 8-bit number with a 16-bit fixed coefficient or vice versa (24-bit output), or a multiply of two 8-bit numbers (16-bit output). On-the-fly coefficient modifications are available through the second read/write port. Two 16 x 8-bit CAMs per embedded block can be implemented in single match, multiple match, and clear modes. The EBRs can also be preloaded at device configuration time.

System-Level Features (continued)

Configuration

The FPGAs functionality is determined by internal configuration RAM. The FPGAs internal initialization/configuration circuitry loads the configuration data at powerup or under system control. The configuration data can reside externally in an EEPROM or any other storage media. Serial EEPROMs provide a simple, low pin-count method for configuring FPGAs.

The RAM is loaded by using one of several configuration modes. Supporting the traditional master/slave serial, master/slave parallel, and asynchronous peripheral modes, the Series 4 also utilizes its microprocessor interface and embedded system bus to perform both programming and readback. Daisy chaining of multiple devices and partial reconfiguration are also permitted.

Other configuration options include the initialization of the embedded-block RAM memories and FPSC memory as well as system bus options and bit stream error checking. Programming and readback through the JTAG *(IEEE* 1149.2*)* port is also available meeting in-system programming (ISP) standards (*IEEE* 1532 Draft).

Additional Information

Contact your local Lattice representative for additional information regarding the *ORCA* Series 4 FPGA devices, or visit our website at:

http://www.latticesemi.com/

ORT82G5 Overview

Device Layout

The ORT82G5 is a backplane transceiver FPSC with embedded CDR and SERDES circuitry and 8b/10b encoding/decoding (*IEEE* 802.3z). It is intended for high-speed serial backplane data transmission. Built using Series 4 reconfigurable system-on-chips (SoC) architecture, it also contains up to 400k usable FPGA system gates.

The ORT82G5 contains an FPGA base array, an eight-channel clock and data recovery macro, and an eight-channel 8b/10b interface on a single monolithic chip.

Figure 1 shows the ORT82G5 block diagram. Boundary scan for the ORT82G5 only includes programmable I/Os and does not include any of the embedded block I/Os.

Backplane Transceiver Interface

The ORT82G5 backplane transceiver FPSC has eight channels, each operating at up to 3.125 Gbits/s (2.5 Gbits/s data rate) with a full-duplex synchronous interface with built-in clock recovery (CDR). The CDR macro with 8b/10b provides guaranteed ones density for the CDR, byte alignment, and error detection.

The CDR interface provides a physical medium for high-speed asynchronous serial data transfer between system devices. Devices can be on the same PC-board, on separate boards connected across a backplane, or connected by cables. This core is intended for, but not limited to, terminal equipment in SONET/SDH, Gbit Ethernet, 10 Gbit Ethernet, ATM, fibre-channel, and *Infiniband* systems.

The SERDES circuitry consists of receiver, transmitter, and auxiliary functional blocks. The receiver accepts high-speed (up to 3.5 Gbits/s) serial data. Based on data transitions, the receiver locks an analog receive PLL for each channel to retime the data, then demultiplexes down to parallel bytes and clock. The transmitter operates in the reverse direction. Parallel bytes are multiplexed up to 3.5 Gbits/s serial data for off-chip communication. The transmitter generates the necessary 3.5 GHz clocks for operation from a lower speed reference clock.

This device will support 8b/10b encoding/decoding, which is capable of frame synchronization and physical link monitoring. Figure 2 shows the internal architecture of the ORT82G5 backplane transceiver core.

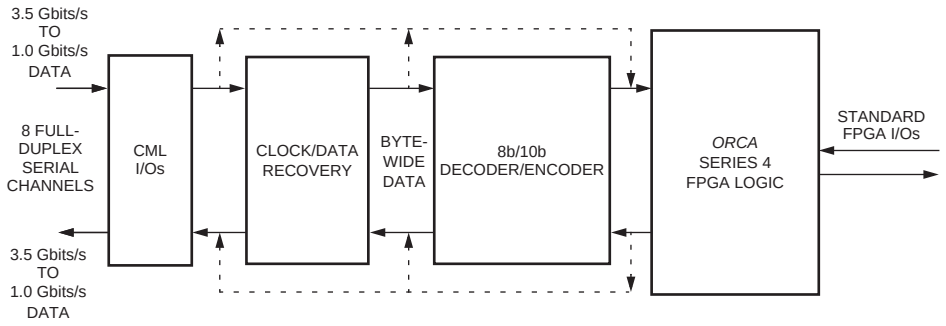

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Figure 1. ORT82G5 Block Diagram

ORT82G5 Overview (continued)

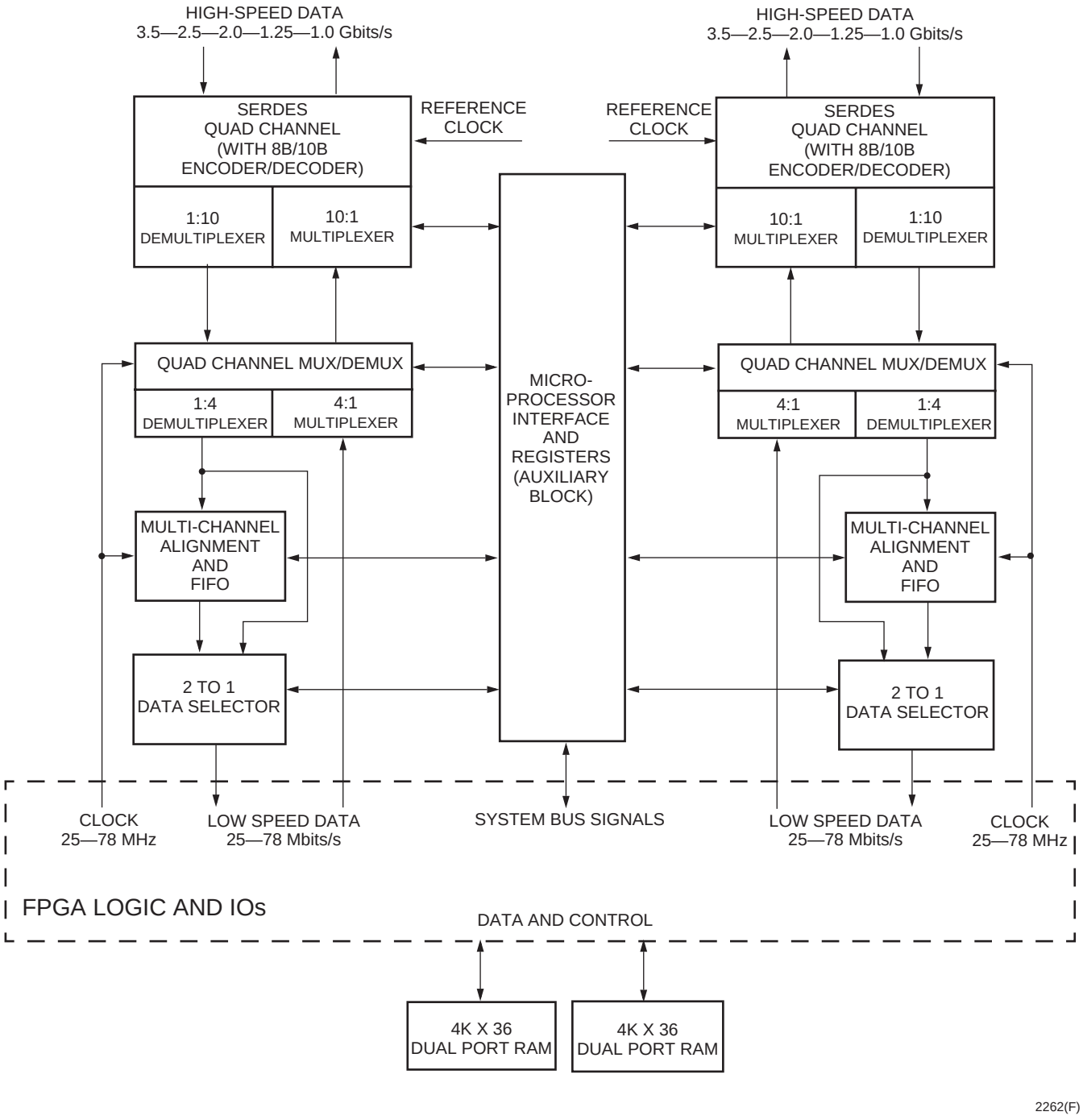

Figure 2. Internal High-Level Diagram of ORT82G5 Transceiver

ORT82G5 Overview (continued)

The ORT82G5 FPSC combines 8 channels of high-speed full duplex serial links (up to 3.5 Gbits/s) with 400k usable gate FPGA. The major functional blocks in the ASB core are two quad-channel serializer-deserializers (SERDES) including 8b/10b encoder/decoder and dedicated PLLs, XAUI or fibre-channel link-state-machine, 4-to-1 or 1-to-4 MUX/deMUX, multichannel alignment FIFO, microprocessor interface, and 4k x 36 RAM blocks.

Serializer and Deserializer (SERDES)

The SERDES block is a quad transceiver for serial data transmission, with a selectable data rate of 1.0—1.25 Gbits/s, 2.0—2.5 Gbits/s, or 3.125—3.5 Gbits/s. It is designed to operate in Ethernet, fibre channel, XAUI, *InfiniBand*, or backplane applications. It features high-speed 8b/10b parallel I/O interfaces, and high-speed CML interfaces.

The quad transceiver is controlled and configured with an 8-bit microprocessor interface through the FPGA. Each channel has dedicated registers that are readable and writable. The quad device also contains global registers for control of common circuitry and functions.

8b/10b Encoding/Decoding

The ORT82G5 facilitates high-speed serial transfer of data in a variety of applications including Gbit Ethernet, fibre channel, serial backplanes, and proprietary links. The SERDES provides 8b/10b coding/decoding for each channel. The 8b/10b transmission code includes serial encoding/decoding rules, special characters, and error detection.

In the receive direction, the user can disable the 8b/10b decoder to receive raw 10 bit words which will be rate reduced by the SERDES. If this mode is chosen, the user must bypass the multichannel alignment FIFOs. In the transmit direction, the 8b/10b encoder must always be enabled.

Clocks

The SERDES block contains its own dedicated PLLs for transmit and receive clock generation. The user provides a reference clock of the appropriate frequency. The receiver PLLs extract the clock from the serial input data and retime the data with the recovered clock.

MUX/DeMUX Block

The purpose of the MUX/deMUX block is to provide a wide, low-speed interface at the FPGA portion of the ORT82G5 for each channel or data lane.

The interface to the SERDES macro runs at 1/10th the bit rate of the data lane. The MUX/deMUX converts the data rate and bit-width so the FPGA core can run at 1/4th this frequency. This implies a range of 25—78 MHz for the data in and out of the FPGA.

The MUX/deMUX block in the ORT82G5 is a 4-channel block. It provides an interface between each quad channel SERDES and the FPGA logic.

Multichannel Alignment FIFOs

The ORT82G5 has a total of 8 channels (4 per SERDES). The incoming data of these channels can be synchronized in several ways, or they can be independent of one other. For example, all four channels in a SERDES can be aligned together to form a communication channel with a bandwidth of 10 Gbits/s. Alternatively, two channels within a SERDES can be aligned together; channel A and B and/or channel C and D. Optionally, the alignment can be extended across SERDES to align all 8 channels. Individual channels within an alignment group can be disabled (i.e., power down) without disrupting other channels.

XAUI or Fibre-Channel Link State Machine

Two separate link state machines are included in the ORT82G5. A XAUI compliant link state machine is included in the embedded core to implement the *IEEE* 802.3ae v2.1 standard. A separate state machine for fibre-channel is also provided.

Dual Port RAMs

There are two independent memory blocks in the ASB. Each memory block has a capacity of 4k word by 36 bits. It has one read port, one write port, and four byte-write-enable (active-low) signals. The read data from the memory block is registered so that it works as a pipelined synchronous memory block.

ORT82G5 Overview (continued)

FPGA Interface

The FPGA logic will receive/transmit 32-bits of data (up to 78 MHz) and 4-bits of k-ctrl characters (in 8b/10b mode) from/to the embedded core. There are a maximum of 8 such streams in each direction. Data sent to the FPGA can be aligned using comma (/K/) characters or /A/ character (as specified in *IEEE* 802.3ae for XAUI based interfaces). The alignment character is made available to the FPGA along with the data. A comma character is a special character that contains a unique pattern (0011111 or its complement 1100000) in the 10-bit space that makes it useful for delimiting word boundaries. The special characters K28.1, K28.5 and K28.7 contain this comma sequence and are treated as valid comma characters by the SERDES.

If the receive channel alignment FIFOs are bypassed, then each channel will provide its own receive clock in addition to data and k-character detect signals. If the 8b/10b decoders are bypassed, then 40-bit data streams are passed to the FPGA logic. No channel alignment can be done in 8b-/10b-bypass mode. For transmit direction (FPGA to core), data and k-ctrl characters will be sent from FPGA to core for each channel.

FPSC Configuration

Configuration of the ORT82G5 occurs in two stages: FPGA bitstream configuration and embedded core setup.

FPGA Configuration

Prior to becoming operational, the FPGA goes through a sequence of states, including powerup, initialization, configuration, start-up, and operation. The FPGA logic is configured by standard FPGA bit stream configuration means as discussed in the Series 4 FPGA data sheet. The options for the embedded core are set via registers that are accessed through the FPGA system bus. The system bus can be driven by an external *PowerPC* compliant microprocessor via the MPI block or via a user master interface in FPGA logic. A simple IP block, that drives the system by using the user register interface and very little FPGA logic, is available in the *MPI/System Bus Application Note*. This IP block sets up the embedded core via a state machine and allows the ORT82G5 to work in an independent system without an external microprocessor interface.

Backplane Transceiver Core Detailed Description

SERDES

A detailed block diagram of the receive and transmit data paths for a single channel of the SERDES is shown in Figure 3.

The transmitter section accepts either 8-bit unencoded data or 10-bit encoded data at the parallel input port. It also accepts the low-speed reference clock at the REFCLK input and uses this clock to synthesize the internal high-speed serial bit clock. The serialized data are available at the differential CML output terminated in 50 Ω or 75 Ω to drive either an optical transmitter or coaxial media or circuit board/backplane.

The receiver section receives high-speed serial data at its differential CML input port. These data are fed to the clock recovery section which generates a recovered clock and retimes the data. This means that the receive clocks are asynchronous between channels. The retimed data are deserialized and presented as a 10-bit encoded or a 8-bit unencoded parallel data on the output port. Two-phase receive byte clocks are available synchronous with the parallel words. The receiver also optionally recognizes the comma characters or code violations and aligns the bit stream to the proper word boundary.

Bias Section

A fractional band-gap voltage generator is included on the design. An external resistor (3.32 k Ω□ ± 1%), connected between the pins REXT and VSSREXT generates the bias currents within the chip. This resistor should be able to handle at least 300 mA.

Backplane Transceiver Core Detailed Description (continued)

Reset Operation

The SERDES block can be reset in one of three different ways as follows: on power up, using the hardware reset, or via the microprocessor interface. The power up reset process begins when the power supply voltage ramps up to approximately 80% of the nominal value of 1.5 V. Following this event, the device will be ready for normal operation after 3 ms.

A hardware reset is initiated by making the PASB_RESETN low for at least two microprocessor clock cycles. The device will be ready for operation 3 ms after the low to high transition of the PASB_RESETN. This reset function affects all SERDES channels and resets all microprocessor and internal registers and counters.

Using the software reset option, each channel can be individually reset by setting SWRST (bit 2) to a logic 1 in the channel configuration register. The device will be ready 3 ms after the SWRST bit is deasserted. Similarly, all four channels per quad SERDES can be reset by setting the global reset bit GSWRST. The device will be ready for normal operation 3 ms after the GSWRST bit is deasserted. Note that the software reset option resets only SERDES internal registers and counters. The microprocessor registers are not affected. It should also be noted that the embedded block cannot be accessed until after FPGA configuration is complete.

Start Up Sequence

The following sequence is required by the ORT82G5 device. For information required for simulation that may be different than this sequence, see the ORT82G5 design kit.

1. Initiate a hardware reset by making PASB_RESETN low. Keep this low during FPGA configuration of the device. The device will be ready for operation 3 ms after the low to high transition of PASB_RESETN.
2. Configure the following SERDES internal and external registers. Note that after device initialization, all alarm and status bits should be read once to clear them. A subsequent read will provide the valid state. Set the following bits in register 30800:
   — Bits LCKREFN_[AD:AA] to 1, which implies lock to data.
   — Bits ENBYSYNC_[AD:AA] to 1 which enables dynamic alignment to comma.

   Set the following bits in register 30801:
   — Bits LOOPENB_[AD:AA] to 1 if high-speed serial loopback is desired.

   Set the following bits in register 30900:
   — Bits LCKREFN_[BD:BA] to 1 which implies lock to data.
   — Bits ENBYSYNC_[BD:BA] to 1 which enables dynamic alignment to comma.

   Set the following bits in register 30901:
   — Bits LOOPENB_[BD:BA] to 1 if high-speed serial loopback is desired.

   Set the following bits in registers 30002, 30012, 30022, 30032, 30102, 30112, 30122, 30132:
   — TXHR set to 1 if TX half-rate is desired.
   — 8B10BT set to 1

   Set the following bits in registers 30003, 30013, 30023, 30033, 30103, 30113, 30123, 30133:
   — RXHR Set to 1 if RX half-rate is desired.
   — 8B10BR set to 1.

   Assert GSWRST bit by writing two 1's. Deassert GSWRST bit by writing two 0's.
   Wait 3ms. If higher speed serial loopback has been selected, the receive PLLs will use this time to lock to the new serial data.

   Monitor the following alarm bits in registers 30000, 30010, 30020, 30030, 30110, 30120, 30130:
   — LKI-PLL lock indicator. 1 indicates that PLL has achieved lock.
3. If 8b/10b mode is enabled, enable link synchronization by sending the following sequence three times:
   — K28.5 D21.4 D21.5 D21.5

Backplane Transceiver Core Detailed Description (continued)

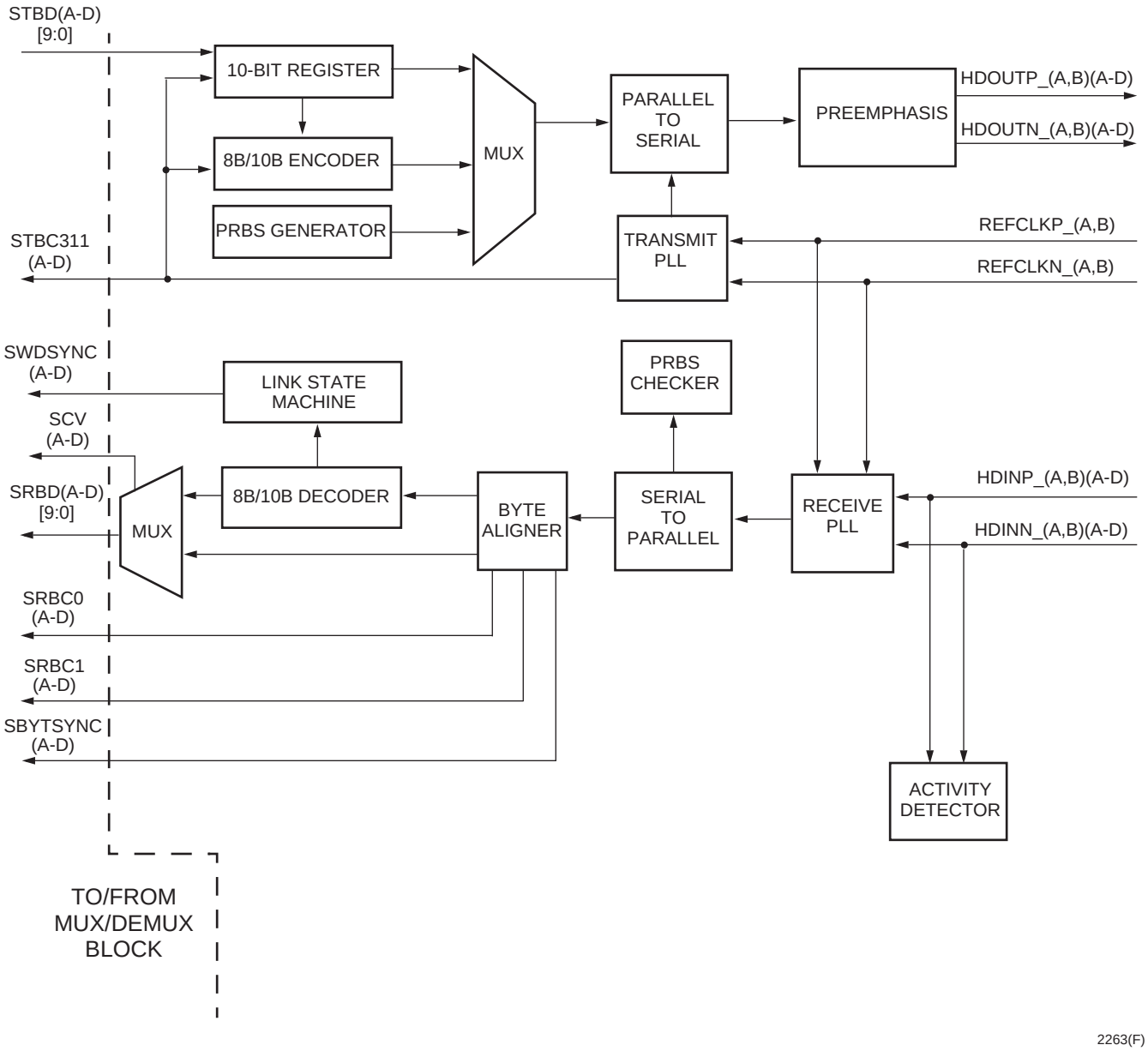

Figure 3. SERDES Functional Block Diagram for One Channel

Backplane Transceiver Core Detailed Description (continued)

SERDES Transmit Path (FPGA » Backplane)

The transmitter section accepts either 8-bit unencoded data or 10-bit encoded data at the parallel input port from the MUX/deMUX block. It also accepts the low-speed reference clock at the REFCLK input and uses this clock to synthesize the internal high-speed serial bit clock.

The serialized data are available at the differential CML output terminated in 50 Ω or 75 Ω to drive either an optical transmitter, coaxial media, or circuit board/backplane.

Each channel includes a PRBS generator that is available for various test capabilities on the device.

The STBDx[8:0] (where x is a placeholder for one of the letters, A—D) ports carry unencoded character data in this design. The time-division multiplexer in the ORT82G5 is only 9 bits wide. The 10th bit (STBDx[9]) of each data lane into the SERDES is held constant. It is not possible to use the ORT82G5 for normal data communication without enabling SERDES 8b/10b encoding.

The functional mode uses the STBCx311 SERDES output as the reference clock. The frequency of this clock will depend on the half-rate/full-rate control bit in the SERDES; and the frequency of the REFCLK ports and/or that of the high-speed serial data. The SERDES TBCKSEL control bit must be configured to a 0 for each channel in order for this clocking strategy to work.

A falling edge on the STBC311x clock port will cause a new data character to be sent from STBDx[9:0] to the SERDES block with a latency of 5 STBC311x clock cycles at the high-speed serial output.

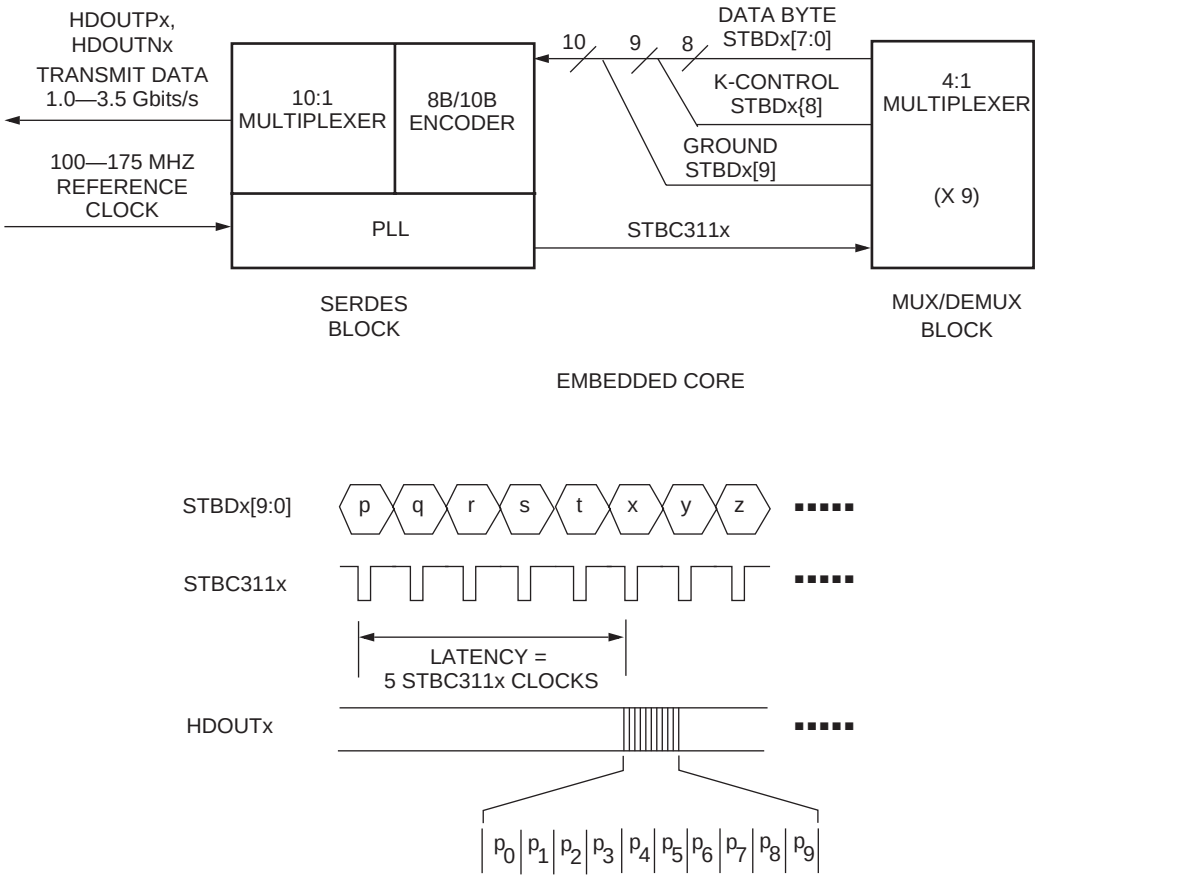

Figure 4. ORT82G5 Transmit Path for a Single SERDES Channel

Backplane Transceiver Core Detailed Description (continued)

Transmit Preemphasis and Amplitude Control

The transmitter's CML output buffer is terminated on-chip to optimize the data eye as well as to reduce the number of discrete components required. The differential output swing reaches a maximum of 1.2 V_{PP} in the normal amplitude mode. A half amplitude mode can be selected via configuration register bit HAMP. Half amplitude mode can be used to reduce power dissipation when the transmission medium has minimal attenuation.

A programmable preemphasis circuit is provided to boost the high frequencies in the transmit data signal to maximize the data eye opening at the far-end receiver. Preemphasis is particularly useful when the data are transmitted over backplanes or low-quality coax cables. The degree of preemphasis can be programmed with a two-bit control from the microprocessor interface as shown in Table 2. The high-pass transfer function of the preemphasis circuit is shown below, where the value of a is shown in Table 2.

$H(z) = (1 - az^{-1})$

Table 2. Preemphasis Settings

PE1	PE0	Amount of Preemphasis (a)
0	0	0% (No Preemphasis)
0	1	12.5%
1	0	12.5%
1	1	25%

SERDES Receive Path (Backplane » FPGA)

The receiver section receives high-speed serial data at its differential CML input port. These data are fed to the clock recovery section which generates a recovered clock and retimes the data. This means that the receive clocks are asynchronous between channels. The retimed data are deserialized and presented as a 10-bit encoded or a 8-bit unencoded parallel data on the output port. Two-phase receive byte clocks are available synchronous with the parallel words. The receiver also recognizes the comma characters and aligns the bit stream to the proper word boundary.

The receive PLL has two modes of operation as follows: lock to reference and lock to data with retiming. When no data or invalid data is present on the HDINP and HDINN pins, the receive VCO will not lock to data and its frequency can drift outside of the nominal ±100 ppm range. Under this condition, the receive PLL will lock to REFCLK for a fixed time interval and then will attempt to lock to receive data. The process of attempting to lock to data, then locking to clock will repeat until valid input data exists. There is also a control register bit per channel to force the receive PLL to always lock to the reference clock.

The activity detector monitors the presence of data on each of the differential high-speed input pins. In the absence of amplitude qualified data on the inputs the chip automatically goes into sleep mode and receiver is powered-down. This function can, however, be disabled through the control interface. The chip automatically becomes active when active data is detected on the serial inputs and valid data can be received after the receive PLL has locked to the input data frequency.

The PRBS checker is a built-in bit error rate tester (BERT). When enabled, it produces a one-bit PRBSCHK output to indicate whether there was an error in the loopback data.

Backplane Transceiver Core Detailed Description (continued)

Data from a SERDES channel appears in 10-bit raw form or 8-bit decoded form at the SRBDx[9:0] port (where x is a placeholder for one of the letters, A-D) with a latency of approximately 14-23 cycles. Accompanying this data are the comma-character indicator (SBYTSYNCx), clocks (SRBC0x, and SRBC1x), link-state indicator (SWDSYNCx), and code-violation indicator (SCVx).

With the 8B10BR control bit of the SERDES channel set to 1, the data presented at SRBDx[9:0] will be decoded characters. Bit 8 will indicate whether SRBDx[7:0] represents an ordinary data character (bit 8 = 0), or whether SRBDx[7:0] represents a special character, like a comma. When 8B10BR is set to 0, the data at SRBDx[9:0] will be encoded characters. The XAUI link-state machine should not be used in this mode of operation. When in XAUI mode, the MUX/deMUX looks for /A/ (as defined in *IEEE* 802.3ae v.2.1) characters for channel alignment and requires the characters to be in decoded form for this to work.

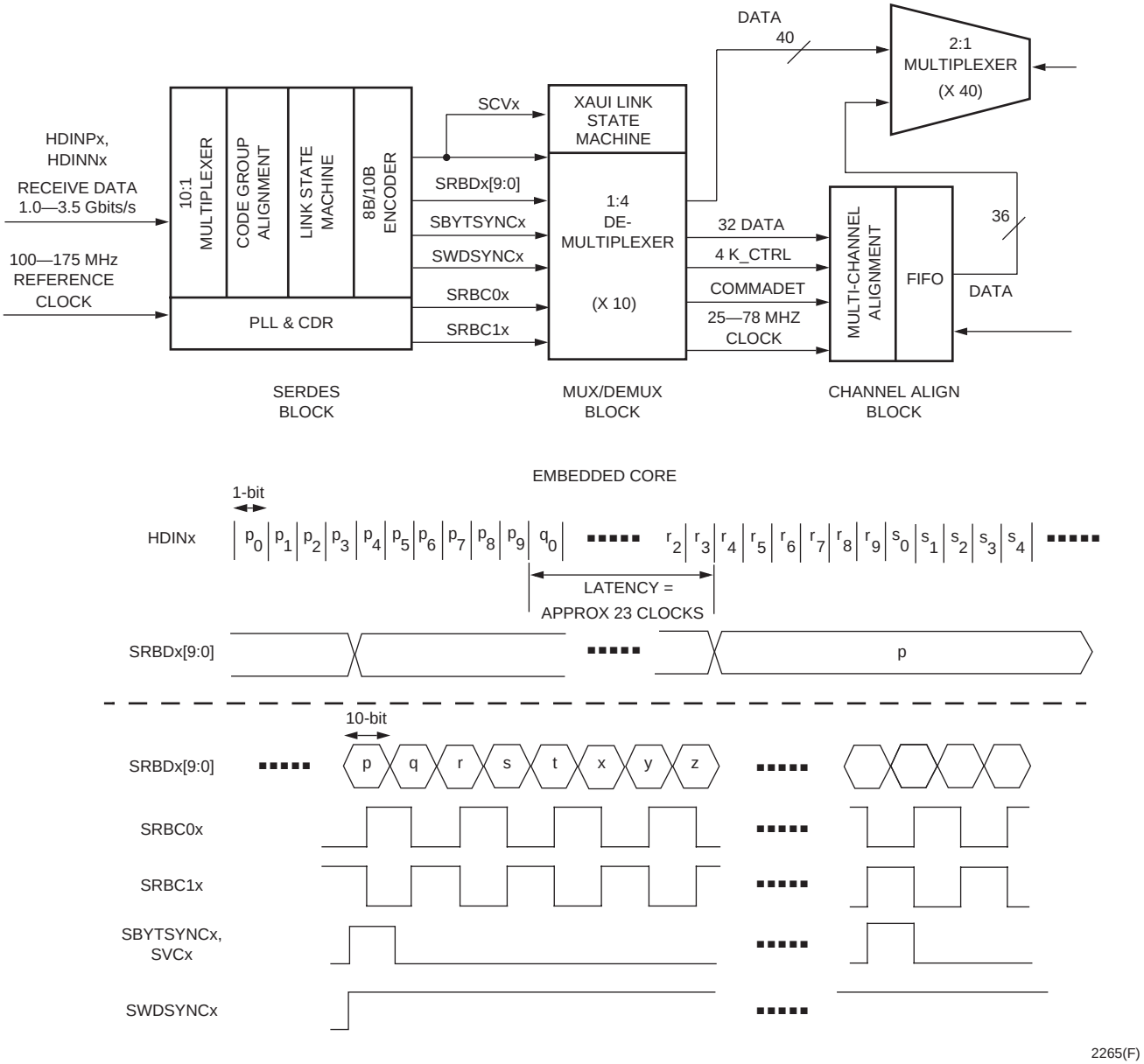

Figure 5. ORT82G5 Receive Path for a Single SERDES Channel

Backplane Transceiver Core Detailed Description (continued)

8b/10b Encoding

The 8b/10b encoder encodes the incoming 8-bit data into a 10-bit format according to the FC-PH ANSI X3.230:1994 standard. Input pins SRBDx<7:0> (where x is a placeholder for one of the letters, A—D) are used for 8 bit unencoded data and SRBDx<8> is used as the K_control input to indicate whether the 8 data bits need to be encoded as special characters (K_control = 1) or as data characters (K_control = 0). When the encoder is bypassed SRBDx<9:0>serve as the data bits for the 10-bit encoded data. The following table shows two different codings that are possible for each data value and are shown as encoded word(+) and encoded word (-). The transmitter selects between (+) and (-) encoded word based on calculated disparity of the present data.

Table 3. Valid Special Characters

K character	HGF EDCBA 765 43210	K control	Encoded Word (–)	Encoded Word (+)
			abcdei fghj	abcdei fghj
K28.0	000 11100	1	001111 0100	110000 1011
K28.1	001 11100	1	001111 1001	110000 0110
K28.2	010 11100	1	001111 0101	110000 1010
K28.3	011 11100	1	001111 0011	110000 1100
K28.4	100 11100	1	001111 0010	110000 1101
K28.5	101 11100	1	001111 1010	110000 0101
K28.6	110 11100	1	001111 0110	110000 1001
K28.7	111 11100	1	001111 1000	110000 0111
K23.7	111 10111	1	111010 1000	000101 0111
K27.7	111 11011	1	110110 1000	001001 0111
K29.7	111 11101	1	101110 1000	010001 0111
K30.7	111 11110	1	011110 1000	100001 0111

Within the definition of the 8b/10b transmission code, the bit positions of the 10-bit encoded transmission characters are labeled as a, b, c, d, e, i, f, g, h, and j in that order. Bit a corresponds to SRBDx[0], bit b to SRBDx[1], bit c to SRBDx[2], bit d to SRBDx[3], bit e to SRBDx[4], bit i to SRBDx[5], bit f to SRBDx[6], bit g to SRBDx[7], bit h to SRBDx[8], and bit j to SRBDx[9]. The data SRBDx[9:0] is transmitted serially with SRBDx[0] transmitted first and SRBDx[9] transmitted last.

For an 8-bit unencoded data, the 8-bit unencoded data SRDBx[7:0] is represented as HGF EDCBA SRDBx[8] represents the K_CTRL bit and SRDBx[9] is unused. SRBDx[0] is still transmitted first and SRBDx[9] transmitted last.

8b/10b Decoding

A 8b/10b decoder block is available to allow for receiving data that has been encoded using a standard 8B/10B encoder. This encoding/decoding scheme also allows for the transmission of special characters and allows for error detection.

Clock recovery for the 8B/10B decoder is performed by the SERDES block for each of the eight receive channels. This recovered data is then aligned to a 10-bit word boundary by detecting and aligning to the comma codeword. Word alignment is done to either polarity of this codeword. The 10-bit code word is passed to the decoder, which provides an 8-bit byte of data and a SBYTSYNC signal.

Backplane Transceiver Core Detailed Description (continued)

SERDES Transmit and Receive PLLs

The high-speed transmit and receive serial data can operate at 1.0—1.25 Gbits/s or 2.0—3.125 Gbits/s depending on the state of the control bits from the microprocessor interface. Table 4 shows the relationship between the data rates, the reference clock, and the transmit TWCKx clocks.

The receiver section receives high-speed serial data at its differential CML input port. These data are fed to the clock recovery section which generates a recovered clock and retimes the data. This means that the receive clocks are asynchronous between channels. The retimed data are deserialized and presented as a 10-bit encoded or a 8-bit unencoded parallel data on the output port. RWCKx receive byte clocks are available synchronous with the parallel words. The receiver also recognizes the comma characters and aligns the bit stream to the proper word boundary.

Table 5 shows the relationship between the data rates, the reference clock, and the RWCKx clocks.

Table 4. Transmit PLL Clock and Data Rates

Data Rate	Reference Clock	TCK78[A, B] Clock	Rate
1.0 Gbits/s	100 MHz	25 MHz	Half
1.25 Gbits/s	125 MHz	31.25 MHz	Half
2.0 Gbits/s	100 MHz	50 MHz	Full
2.5 Gbits/s	125 MHz	62.5 MHz	Full
3.125 Gbits/s	156 MHz	78 MHz	Full
3.5 Gbits/s	175 MHz	87.5 MHz	Full

Note: The selection of full-rate or half-rate for a given reference clock speed is set by a bit in the transmit control register and can be set per channel.

Table 5. Receive PLL Clock and Data Rates

Data Rate	Reference Clock	RWCKx Clocks	Rate
1.0 Gbits/s	100 MHz	25 MHz	Half
1.25 Gbits/s	125 MHz	31.25 MHz	Half
2.0 Gbits/s	100 MHz	50 MHz	Full
2.5 Gbits/s	125 MHz	62.5 MHz	Full
3.125 Gbits/s	156 MHz	78 MHz	Full
3.5 Gbits/s	175 MHz	87.5 MHz	Full

Note: The selection of full-rate or half-rate for a given reference clock speed is set by a bit in the receive control register and can be set per channel.

Reference Clock

There are two pairs of reference clock inputs on the ORT82G5. The differential reference clock is distributed to all four channels in a quad. Each channel has a differential buffer to isolate the clock from the other channels. The input clock is preferably a differential signal; however, the device can operate with a single-ended input. The input reference clock directly impacts the transmit data eye, so the clock should have low jitter. In particular, jitter components in the dc—5 MHz range should be minimized.

Note: The reference clock, REFCLK, is equivalent to REFINP and REFINN; throughout the text simply refer to the reference clock as REFCLK.

For more information on the reference clock input requirements and connections to either single ended or differential inputs, see the *SERDES* reference clock application note.

Backplane Transceiver Core Detailed Description (continued)

Byte Alignment

When ENBYSYNC = 1, the ORT82G5 recognizes the comma sequence and aligns the 10-bit comma containing character to the word boundary. BYTSYNC = 1 when the parallel output word contains a byte-aligned comma containing character. The BYTSYNC flag will continue to pulse a logic 1 whenever a byte aligned comma containing character is at the parallel output port.

Link State Machines

Two link state machines are included in the ORT82G5, one for XAUI applications and a second for fibre-channel applications.

The fibre-channel link state machine is responsible for establishing a valid link between the transmitter and the receiver and for maintaining link synchronization. The machine wakes up in the loss of synchronization state upon powerup reset. This is indicated by WDSYNC = 0. While in this state, the machine looks for a particular number of consecutive idle ordered sets without any invalid data transmission in between before declaring synchronization achieved. Synchronization achieved is indicated by asserting WDSYNC = 1. Specifically, the machine looks for three continuous idle ordered sets without any misaligned comma character or any running disparity based code violation in between. In the event of any such code violation, the machine would reset itself to the ground state and start its search for the idle ordered sets again. An example of a valid sequence for achieving link synchronization would be K28.5 D21.4 D21.5 D21.5 repeated 3 times.

In the synchronization achieved state, the machine constantly monitors the received data and looks for any kind of code violation that might result due to running disparity errors. If it were to receive four such consecutive invalid words, the link machine loses its synchronization and once again enters the loss of synchronization state (LOS). A pair of valid words received by the machine overcomes the effect of a previously encountered code violation. LOS is indicated by the status of WDSYNC output which now transitions from 1 to 0. At this point the machine attempts to establish the link yet again. Figure 6 shows the state diagram for the fibre-channel link state machine.

In the ORT82G5 LOS is indicated by DEMUXWAS_[AA, AB,... BD] register bit. This bit is 0 during LOS.

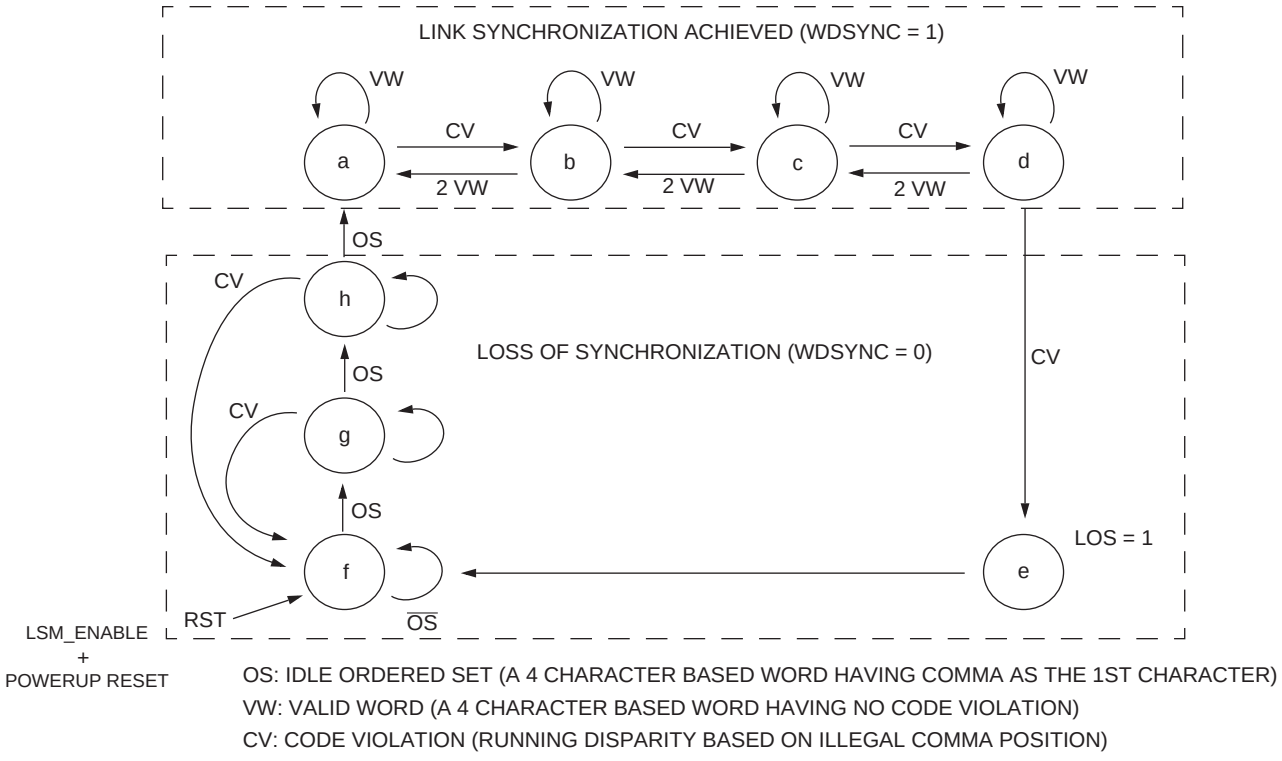

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Figure 6. Fibre-Channel Link State Machine State Diagram

Backplane Transceiver Core Detailed Description (continued)

XAUI Link Synchronization Function

For each lane, the receive section of the XAUI link state machine incorporates a synchronization state machine that monitors the status of the 10-bit alignment. A 10-bit alignment is done in the SERDES based on a comma character such as K28.5. A comma (0011111 or its complement 1100000) is a unique pattern in the 10-bit space that cannot appear across the boundary between any two valid 10-bit code-groups. This property makes the comma useful for delimiting code-groups in a serial stream.This mechanism incorporates a hysteresis to prevent false synchronization and loss of synchronization due to infrequent bit errors. For each lane, the sync_complete signal is disabled until the lane achieves synchronization. The synchronization state diagram is shown in Figure 1. Table 1 and Table 2 describe the state variables used in Figure 1.

Table 6. XAUI Link Synchronization State Diagram Notation—Variables

Variable	Description
sync_status	FAIL: Lane is not synchronized (correct 10-bit alignment has not been established). OK: Lane is synchronized. OK_NOC: Lane is synchronized but a comma character has not been detected in the past TBD seconds.
enable_CDET	TRUE: Align subsequent 10-bit words to the boundary indicated by the next received comma. FALSE: Maintain current 10-bit alignment.
gd_cg	Current number of consecutive cg_good indications.

Table 7. XAUI Link Synchronization State Diagram—Functions

Function	Description
sync_complete	Indication that alignment code-group alignment has been established at the boundary indicated by the most recently received comma.
cg_comma	Indication that a valid code-group, with correct running disparity, containing a comma has been received.
cg_good	Indication that a valid code-group with the correct running disparity has been received.
cg_bad	Indication that an invalid code-group has been received.
no_comma	Indication that comma timer has expired. The timer is initialized upon receipt of a comma.

Backplane Transceiver Core Detailed Description (continued)

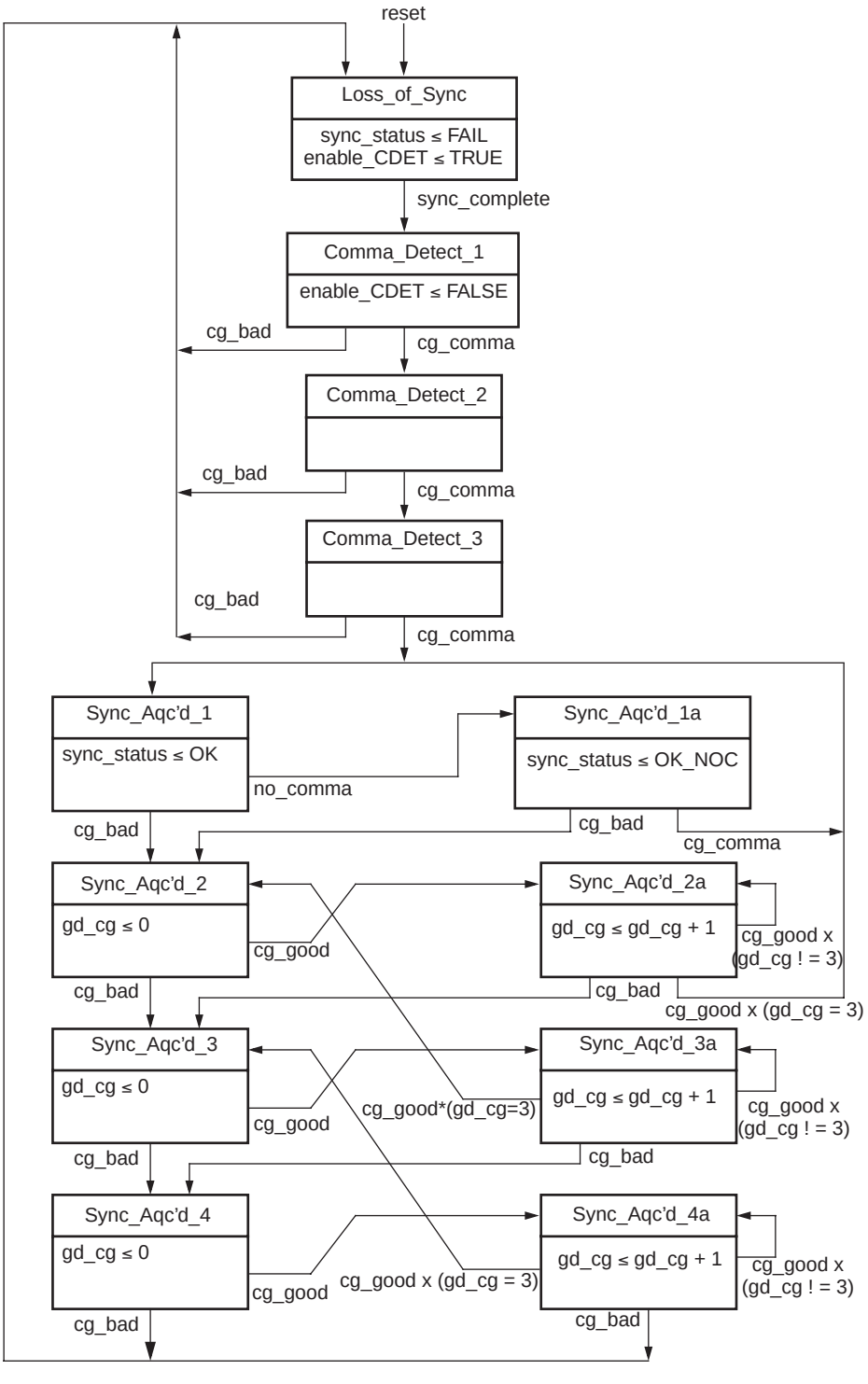

Figure 7. XAUI Link Synchronization State Diagram

Backplane Transceiver Core Detailed Description (continued)

MUX/DeMUX Block

Transmit Path (FPGA » Backplane)

The MUX is responsible for taking 36 bits of data/control at the low-speed transmit interface and up-converting it to 9 bits of data/control at the SERDES transmit interface.

The MUX has 2 clock domains: one based on a clock received from the SERDES; the other that comes from the FPGA at 1/4 the frequency of the SERDES clock. The time sequence of interleaving data/control values is shown in Figure 8 below.

The low-speed transmit interface consists of a clock, 4 data byte values and a control bit for each of the byte values. The data bytes are conveyed to the MUX via the TWDx[31:0] ports. The control bits are TCOMMAx[3:0]. The clock is TSYS_CLK_[AA, AB, AC.... BD] or TSYS_CLK_x for the sake of brevity.

Both the data and control are strobed into the MUX at this interface on the rising edge of TSYS_CLK_x. Besides taking in a clock for capture, the interface sends back a clock of the same frequency, but arbitrary phase. This clock, TCK78(A,B), is derived from one of the 4 channels of MUX. Within each MUX is a divide-by-4 of the SERDES STBC311x clock used in synchronizing the transmit data words to the STBC311x clock domain. TCKSEL bits select the source channel of TCK78. The selection of clock source for TCK78(A,B) is shown in Table 8.

Table 8. TCK78 selection

TCKSEL0	TCKSEL1	Clock Source
0	0	Channel A
1	0	Channel B
0	1	Channel C
1	1	Channel D

Backplane Transceiver Core Detailed Description (continued)

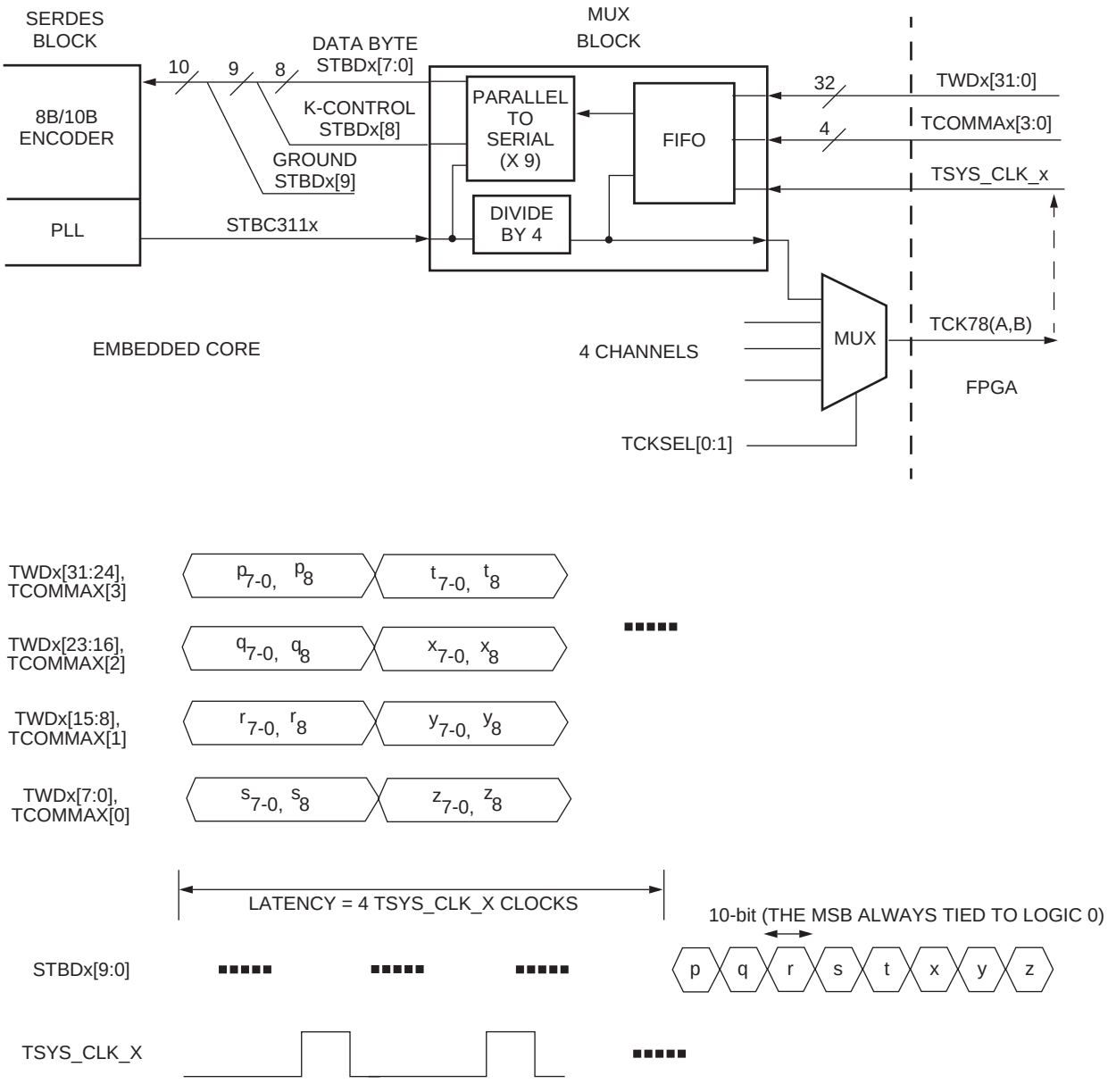

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Figure 8. Transmit MUX Block for a Single SERDES Channel

Backplane Transceiver Core Detailed Description (continued)

Receive Path (Backplane » FPGA)

The deMUX has to accumulate four sets of characters presented to it at the SERDES receive interface and put these out at one time at the low-speed receive interface.

Another task of the deMUX is to recognize the synchronizing event and adjust the 4-byte boundary so that the synchronizing character leads off a new 4-byte word. Typically, this synchronizing character is a comma. This feature will be referred to as deMUX word alignment in other areas of this document. DeMUX word alignment will only occur when the communication channel is synchronized. When there is no synchronization of the link, the deMUX will continue to output 4-byte words at some arbitrary, but constant, boundary.

There are 2 controls available to each channel for word alignment. They are DOWDALGN and NOWDALGN. The DOWDALGN bit is positive edge triggered. Writing a 0 followed by a 1 to this register bit will cause the deMUX to look for a new comma character and align the 32-bit word such that the comma is in the most significant byte position. It is important that the comma is in the most significant byte position since the multi-channel aligner looks for comma in the most significant byte only. Typically, it is not necessary to set the DOWDALGN bit. When the link state machine loses synchronization (DEMUXWAS register bit is 0), the deMUX block automatically looks for a new comma character irrespective of whether the DOWDALGN bit is set or not. A scenario where the DOWDALGN bit can be set is when no channel alignment happens for sometime and one of the reasons could be that there is no comma character in the most significant byte position. There can be a loss of data from creating a new word boundary based on a comma.

The NOWDALGN bit is a level-sensitive bit. If it is a 1, then the deMUX does not dynamically alter the word boundary based on comma and SWDSYNCx output of the SERDES. This might be useful if a channel were configured to bypass the multi-channel alignment FIFO and raw 40-bits of data are directed from SERDES to FPGA. The default (NOWDALGN = 0) causes the word boundary to be set as soon as the SERDES SWDSYNCx output is a 1 and a comma character has been detected. The character that is the comma becomes the most-significant portion of the demultiplexed word. When the SERDES loses link synchronization it will drop SWDSYNCx low. The deMUX will begin search for word alignment as soon as SWDSYNCx goes to 1 again.

The deMUX passes on to the channel alignment FIFO block a set of control signals that indicate the location of the synchronizing event. RCOMMAx[3:0] are these indicators. If there is no link synchronization, all of the RCOMMAx[3:0] bits will be 0s independent of synchronizing events that come in. When the link is synchronized, then the bit that corresponds to the time of the synchronization event will be set to a 1.

The relationship between a time sequence of values input at SRBDx[7:0] to the values output at RWDx[31:0] is shown in Figure 9 below. A parallel relationship exists between SRBDx[8] and RWBIT8x[3:0] as well as between SRBDx[9] and RWBIT9x[3:0].

One clock per bank of 4 channels called RCK78(A,B) is sent to the FPGA. The control bits RCKSEL(A,B) are used to select the clock source for these clocks. The selection of clock source for RCK78(A,B) is shown in Table 9.

Table 9. RCK78 Selection

RCKSEL0	RCKSEL1	Clock Source
0	0	Channel A
1	0	Channel B
0	1	Channel C
1	1	Channel D

Backplane Transceiver Core Detailed Description (continued)

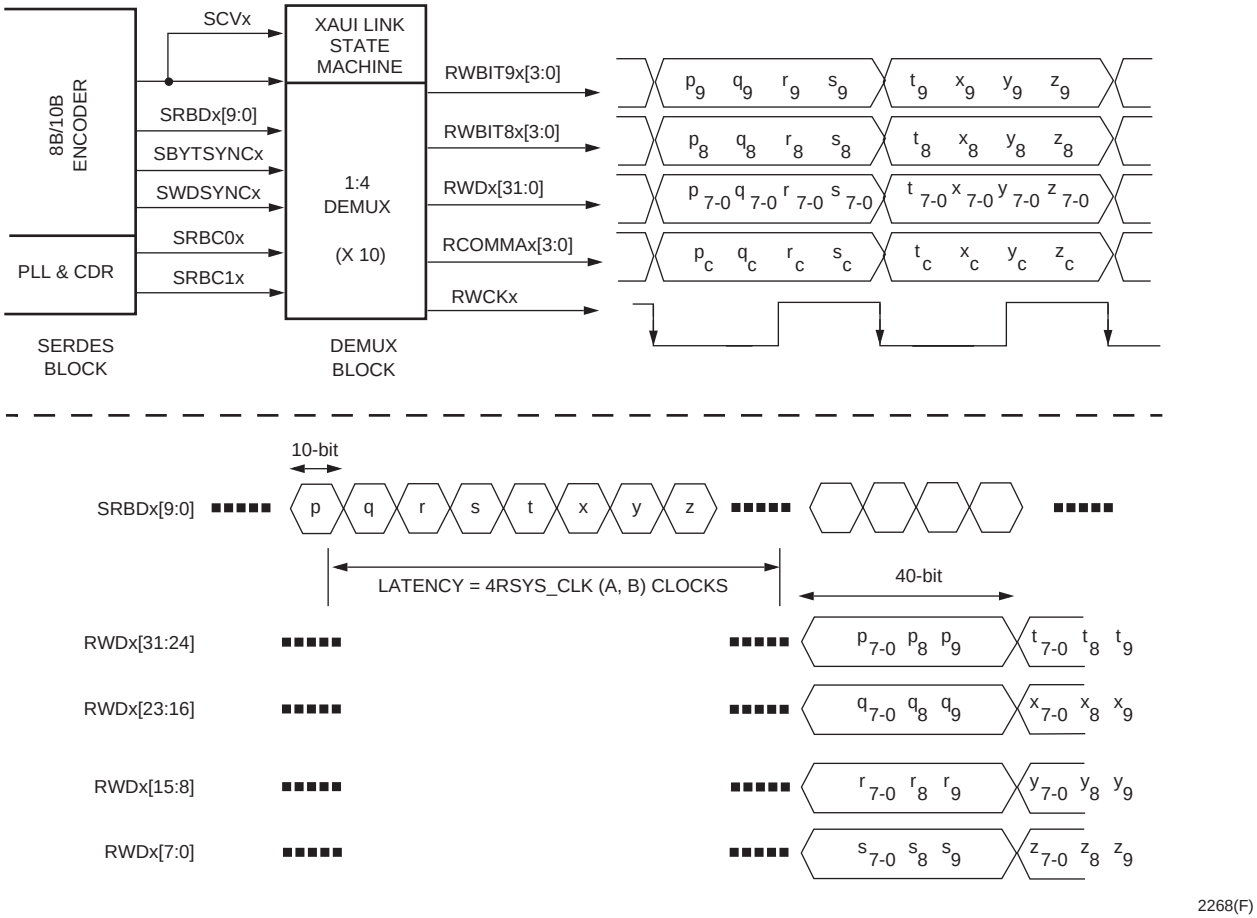


Figure 9. Receive DeMUX Block for a Single SERDES Channel

Backplane Transceiver Core Detailed Description (continued)

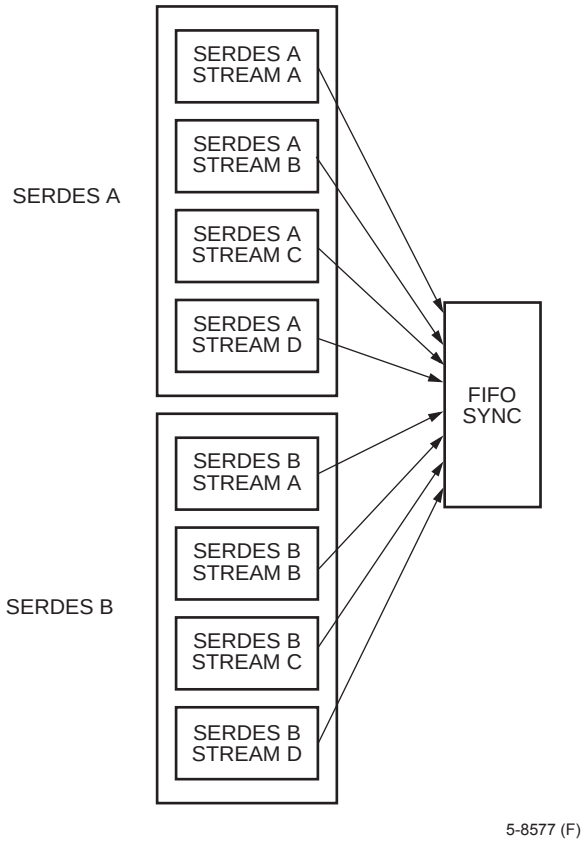


Figure 10. Interconnect of Streams for FIFO Alignment

Multichannel Alignment (Backplane » FPGA)

The alignment FIFO allows the transfer of all data to the system clock. The FIFO sync block (Figure 10) allows the system to be configured to allow the frame alignment of multiple slightly varying data streams. This optional alignment ensures that matching SERDES streams will arrive at the FPGA end in perfect data sync.

The ORT82G5 has a total of 8 channels (4 per SERDES). The incoming data of these channels can be synchronized in several ways, or they can be independent of one other. For example, all four channels in a SERDES can be aligned together to form a communication channel with a bandwidth of 10 Gbits/s as shown in Figure 11.

Optionally, the alignment can be extended across SERDES to align all 8 channels in ORT82G5 as shown in Figure 12. Individual channels within an alignment group can be disabled (i.e., power down) without disrupting other channels.

Alternatively, two channels within a SERDES can be aligned together; channel A and B and/or channel C and D can form a pair as shown in Figure 13.

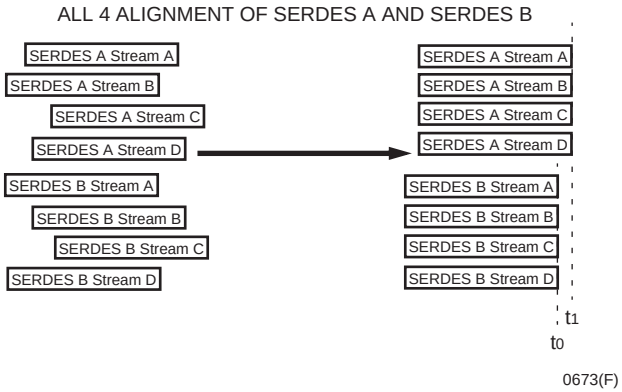


Figure 11. Example of SERDES A Alignment and SERDES B Alignment

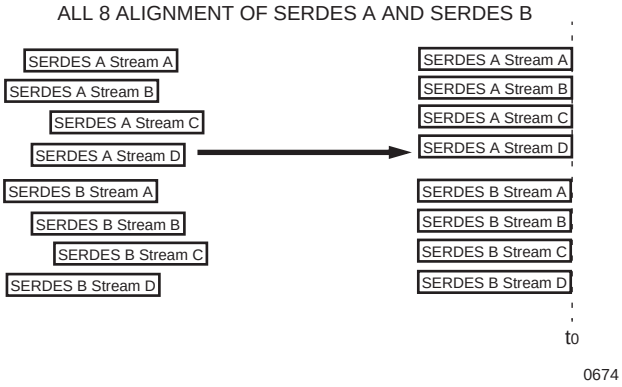
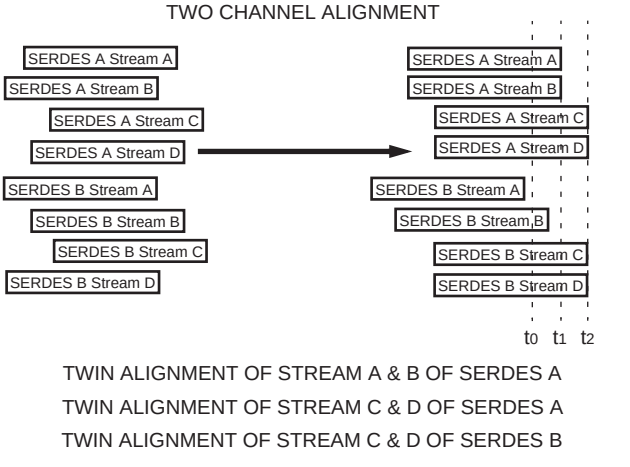


Figure 12. Example of SERDES A and B Alignment



Note: Streams A and B of SERDES B are not aligned.

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Figure 13. Example of Multiple Twin Channel Alignment

Backplane Transceiver Core Detailed Description (continued)

The de-multiplexed, receive word outputs to the FPGA are shown in Figure 14. These are each 40 bits wide. There are eight of these interfaces, one for each data lane. Each consist of four 10-bit characters, or four decoded characters (each 8 bits + 1 bit K_CTRL) + CH248_SYNCx status indicator bit depending on setting of NOCHALGNx control register bits. The NOCHALGNx register bit decides whether data into the FPGA (MRWDxy] comes from the channel alignment FIFOs or deMUX block. Note that there is one control bit for a bank of channels, for a total of two control bits. Also, note that while 10 bits are provided for each character when NOCHALGNx = 1, only the lower 9 bits of each character will be meaningful if the 8B10BR bit is configured to 1 for that SERDES channel.

With x representing the bank (placeholder for A or B) and y representing the channel (placeholder for A, B, C, or D) the 40-bit MRWDxy[39:0] is allocated as in Table 10.

In the receive path, each channel is provided with a 24 word x 36-bit FIFO. The FIFO can perform two tasks: (1) to change the clock domain from receive clock to a clock from the FPGA side, and (2) to align the receive data over 2, 4, or 8 channels. This FIFO allows a timing budget of +/- 230.4 ns that can be allocated to skew between the data lanes and for transfer to the system clock. The input to the FIFO consists of 36-bit demultiplexed data, RWBYTESYNC[3:0], RWDx[31:0], and RWBIT8x[3:0].

The four RWBYTESYNC bits are control signals, e.g., they can be the COMMADET signals indicating the presence of COMMA character. The other 32 RWD bits are the 4 characters from the 8b/10b decoder. The RWBIT8 indicates the presence of Km.n control character in the receive data byte. Only RWBIT8 and RWD inputs are stored in the FIFO. During alignment process, RWBYTESYNC[3] is used to synchronize multiple channels. If a channel is not in any alignment group, it will set the FIFO-write-address to the beginning of the FIFO, and will set the FIFO-read-address to the middle of the FIFO, at the first assertion of RWBYTESYNC[3] after reset or after the resync command.

The RX_FIFO_MIN register bits can be used to control the threshold for minimum unused buffer space in the alignment FIFOs between read and write pointers before OVFL status is flagged. The synchronization algorithm consists of a down counter which starts to count down by 1 from its initial value of 18 (decimal) when an alignment character from any channel within an alignment group has been received. When alignment characters from all channels within the alignment group have been received and count < RX_FIFO_MIN, an OVFL status is flagged. Once the alignment characters within the alignment group have been received, the count is decremented by 2 until 0 is reached. Data is then read from the FIFOs and output to the FPGA.

For every alignment group, there is an OVFL and OOS status register bit. The OOS bit is flagged when the down counter in the synchronization algorithm has reached a value of 0 and alignment characters from all channels within an alignment group have not been received. In the memory map section OOS is referred to as SYNC[2,4]_[A1,A2,B1,B2]_OOS, SYNC8_OOS. OVFL is referred to as SYNC[2,4]_[A1,A2,B1,B2]_OVFL, SYNC8_OVFL.

Backplane Transceiver Core Detailed Description (continued)

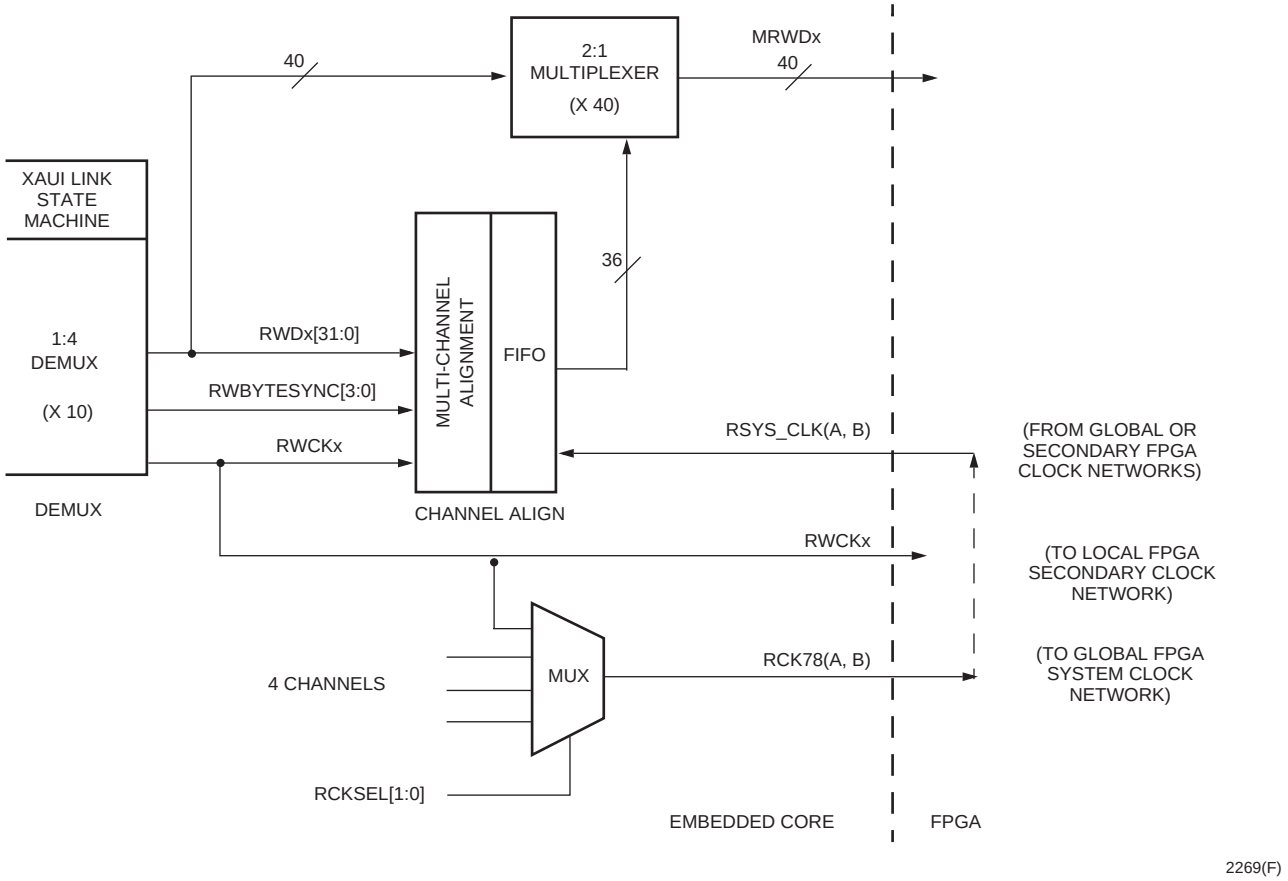

Figure 14. Multichannel Alignment FIFO Block for a Single SERDES Channel

Backplane Transceiver Core Detailed Description (continued)

Table 10. Definition of Bits of MRWDxy[39:0]

Bit Index	NOCHALGNx = 1	NOCHALGNx = 0
39	b9 of char 1	CH248_SYNCx
38	b8 of char 1	K_CTRL for char 1
37	b7 of char 1	b7 of char 1
36	b6 of char 1	b6 of char 1
35	b5 of char 1	b5 of char 1
34	b4 of char 1	b4 of char 1
33	b3 of char 1	b3 of char 1
32	b2 of char 1	b2 of char 1
31	b1 of char 1	b1 of char 1
30	b0 of char 1	b0 of char 1
29	b9 of char 2	n/c
28	b8 of char 2	K_CTRL for char 2
27	b7 of char 2	b7 of char 2
26	b6 of char 2	b6 of char 2
25	b5 of char 2	b5 of char 2
24	b4 of char 2	b4 of char 2
23	b3 of char 2	b3 of char 2
22	b2 of char 2	b2 of char 2
21	b1 of char 2	b1 of char 2
20	b0 of char 2	b0 of char 2
19	b9 of char 3	n/c
18	b8 of char 3	K_CTRL for char 3
17	b7 of char 3	b7 of char 3
16	b6 of char 3	b6 of char 3
15	b5 of char 3	b5 of char 3
14	b4 of char 3	b4 of char 3
13	b3 of char 3	b3 of char 3
12	b2 of char 3	b2 of char 3
11	b1 of char 3	b1 of char 3
10	b0 of char 3	b0 of char 3
09	b9 of char 4	n/c
08	b8 of char 4	K_CTRL for char 4
07	b7 of char 4	b7 of char 4
06	b6 of char 4	b6 of char 4
05	b5 of char 4	b5 of char 4
04	b4 of char 4	b4 of char 4
03	b3 of char 4	b3 of char 4
02	b2 of char 4	b2 of char 4
01	b1 of char 4	b1 of char 4
00	b0 of char 4	b0 of char 4

The use of the FIFO is controlled by configuration bits, and the raw demultiplexed data can also be sent to the FPGA directly, by passing the alignment FIFO. The control register bits for alignment FIFO in ORT82G5 are described below.

Table 11. Multichannel Alignment Modes

Register Bits FMPU_SYNMODE_xx [0:1]	Mode
00	No multichannel alignment.
10	Twin channel alignment.
01	Quad channel alignment.
11	Eight channel alignment.

Note: Where xx is one of A[A:D] and B[A:D].

To align all eight channels:

- FMPU_SYNMODE_A[A:D] = 11
- FMPU_SYNMODE_B[A:D] = 11

To align all four channels in SERDES A:

- FMPU_SYNMODE_A[A:D] = 01

To align two channels in SERDES A:

- FMPU_SYNMODE_A[A:B] = 10 for channel AA and AB
- FMPU_SYNMODE_A[C:D] = 10 for channel AC and AD

Similar alignment can be defined for SERDES B.

To enable/disable synchronization signal of individual channel within a multi-channel alignment group:

- FMPU_STR_EN_xx = 1 enabled
- FMPU_STR_EN_xx = 0 disabled
  where xx is one of A[A:D] and B[A:D].

Backplane Transceiver Core Detailed Description (continued)

To resynchronize a multichannel alignment group set the following bit to zero, and then set it to 1.

- FMPU_RESYNC8 for eight channel A[A:D] and B[A:D]
- FMPU_RESYNC4A for quad channel A[A:D]
- FMPU_RESYNC2A1 for twin channel A[A:B]
- FMPU_RESYNC2A2 for twin channel A[C:D]
- FMPU_RESYNC4B for quad channel B[A:D]
- FMPU_RESYNC2B1 for twin channel B[A:B]
- FMPU_RESYNC2B2 for twin channel B[C:D]

To resynchronize an independent channel (resetting the write and the read pointer of the FIFO) set the following bit to zero, and then set it to 1.

- FMPU_RESYNC1_xx where xx is one of A[A:D] and B[A:D]

A two-to-one multiplexor is used to select between aligned or nonaligned data to be sent to the FPGA on MRWDxy[39:0]. With x representing the bank (placeholder for A or B) and y representing the channel (placeholder for A, B, C or D), the 40-bit MRWDxy[39:0] is allocated as shown in Table 10.

Alignment Sequence

1. Follow steps 1 and 2 in the start up sequence described previously.
2. Initiate a SERDES software reset by setting the SWRST bit to 1 and then to 0. Note that, any changes to the SERDES configuration bits should be followed by a software reset.
3. Wait for 3 ms. REFCLK should be toggling by this time. During this time, configure the following registers.

   Set the following bits in registers 30820, 30920

   - XAUI_MODEx-set to 1 for XAUI mode or keep the default value of 0.

   Enable channel alignment by setting FMPU_SYNMODE bits in registers 30811, 30911.

   - FMPU_SYNMODE_xx. Set to appropriate values for 2, 4, or 8 alignment based on Table 11.

   Set RCLKSELx and TCKSELx bits in registers 30A00.

- RCKSELx-choose clock source for 78 MHz RCK78x (Table 9).
  - TCKSELx-Choose clock source for 78 MHz TCK78x (Table 8).

4. Send data on serial links. Monitor the following status/alarm bits:

   Monitor the following alarm bits in registers 30000, 30010, 30020, 30030, 30100, 30110, 30120, 30130.

   - LKI-PLL lock indicator. A 1 indicates that PLL has achieved lock.

   Monitor the following status bits in registers 30804, 30904

   - XAUISTAT_xx - In XAUI mode, they should be 10.

   Monitor the following status bits in registers 30805, 30905

   - DEMUXWAS_xx-They should be 1 indicating word alignment is achieved.
   - CH248_SYNCxx-They should be 1 indicating channel alignment. This is cleared by resync.

5. Write a 1 to the appropriate resync registers 30820, 30920. Note that this assumes that the previous value of the resync bits are 0. The resync operation requires a rising edge. Two writes are required to the resync bits: write a 0 and then write a 1.

   Check out-of-sync and FIFO overflow status in registers 30814 (Bank A).

   - SYNC4_A_OOS, SYNC4_A_OVFL-by 4 alignment.
   - SYNC2_A2_OOS, SYNC_A2_OVFL or SYNC2_A!_OOS, SYNC2_A!_OVFL-by 2 alignment.

   Check out-of-sync status in registers 30914 (Bank B).

   - SYNC4_B_OOS, SYNC4_B_OVFL-by 4 alignment.
   - SYNC_B2_OOS, SYNC2_B2_OVFL or SYNC2_B1_OOS, SYNC_B1_OVFL-by 2 alignment.

   Check out-of-sync status in register 30A03

   - SYNC8_OOS, SYNC8_OVFL-by 8 alignment.

- If out-of-sync bit is 1, then rewrite a 1 to the appropriate resync registers and monitor the OOS bit again. If out-of-sync (OOS) bit is 0 but OVFL bit is 1, then check if the RX_FIFO_MIN value has been programmed to a value > 0. (Default value is 0.) Change the value to 0 and check the OVFL bit again. If OOS and OVFL are 1, then rewrite a 1 to the appropriate resync registers. The resync operation requires a rising edge. Two writes are required to the resync bits: write a 0 and then write a 1.

Backplane Transceiver Core Detailed Description (continued)

Note that any channel within an alignment group can be removed from that alignment group by setting FMPU_STR_EN_XX to 0. The disabling of any channel(s) within an alignment group will not affect the operation of the remaining active channels. If the active channels are synchronized, that synchronization will be maintained and no data loss will occur.

Alignment can also be done between the receive channels on two ORT82G5 devices. Each of the two devices needs to provide its aligned K_CTRL or other alignment character to the other device, which will delay reading from a second alignment FIFO until all channels requesting alignment on the current device AND all channels requesting alignment on the other device are aligned (as indicated on the K_CTRL character). This second alignment FIFO will be implemented in FPGA logic on the ORT82G5. This scheme also requires that the reference clock for both devices be driven by the same signal.

XAUI Lane Alignment Function (Lane Deskew)

In XAUI mode, the receive section in each lane uses the /A/ code group to compensate for lane-to-lane skew. The mechanism restores the timing relationship between the 4 lanes by lining up the /A/ characters into a column. Figure 2 shows the alignment of four lanes based on /A/ character. A minimum spacing of 16 code-groups implies that at least ± 80 bits of skew compensation capability should be provided, which the ORT82G5 significantly exceeds.

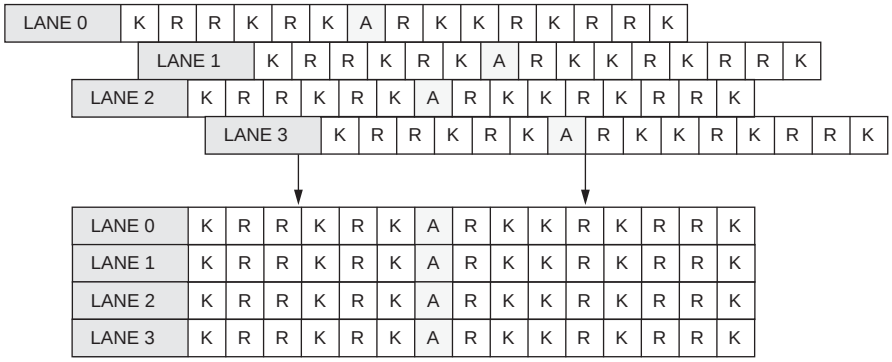

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Figure 15. Deskew Lanes by Aligning /A/ Columns

Mixing Half-rate, Full-rate Modes

When channel alignment is enabled, all receive channels within an alignment group should be configured at the same rate. For example, channels AA, AB, can be configured for twin alignment and full-rate mode, while channels AC, AD that form an alignment group can be configured for half-rate mode. In quad alignment mode, each receive quad can be configured in either half or full-rate mode.

When channel alignment is disabled (this control bit NOCHALGNX is available per quad) within a quad, any receive channel within the quad can be used in half-rate or full-rate mode. The clocking strategy for half-rate mode in both scenarios- (channel alignment enabled and disabled) is described in section Clocking Recommendations of ORT82G5.

Backplane Transceiver Core Detailed Description (continued)

SERDES Characterization

The SERDES characterization mode is a test mode that allows for direct control and observation of the transmit and receive SERDES interfaces at chip ports.

This test mode is configured via the system bus. There are 4 bits that setup the characterization mode. SCHAR_ENA=1 and SCHAR_TXSEL=1 will cause chip ports to directly control the SERDES low-speed transmit ports of one of the channels as shown in Table 12. The x in the table will be a single channel, selected by the SCHAR_CHAN control bits. The decoding of SCHAR_CHAN is shown in Table 13.

Table 12. SERDES Characterization Transmit Mode

Chip Port	SERDES Input
PSCHAR_CKIO0	TBCx
PSCHAR_LDIO[9:0]	LDINx[9:0]

Table 13. Decoding of SCHAR_CHAN

SCHAR_CHAN0	SCHAR_CHAN1	Channel
0	0	BA
1	0	BB
0	1	BC
1	1	BD

When SCHAR_ENA=1 and SCHAR_TXSEL=0, then one of the channels of SERDES outputs is observed at chip ports as shown in Table 14. The channel that is observed is based on the decoding of SCHAR_CHAN as shown in Table 13.

Table 14. SERDES Receive Characterization Mode

SERDES Output	Chip Port
BYTSYNCx	PSCHAR_BYTSYNC
WDSYNCx	PSCHAR_WDSYNC
CVOx	PSCHAR_CV
LDOUTx[9:0]	PSCHAR_LDIO[9:0]
RBC0x	PSCHAR_CKIO0
RBC1x	PSCHAR_CKIO1

With these modes the SERDES can be tested one channel at a time in either its receive or transmit modes. The SERDES characterization mode is available for only one quad (quad B) of the ORT82G5.

Backplane Transceiver Core Detailed Description (continued)

Loopback Modes

The device can be exercised in four possible loopback modes. These loopback modes are identified as:

- High-speed serial loopback
- Parallel loopback at the SERDES boundary
- Parallel loopback at MUX/deMUX boundary excluding SERDES
- Operational mode full loopback using the PRBS generator/checker

These four loopback modes are described next.

High-Speed Serial Loopback

The high-speed serial loopback involves the transmit signal at the serial interface being looped back internally to the receive circuitry. The serial loopback path does not include the high-speed input and output buffers. The HDOUTP, HDOUTN outputs are active in this loopback mode, but the CML input buffers are powered down. The data are sourced at the LDIN[9:0] pins and detected at the LDOUT[9:0] pins. The device is otherwise in its normal mode of operation. The data rate selection bits, TXHR and RXHR, in the channel configuration registers must be configured to carry the same value and the PRBS Generator and Checker are excluded by setting the PRBS configuration bit to 0. The 8b/10b encoder/decoder can optionally be configured into or out of the loopback path. The following Table 15 illustrates the control interface register configuration for the high-speed serial loopback.

Table 15. High-Speed Serial Loopback Configuration

Register Address	Bit Value	Bit Name	Comments
30002, 30012, 30022, 30032, 30102, 30112, 30122, 30132	Bit 0 = 0 or 1	TXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
30002, 30012, 30022, 30032, 30102, 30112, 30122, 30132	Bit 7 = 0 or 1	8B10BT	Set to 0 or 1. If set to 0, the 8b/10b encoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to the same value.
30003, 30013, 30023, 30033, 30103, 30113, 30123, 30133	Bit 0 = 0 or 1	RXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
30003, 30013, 30023, 30033, 30103, 30113, 30123, 30133	Bit 3 = 0 or 1	8B10BR	Set to 0 or 1. If set to 0, the 8b/10b decoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to the same value.
30004, 30014, 30024, 30034, 30104, 30114, 30124, 30134	Bit 0 = 0	PRBS	Set to 0.
30801, 30901	Bit 0 =1 (Channel A) Bit 1 = 1 (Channel B) Bit 2 = 1 (Channel C) Bit 3 = 1 (Channel D)	LOOPENB_x	Set any of the bits 0-3 to 1 to do serial loopback on the corresponding channel.

Backplane Transceiver Core Detailed Description (continued)

Parallel Loopback at the SERDES Boundary

The parallel loopback involves the parallel buses LDIN[9:0] and LDOUT[9:0]. The loopback connection is made such that LDIN[9:0] is logically equivalent to LDOUT[9:0]. In the parallel loopback mode, the LDOUT[9:0] pins remain active. The receive data are sourced at the HDINP, HDINN pins and detected at the HDOUTP, HDOUTN pins. The device is otherwise in its normal mode of operation. The data rate selection bits TXHR and RXHR in the channel configuration registers must be configured to carry the same value and the PRBS generator and checker are excluded by setting the PRBS configuration bit to 0. Also, the 8b/10b encoder and decoder are excluded from the loopback path by setting the 8b10bT and 8b10bR configuration bits to 0. Table 16 illustrates the control interface register configuration for the parallel loopback.

Table 16. Parallel Loopback Configuration

Register Address	Bit Value	Bit Name	Comments
30002, 30012, 30022, 30032, 30102, 30112, 30122, 30132	Bit 0 = 0 or 1	TXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
30002, 30012, 30022, 30032, 30102, 30112, 30122, 30132	Bit 7 = 0	8B10BT	Set to 0. The 8b/10b encoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to 0.
30003, 30013, 30023, 30033, 30103, 30113, 30123, 30133	Bit 0 = 0 or 1	RXHR	Set to 0 or 1. TXHR and RXHR bits must be set to the same value.
30003, 30013, 30023, 30033, 30103, 30113, 30123, 30133	Bit 3 = 0	8B10BR	Set to 0. The 8b/10b decoder is excluded from the loopback path. The 8b/10b encoder and decoder selection control bits must both be set to 0.
30004, 30014, 30024, 30034, 30104, 30114, 30124, 30134	Bit 0 = 0	PRBS	Set to 0.
30004, 30014, 30024, 30034, 30104, 30114, 30124, 30134	Bit 7 = 1	—	Set to 1 if the loopback is done on a per-channel basis. However, if the loopback is done on all the four channels in a quad macro, this bit can be set to 0 but bit 7 of register 5 must be set to 1.
30005, 30105	Bit 7 = 1	—	Set to 1 if the loopback is done globally on all four channels in a quad macro.
30006, 30106	Bits[4:0] =00001	—	Set to 00001.

Parallel Loopback at MUX/DeMUX Boundary Excluding SERDES

This is a low-frequency testmode. This parallel loopback involves the parallel buses SRBDx[9:0] and STBDx[9:0]. The loopback connection is made such that SRBDx[9:0] is logically equivalent to STBDx[9:0] and STBDx[9:0] remains active, thus bypassing the SERDES. Data can be sent from the FPGA through TWDxx signals and monitored on MRWDxx signals. This test is enabled by setting the pin PLOOP_TEST_ENN to 1. PASB_TESTCLK must be running in this mode at 4x frequency of RSYS_CLK[A1,A2,B1,B2] or TSYS_CLK_[AA, AB . . . BD].

Backplane Transceiver Core Detailed Description (continued)

Operational Mode Full Loopback Test Using The PRBS Generator/Checker

The operational mode full loopback test forms one of the normal operational modes of the device. The loopback can be either internal to the device or external to it. To perform the test with internal loopback, the LOOPENB bit should be set to a logic 1. The test includes the PRBS generator in the transmit path and the PRBS checker in the receive path. In this case, the device is placed in its normal operational mode with all the functional blocks in the transmit and the receive path active. The transmit data is generated by an LFSR. The generated word is then serialized and looped back (either internally or externally) to the receiver. The receiver first deserializes the 8-bit word to regenerate the transmitted 8-bit word. The PRBS checker on the receiver compares the regenerated 8-bit word against the transmitted 8-bit word on a word by word basis and signals a mismatch by asserting a PRBSCHK alarm status bit. During this test, the receiver regenerated 8-bit words can also be observed on the device output ports. The PRBS checker contains a watchdog timer which asserts the time-out alarm status bit, PRBSTOUT, if the PRBS test cannot progress beyond its start state within a reasonable time interval. This time interval is set by the precision of the watchdog timer. Both the PRBSCHK and the PRBSTOUT alarms can generate an interrupt if their corresponding masks are disabled.

To enable PRBS test, use the following sequence:

- To preform test with internal loopback, set LOOPENB bit to 1 (registers 30801, 30901).
- Set ENBSYNC register bit(s) to 1, depending on the channel(s) being tested (registers 30800, 30900).
- Lock receiver to data by setting LCKREFN register bits to 1 (registers 30800, 30900).
- Enable PRBS by setting PRBS register bits (30004, 30014, 30024, 30034) (30104, 30114, 30124, 30134). Alternately, the GIPRBS_[A,B] bits can be used to enable PRBS test for all 4 SERDES channels within a bank (registers 30005, 30105).
- Assert GSWRST bit by writing two 1s. Then deassert the bit by writing two 0s.
- Monitor DRBSCHK and PRBSTOUT alarm bits.

Backplane Transceiver Core Detailed Description (continued)

ASB Memory Blocks

This section describes the memory blocks in the embedded core. Note that although the memory blocks are in the embedded core part of the chip, they do not interact with the rest of the embedded core circuits. They are stand-alone blocks designed specifically to increase RAM capacity in the ORT82G5 chip, and will be used by the soft IP cores in the FPGA.

There are two independent memory blocks in the embedded core. These are in addition to the block RAMs found in the FPGA portion of the ORT82G5. A block diagram of a memory block is shown in Figure 16. Each memory block has a capacity of 4K word by 36 bit. It has one read port and one write port and four byte-write-enable (active-low) signals. The read data from the memory block is registered so that it works as a pipelined synchronous memory block. A block diagram of the memory block in shown below in Figure 16.The minimum timing specifications are shown in Figure 18.

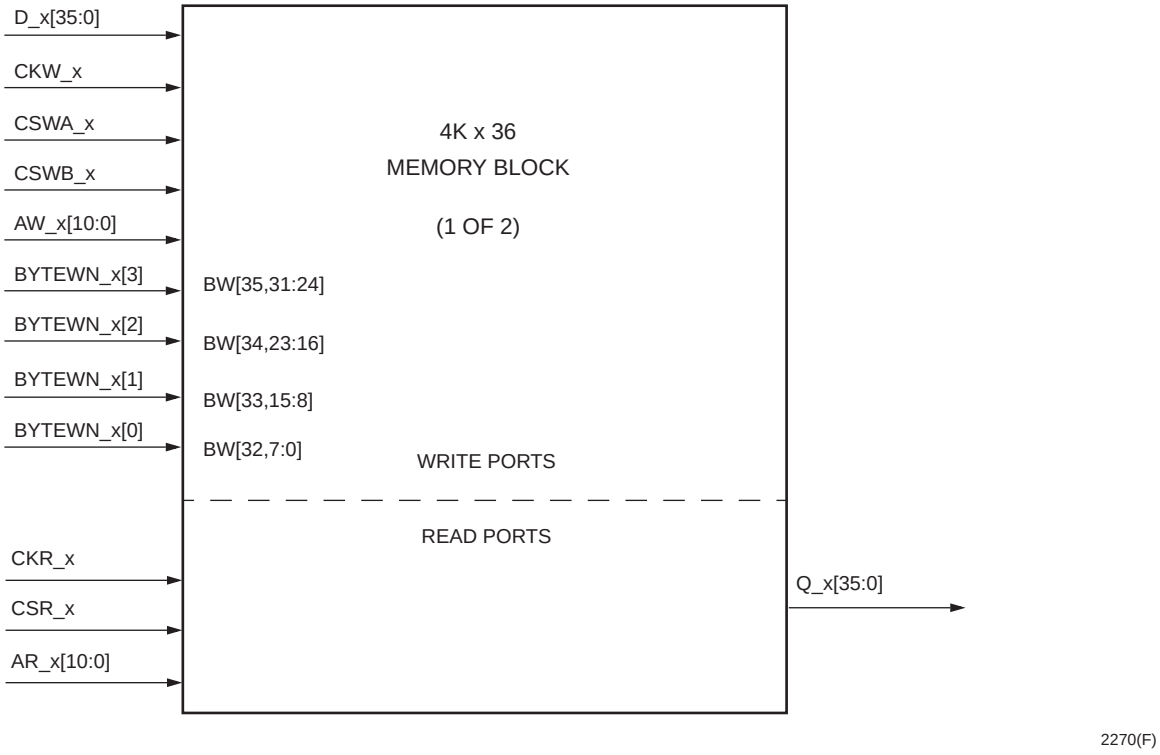


Figure 16. Block Diagram of Memory Block

Backplane Transceiver Core Detailed Description (continued)

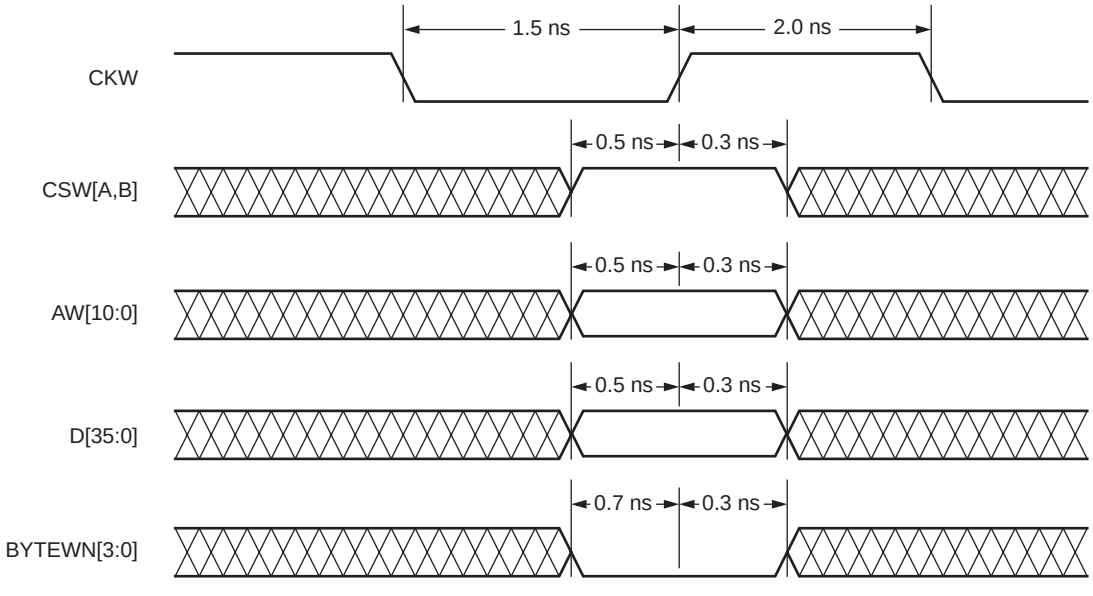


Figure 17. Minimum Timing Specs for Memory Blocks-Write Cycle

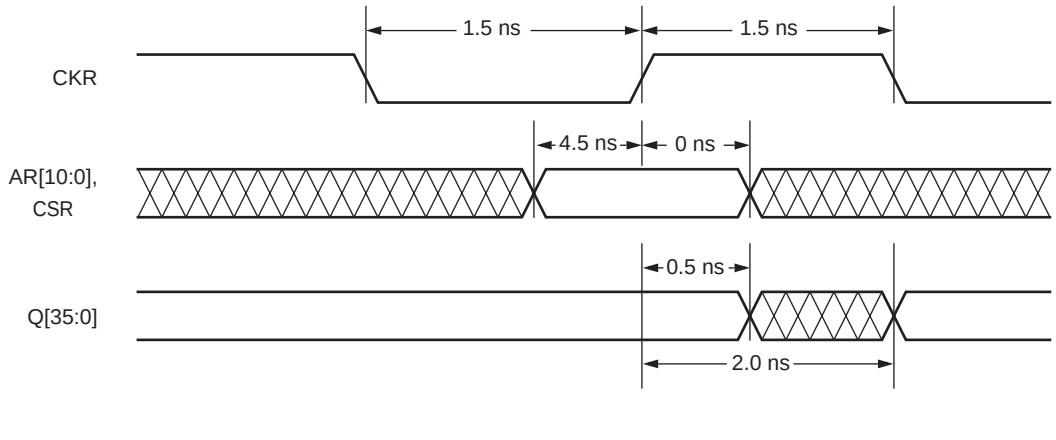


Figure 18. Minimum Timing Specs for Memory Blocks-Read Cycle

Memory Map

Definition of Register Types

The registers in ORT82G5 are 8-bit memory locations, which in general can be classified into the following types: Status Register and Control Register.

Status Register

Read-only register to convey the status information of various operations within the FPSC core. An example is the state of the XAUI link-state-machine.

Control Register

Read-write register to set up the control inputs that define the operation of the FPSC core.

The SERDES block within the ORT82G5 core has a set of status and control registers for it's operation. There is another group of status and control registers which are implemented outside the SERDES, which are related to the SERDES and other functional blocks in the FPSC core. They will be described in detail here. Each SERDES has four independent channels, which are named A, B, C, or D. Using this nomenclature, the SERDES A channels are named as AA, AB, AC, and AD, while SERDES B channels will be BA, BB, BC, and BD.

Table 17. Structural Register Elements

Address (Hex)	Description
300xx	SERDES A, internal registers.
301xx	SERDES B, internal registers.
308xx	Channel A [A:D] registers (external to SERDES blocks).
309xx	Channel B [A:D] registers (external to SERDES blocks).
30A0x	Global registers (external to SERDES blocks).

A full memory map is included in Table 18.

Memory Map (continued)

Table 18 details the memory map for the ASIC core of the ORT82G5 device. This table shows the databus oriented for the PPC interface. DB0 is the MSB, while DB7 is the LSB. If the user master interface is used to preform operations to the ASIC core then the databus must be used in the opposite notation, where DB7 is the MSB and DB0 is the LSB.

Table 18. Memory Map

Addr (Hex)	Reg #	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	Default Value
SERDES A Alarm Registers (Read Only)										
30000	—	Reserved	LKI_AA Receive PLL Lock Indication, Bank A, Channel A. When LKI_AA = 1, then PLL receive is locked.	PRBSCHK_AA PRBS Check Pass/ Fail Indication, Bank A, Channel A. When PRBSCHK_AA = 0, then it is a pass indication.	PRBSTOUT_AA PRBS Checker Watchdog Timer Time-Out Alarm, Bank A, Channel A. When PRBSTOUT_AA = 1, then timeout has occurred.	—	—	—	—	00
30010	—	Reserved	LKI_AB Receive PLL Lock Indication, Bank A, Channel B. When LKI_AB = 1, then PLL receive is locked.	PRBSCHK_AB PRBS Check Pass/ Fail Indication, Bank A, Channel B. When PRBSCHK_AB = 0, then it is a pass indication.	PRBSTOUT_AB PRBS Checker Watchdog Timer Time-Out Alarm, Bank A, Channel B. When PRBSTOUT_AB = 1, then timeout has occurred.	—	—	—	—	00
30020	—	Reserved	LKI_AC Receive PLL Lock Indication, Bank A, Channel C. When LKI_AC = 1, then PLL receive is locked.	PRBSCHK_AC PRBS Check Pass/ Fail Indication, Bank A, Channel C. When PRBSCHK_AC = 0, then it is a pass indication.	PRBSTOUT_AC PRBS Checker Watchdog Timer Time-Out Alarm, Bank A, Channel C. When PRBSTOUT_AC = 1, then timeout has occurred.	—	—	—	—	00
30030	—	Reserved	LKI_AD Receive PLL Lock Indication, Bank A, Channel D. When LKI_AD = 1, then PLL receive is locked.	PRBSCHK_AD PRBS Check Pass/ Fail Indication, Bank A, Channel D. When PRBSCHK_AD = 0, then it is a pass indication.	PRBSTOUT_AD PRBS Checker Watchdog Timer Time-Out Alarm, Bank A, Channel D. When PRBSTOUT_AD = 1, then timeout has occurred.	—	—	—	—	00
SERDES A Alarm Mask Registers										
30001	—	Reserved	MLKI_AA Mask Receive PLL Lock Indication, Bank A, Channel A.	MPRBSCHK_AA. Mask PRBS Check Pass/Fail Indication, Bank A, Channel A.	MPRBSTOUT_AA Mask PRBS Checker Watchdog Timer Time-Out Alarm, Bank A, Channel A.	—	—	—	—	FF
30011	—	Reserved	MLKI_AB Mask Receive PLL Lock Indication, Bank A, Channel B.	MPRBSCHK_AB. Mask PRBS Check Pass/Fail Indication, Bank A, Channel B.	MPRBSTOUT_AB Mask PRBS Checker Watchdog Timer Time-Out Alarm, Bank A, Channel B.	—	—	—	—	FF
30021	—	Reserved	MLKI_AC Mask Receive PLL Lock Indication, Bank A, Channel C.	MPRBSCHK_AC. Mask PRBS Check Pass/Fail Indication, Bank A, Channel C.	MPRBSTOUT_AC Mask PRBS Checker Watchdog Timer Time-Out Alarm, Bank A, Channel C.	—	—	—	—	FF
30031	—	Reserved	MLKI_AD Mask Receive PLL Lock Indication, Bank A, Channel D.	MPRBSCHK_AD. Mask PRBS Check Pass/Fail Indication, Bank A, Channel D.	MPRBSTOUT_AD Mask PRBS Checker Watchdog Timer Time-Out Alarm, Bank A, Channel D.	—	—	—	—	FF

Memory Map (continued)

Table 18. Memory Map (continued)

Addr (Hex)	Reg #	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	Default Value
SERDES A Transmit Channel Configuration Registers										
30002	—	TXHR_AA Transmit Half Rate Selection Bit, Bank A, Channel A. When TXHR = 1, the transmitter samples data on the falling edge of the TBC clock. When TXHR = 0, the transmitter samples data on the falling edge of the double rate clock (derived from TBC). TXHR = 0 on device reset.	PWRDNT_AA Transmit Powerdown Control Bit, Bank A, Channel A. When PWRDNT = 1, sections of the transmit hardware are powered down to conserve power. PWRDNT = 0 on device reset.	PE0_AA Transmit Preemphasis Selection Bit 0, Bank A, Channel A. PE0, together with PE1, selects one of three preemphasis settings for the transmit section. PE0 = 0 on device reset.	PE1_AA Transmit Preemphasis Selection Bit 1, Bank A, Channel A. PE1, together with PE0, selects one of three preemphasis settings for the transmit section. PE1 = 0 on device reset.	HAMP_AA Transmit Half Amplitude Selection Bit, Bank A, Channel A. When HAMP = 1, the transmit output buffer voltage swing is limited to half its amplitude. Otherwise, the transmit output buffer maintains its full voltage swing. HAMP = 0 on device reset.	TBCKSEL_AA Transmit Byte Clock Selection Bit, Bank A, Channel A. When TBCKSEL = 0, the internal XCK is selected. Otherwise, the TBC clock is selected. TBCKSEL = 0 on device reset.	RSVD	8B10BT_AA Transmit 8B/10B Encoder Enable Bit, Bank A, Channel A. When 8B10BT = 1, the 8B/10B encoder on the transmit path is enabled. Otherwise, it is bypassed. 8B10BT = 0 on device reset.	00
30012	—	TXHR_AB Transmit Half Rate Selection Bit, Bank A, Channel B. When TXHR = 1, the transmitter samples data on the falling edge of the TBC clock. When TXHR = 0, the transmitter samples data on the falling edge of the double rate clock (derived from TBC). TXHR = 0 on device reset.	PWRDNT_AB Transmit Powerdown Control Bit, Bank A, Channel B. When PWRDNT = 1, sections of the transmit hardware are powered down to conserve power. PWRDNT = 0 on device reset.	PE0_AB Transmit Preemphasis Selection Bit 0, Bank A, Channel B. PE0, together with PE1, selects one of three preemphasis settings for the transmit section. PE0 = 0 on device reset.	PE1_AB Transmit Preemphasis Selection Bit 1, Bank A, Channel B. PE1, together with PE0, selects one of three preemphasis settings for the transmit section. PE1 = 0 on device reset.	HAMP_AB Transmit Half Amplitude Selection Bit, Bank A, Channel B. When HAMP = 1, the transmit output buffer voltage swing is limited to half its amplitude. Otherwise, the transmit output buffer maintains its full voltage swing. HAMP = 0 on device reset.	TBCKSEL_AB Transmit Byte Clock Selection Bit, Bank A, Channel B. When TBCKSEL = 0, the internal XCK is selected. Otherwise, the TBC clock is selected. TBCKSEL = 0 on device reset.	RSVD	8B10BT_AB Transmit 8B/10B Encoder Enable Bit, Bank A, Channel B. When 8B10BT = 1, the 8B/10B encoder on the transmit path is enabled. Otherwise, it is bypassed. 8B10BT = 0 on device reset.	00
30022	—	TXHR_AC Transmit Half Rate Selection Bit, Bank A, Channel C. When TXHR = 1, the transmitter samples data on the falling edge of the TBC clock. When TXHR = 0, the transmitter samples data on the falling edge of the double rate clock (derived from TBC). TXHR = 0 on device reset.	PWRDNT_AC Transmit Powerdown Control Bit, Bank A, Channel C. When PWRDNT = 1, sections of the transmit hardware are powered down to conserve power. PWRDNT = 0 on device reset.	PE0_AC Transmit Preemphasis Selection Bit 0, Bank A, Channel C. PE0, together with PE1, selects one of three preemphasis settings for the transmit section. PE0 = 0 on device reset.	PE1_AC Transmit Preemphasis Selection Bit 1, Bank A, Channel C. PE1, together with PE0, selects one of three preemphasis settings for the transmit section. PE1 = 0 on device reset.	HAMP_AC Transmit Half Amplitude Selection Bit, Bank A, Channel C. When HAMP = 1, the transmit output buffer voltage swing is limited to half its amplitude. Otherwise, the transmit output buffer maintains its full voltage swing. HAMP = 0 on device reset.	TBCKSEL_AC Transmit Byte Clock Selection Bit, Bank A, Channel C. When TBCKSEL = 0, the internal XCK is selected. Otherwise, the TBC clock is selected. TBCKSEL = 0 on device reset.	RSVD	8B10BT_AC Transmit 8B/10B Encoder Enable Bit, Bank A, Channel C. When 8B10BT = 1, the 8B/10B encoder on the transmit path is enabled. Otherwise, it is bypassed. 8B10BT = 0 on device reset.	00

Memory Map (continued)

Table 18. Memory Map (continued)

Addr (Hex)	Reg #	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	Default Value
SERDES A Transmit Channel Configuration Registers (continued)										
30032	—	TXHR_AD Transmit Half Rate Selection Bit, Bank A, Channel D. When TXHR = 1, the transmitter samples data on the falling edge of the TBC clock. When TXHR = 0, the transmitter samples data on the falling edge of the double rate clock (derived from TBC). TXHR = 0 on device reset.	PWRDNT_AD Transmit Powerdown Control Bit, Bank A, Channel D. When PWRDNT = 1, sections of the transmit hardware are powered down to conserve power. PWRDNT = 0 on device reset.	PE0_AD Transmit Preemphasis Selection Bit 0, Bank A, Channel D. PE0, together with PE1, selects one of three preemphasis settings for the transmit section. PE0 = 0 on device reset.	PE1_AD Transmit Preemphasis Selection Bit 1, Bank A, Channel D. PE1, together with PE0, selects one of three preemphasis settings for the transmit section. PE1 = 0 on device reset.	HAMP_AD Transmit Half Amplitude Selection Bit, Bank A, Channel D. When HAMP = 1, the transmit output buffer voltage swing is limited to half its amplitude. Otherwise, the transmit output buffer maintains its full voltage swing. HAMP = 0 on device reset.	TBCKSEL_AD Transmit Byte Clock Selection Bit, Bank A, Channel D. When TBCKSEL = 0, the internal XCK is selected. Otherwise, the TBC clock is selected. TBCKSEL = 0 on device reset.	RSVD	8B10BT_AD Transmit 8B/10B Encoder Enable Bit, Bank A, Channel D. When 8B10BT = 1, the 8B/10B encoder on the transmit path is enabled. Otherwise, it is bypassed. 8B10BT = 0 on device reset.	00

Memory Map (continued)

Table 18. Memory Map (continued)

Addr (Hex)	Reg #	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	Default Value
SERDES A Receive Channel Configuration Registers										
30003	—	RXHR_AA Receive Half Rate Selection Bit, Bank A, Channel A. When RXHR = 1, the RBC[1:0] clocks are issued at half the scheduled rate of the reference clock. RXHR = 0 on device reset.	PWRDNR_AA Receiver Power Down Control Bit, Bank A, Channel A. When PWRDNR = 1, sections of the receive hardware are powered down to conserve power. PWRDNR = 0 on device reset.	SDOVRIDE_AA Receive Signal Detect Alarm Override Bit, Bank A, Channel A. When SDOVRIDE = 1, the energy detector output from the receiver is masked. Thus, when there is no receive data, the powerdown function is disabled and the corresponding SDON alarm is suppressed. SDOVRIDE = 1 on device reset.	8B10BR_AA Receive 8B/10B Decoder Enable Bit, Bank A, Channel A. When 8B10BR = 1, the 8B/10B decoder on the receive path is enabled. Otherwise, it is bypassed. 8B10BR = on device reset.	LINKSM_AA Link State Machine Enable Bit, Bank A, Channel A. When LINKSM = 1, the receiver link state machine is enabled. Otherwise, the link state machine is disables. LINKSM = 0 on device reset.	—	—	—	20
30013	—	RXHR_AB Receive Half Rate Selection Bit, Bank A, Channel B. When RXHR = 1, the RBC[1:0] clocks are issued at half the scheduled rate of the reference clock. RXHR = 0 on device reset.	PWRDNR_AB Receiver Power Down Control Bit, Bank A, Channel B. When PWRDNR = 1, sections of the receive hardware are powered down to conserve power. PWRDNR = 0 on device reset.	SDOVRIDE_AB Receive Signal Detect Alarm Override Bit, Bank A, Channel B. When SDOVRIDE = 1, the energy detector output from the receiver is masked. Thus, when there is no receive data, the powerdown function is disabled and the corresponding SDON alarm is suppressed. SDOVRIDE = 1 on device reset.	8B10BR_AB Receive 8B/10B Decoder Enable Bit, Bank A, Channel B. When 8B10BR = 1, the 8B/10B decoder on the receive path is enabled. Otherwise, it is bypassed. 8B10BR = on device reset.	LINKSM_AB Link State Machine Enable Bit, Bank A, Channel B. When LINKSM = 1, the receiver link state machine is enabled. Otherwise, the link state machine is disables. LINKSM = 0 on device reset.	—	—	—	20
30023	—	RXHR_AC Receive Half Rate Selection Bit, Bank A, Channel C. When RXHR = 1, the RBC[1:0] clocks are issued at half the scheduled rate of the reference clock. RXHR = 0 on device reset.	PWRDNR_AC Receiver Power Down Control Bit, Bank A, Channel C. When PWRDNR = 1, sections of the receive hardware are powered down to conserve power. PWRDNR = 0 on device reset.	SDOVRIDE_AC Receive Signal Detect Alarm Override Bit, Bank A, Channel C. When SDOVRIDE = 1, the energy detector output from the receiver is masked. Thus, when there is no receive data, the powerdown function is disabled and the corresponding SDON alarm is suppressed. SDOVRIDE = 1 on device reset.	8B10BR_AC Receive 8B/10B Decoder Enable Bit, Bank A, Channel C. When 8B10BR = 1, the 8B/10B decoder on the receive path is enabled. Otherwise, it is bypassed. 8B10BR = on device reset.	LINKSM_AC Link State Machine Enable Bit, Bank A, Channel C. When LINKSM = 1, the receiver link state machine is enabled. Otherwise, the link state machine is disables. LINKSM = 0 on device reset.	—	—	—	20
30033	—	RXHR_AD Receive Half Rate Selection Bit, Bank A, Channel D. When RXHR = 1, the RBC[1:0] clocks are issued at half the scheduled rate of the reference clock. RXHR = 0 on device reset.	PWRDNR_AD Receiver Power Down Control Bit, Bank A, Channel D. When PWRDNR = 1, sections of the receive hardware are powered down to conserve power. PWRDNR = 0 on device reset.	SDOVRIDE_AD Receive Signal Detect Alarm Override Bit, Bank A, Channel D. When SDOVRIDE = 1, the energy detector output from the receiver is masked. Thus, when there is no receive data, the powerdown function is disabled and the corresponding SDON alarm is suppressed. SDOVRIDE = 1 on device reset.	8B10BR_AD Receive 8B/10B Decoder Enable Bit, Bank A, Channel D. When 8B10BR = 1, the 8B/10B decoder on the receive path is enabled. Otherwise, it is bypassed. 8B10BR = on device reset.	LINKSM_AD Link State Machine Enable Bit, Bank A, Channel D. When LINKSM = 1, the receiver link state machine is enabled. Otherwise, the link state machine is disables. LINKSM = 0 on device reset.	—	—	—	20

Memory Map (continued)

Table 18. Memory Map (continued)

Addr (Hex)	Reg #	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	Default Value
SERDES A Common Transmit and Receive Channel Configuration Registers										
30004	—	PRBS_AA Transmit and Receive PRBS Enable Bit, Bank A, Channel A. When PRBS = 1, the PRBS generator on the transmitter and the PRBS checker on the receiver are enabled. PRBS = 0 on device reset.	MASK_AA Transmit and Receive Alarm Mask Bit, Bank A, Channel A. When MASK = 1, the transmit and receive alarms of a channel are prevented from generating an interrupt. This MASK bit overrides the individual alarm mask bits in the Alarm Mask Registers. MASK = 1 on device reset.	SWRST_AA Transmit and Receive Software Reset Bit, Bank A, Channel A. When SWRST = 1, this bit provides the same function as the hardware reset, except all configuration register settings are preserved. This is not a self-clearing bit. Once set, this bit must be cleared by writing a 0 to it. SWRST = 0 on device reset.	—	—	—	—	TESTEN_AA Transmit and Receive Test Enable Bit, Bank A, Channel A. When TESTEN = 1, the transmit and receive sections are placed in test mode. TESTEN = 0 on device reset. When the global test enable bit GTESTEN = 0, the individual channel test enable bits are used to selectively place a channel in test or normal mode. When GTESTEN = 1, all channels are set to test mode regardless of their TESTEN setting.	40
30014	—	PRBS_AB Transmit and Receive PRBS Enable Bit, Bank A, Channel B. When PRBS = 1, the PRBS generator on the transmitter and the PRBS checker on the receiver are enabled. PRBS = 0 on device reset.	MASK_AB Transmit and Receive Alarm Mask Bit, Bank A, Channel B. When MASK = 1, the transmit and receive alarms of a channel are prevented from generating an interrupt. This MASK bit overrides the individual alarm mask bits in the Alarm Mask Registers. MASK = 1 on device reset.	SWRST_AB Transmit and Receive Software Reset Bit, Bank A, Channel B. When SWRST = 1, this bit provides the same function as the hardware reset, except all configuration register settings are preserved. This is not a self-clearing bit. Once set, this bit must be cleared by writing a 0 to it. SWRST = 0 on device reset.	—	—	—	—	TESTEN_AB Transmit and Receive Test Enable Bit, Bank A, Channel B. When TESTEN = 1, the transmit and receive sections are placed in test mode. TESTEN = 0 on device reset. When the global test enable bit GTESTEN = 0, the individual channel test enable bits are used to selectively place a channel in test or normal mode. When GTESTEN = 1, all channels are set to test mode regardless of their TESTEN setting.	40
30024	—	PRBS_AC Transmit and Receive PRBS Enable Bit, Bank A, Channel C. When PRBS = 1, the PRBS generator on the transmitter and the PRBS checker on the receiver are enabled. PRBS = 0 on device reset.	MASK_AC Transmit and Receive Alarm Mask Bit, Bank A, Channel C. When MASK = 1, the transmit and receive alarms of a channel are prevented from generating an interrupt. This MASK bit overrides the individual alarm mask bits in the Alarm Mask Registers. MASK = 1 on device reset.	SWRST_AC Transmit and Receive Software Reset Bit, Bank A, Channel C. When SWRST = 1, this bit provides the same function as the hardware reset, except all configuration register settings are preserved. This is not a self-clearing bit. Once set, this bit must be cleared by writing a 0 to it. SWRST = 0 on device reset.	—	—	—	—	TESTEN_AC Transmit and Receive Test Enable Bit, Bank A, Channel C. When TESTEN = 1, the transmit and receive sections are placed in test mode. TESTEN = 0 on device reset. When the global test enable bit GTESTEN = 0, the individual channel test enable bits are used to selectively place a channel in test or normal mode. When GTESTEN = 1, all channels are set to test mode regardless of their TESTEN setting.	40
30034	—	PRBS_AD Transmit and Receive PRBS Enable Bit, Bank A, Channel D. When PRBS = 1, the PRBS generator on the transmitter and the PRBS checker on the receiver are enabled. PRBS = 0 on device reset.	MASK_AD Transmit and Receive Alarm Mask Bit, Bank A, Channel D. When MASK = 1, the transmit and receive alarms of a channel are prevented from generating an interrupt. This MASK bit overrides the individual alarm mask bits in the Alarm Mask Registers. MASK = 1 on device reset.	SWRST_AD Transmit and Receive Software Reset Bit, Bank A, Channel D. When SWRST = 1, this bit provides the same function as the hardware reset, except all configuration register settings are preserved. This is not a self-clearing bit. Once set, this bit must be cleared by writing a 0 to it. SWRST = 0 on device reset.	—	—	—	—	TESTEN_AD Transmit and Receive Test Enable Bit, Bank A, Channel D. When TESTEN = 1, the transmit and receive sections are placed in test mode. TESTEN = 0 on device reset. When the global test enable bit GTESTEN = 0, the individual channel test enable bits are used to selectively place a channel in test or normal mode. When GTESTEN = 1, all channels are set to test mode regardless of their TESTEN setting.	40

Memory Map (continued)

Table 18. Memory Map (continued)

Addr (Hex)	Reg #	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	Default Value
SERDES A Global Control Register (Acts on Channels A, B, C, and D)										
30005	—	GPRBS_A Global Enable. The GPRBS bit globally enables the PRBS generators and checkers all four channels of SERDES A when GPRBS = 1. GPRBS = 0 on device reset.	GMASK_A Global Mask. The GMASK globally masks all the channel alarms of SERDES A when GMASK = 1. This prevents all the transmit and receive alarms from generating an interrupt. GMASK = 1 on device reset.	GSWRST_A RESET Function. The GSWRST bit provides the same function as the hardware reset for the transmit and receive sections of all four channels of ASERDES A, except that the device configuration settings are not affected when GSWRST is asserted. GSWRST = 0 on device reset. This is not a self-clearing bit. Once set, it must be cleared by writing a 0 to it.	GPWRDNT_A Powerdown Transmit Function. When GPWRDNT = 1, sections of the transmit hardware for all four channels of SERDES A are powered down to conserve power. GPWRDNT = 0 on device reset.	GPWRDNR_A Powerdown Receive Function. When GPWRDNR = 1, sections of the receive hardware for all four channels of SERDES A are powered down to conserve power. GPWRDNR = 0 on device reset.	GTRISTN_A Active-Low TRISTN Function. When GTRISTN = 0, the CMOS output buffers for SERDES A are 3-stated. GTRISTN = 1 on device reset.	—	GTESTEN_A Test Enable Control. When GTESTEN = 1, the transmit and receive sections of all four channels of SERDES A are placed in test mode. GTESTEN = 0 on device reset.	44
30006	—	TestMode	TestMode	TestMode	TestMode	TestMode	—	RSVD	RSVD	00

Memory Map (continued)

Table 18. Memory Map (continued)

Addr (Hex)	Reg #	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	Default Value
Control Registers A										
30800	A0	ENBYSYNC_AA 1 = Byte Alignments bank A, channelA	ENBYSYNC_AB 1 = Byte Alignments bank A, channel B	ENBYSYNC_AC 1 = Byte Alignments bank A, channel C	ENBYSYNC_AD 1 = Byte Alignments bank A, channel D	LCKREFN_AA 0 = Lock receiver to ref. clock 1 = Lock receiver to data for bank A channel A	LCKREFN_AB 0 =Lock receiver to ref. clock 1 =Lock receiver to data for bank A channel B	LCKREFN_AC 0 = Lock receiver to ref. clock 1 = Lock receiver to data for bank A channel C	LCKREFN_AD 0 = Lock receiver to ref. clock 1 = Lock receiver to data for bank A channel D	00
30801	A1	LOOPENB_AA Enable loopback mode for bank A, channel A	LOOPENB_AB Enable loopback mode for bank A, channel B	LOOPENB_AC Enable loopback mode for bank A, channel C	LOOPENB_AD Enable loopback mode for bank A, channel D	NOWDALIGN_AA Defeats deMUX alignment for bank A, channel A	NOWDALIGN_AB Defeats deMUX alignment for bank A, channel B	NOWDALIGN_AC Defeats deMUX alignment for bank A, channel C	NOWDALIGN_AD Defeats deMUX alignment for bank A, channel	00
30802	A2	Reserved for future use								
30803	A3	Reserved for future use								
30810	A4	DOWDALIGN_AA Force new deMUX word alignment for bank A, channel A	DOWDALIGN_AB Force new deMUX word alignment for bank A, channel B	DOWDALIGN_AC Force new deMUX word alignment for bank A, channel C	DOWDALIGN_AD Force new deMUX word alignment for bank A, channel D	FMPU_STR_EN_AA Enable alignment function for channel AA	FMPU_STR_EN_AB Enable alignment function for channel AB	FMPU_STR_EN_AC Enable alignment function for channel AC	FMPU_STR_EN_AD Enable alignment function for channel AD	00
30811	A5*	FMPU_SYNMODE_AA[0:1] Sync mode for AA		FMPU_SYNMODE_AB[0:1] Sync mode for AB		FMPU_SYNMODE_AC[0:1] Sync mode for AC		FMPU_SYNMODE_AD[0:1] Sync mode for AD		00
30812	A6	Reserved for future use								
30813	A7	Reserved for future use								
30820	A8	FMPU_RESYNC1_AA Resync a single channel, AA. Write a 0, then write a 1.	FMPU_RESYNC1_AB Resync a single channel, AB. Write a 0, then write a 1.	FMPU_RESYNC1_AC Resync a single channel, AC. Write a 0, then write a 1.	FMPU_RESYNC1_AD Resync a single channel, AD. Write a 0, then write a 1.	FMPU_RESYNC2_A1 Resync 2 channels, AA and AB. Write a 0, then write a 1.	FMPU_RESYNC2A2 Resync 2 channels, AC and AD. Write a 0, then write a 1.	FMPU_RESYNC4A Resync 4 channels A[A:D]. Write a 0, then write a 1.	XAUI_MODEA Controls use of XAUI link state machine vs. SERDES link State machine for bank A	00
30821	A9	NOCHALGNA Bypass channel alignment deMUXed data directly to FPGA for bank A	Reserved for future use							00
30822	A10	Reserved for future use								
30823	A11	Reserved for future use								
30830	A12	Reserved for future use								
30831	A13	Reserved for future use								
30832	A14	Reserved for future use								
30833	A15	Reserved for future use								

* FMPU_SYNMODE_xx[0:1]
  00 = No channel alignment
  10 = Twin channel alignment
  01 = Quad channel alignment
  11 = 8 channel alignment

Memory Map (continued)

Table 18. Memory Map (continued)

Addr (Hex)	Reg #	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	Default Value
Status Registers A										
30804	A16	XAUISTAT_AA[0:1]† Status of XAUI link state machine for bank A, channel A		XAUISTAT_AB[0:1]* Status of XAUI link state machine for bank A, channel B		XAUISTAT_AC[0:1]* Status of XAUI link state machine for bank A, channel C		XAUISTAT_AD[0:1]* Status of XAUI link state machine for bank A, channel D		00
30805	A17	DEMUXWAS_AA Status of deMUX word alignment for bank A, channel A	DEMUXWAS_AB Status of deMUX word alignment for bank A, channel B	DEMUXWAS_AC Status of deMUX word alignment for bank A, channel C	DEMUXWAS_AD Status of deMUX word alignment for bank A, channel D	CH248_SYNC_AA Alignment completed for AA	CH248_SYNC_AB Alignment completed for AB	CH248_SYNC_AC Alignment completed for AC	CH248_SYNC_AD Alignment completed for AD	00
30806	A18	Reserved for future use								
30807	A19	Reserved for future use								
30814	A20	SYNC2_A1 OVFL Alignment FIFO overflow AA and AB	SYNC2_A2 OVFL Alignment FIFO overflow AC and AD	SYNC4_A OVFL Alignment FIFO overflow for A[A:D]	SYNC2_A1 OOS Alignment out of sync for AA and AB	SYNC2_A2 OOS Alignment out of sync for AC and AD	SYNC4_A_OOS Alignment out of sync for A[A:D]	Reserved for future use		
30815	A21	Reserved for future use								
30816	A22	Reserved for future use								
30817	A23	Reserved for future use								
30824	A24	Reserved for future use								
30825	A25	Reserved for future use								
30826	A26	Reserved for future use								
30827	A27	Reserved for future use								
30834	A28	Reserved for future use								
30835	A29	Reserved for future use								
30836	A30	Reserved for future use								
30837	A31	Reserved for future use								

† For XAUISTAT_Ay[0:1] (address 0x30804), the definitions of these bits are:
00—No synchronization.
10—Synchronization done.
01,11—Not used.

Memory Map (continued)

Table 18. Memory Map (continued)

Addr (Hex)	Reg #	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	Default Value
SERDES B Alarm Registers (Read Only)										
30100	—	Reserved	LKI_BA Receive PLL Lock Indication, Bank B, Channel A. When LKI_BA = 1, then PLL receive is locked.	PRBSCHK_BA PRBS Check Pass/Fail Indication, Bank B, Channel A. When PRBSCHK_BA = 0, then it is a pass indication.	PRBSTOUT_BA PRBS Checker Watchdog Timer Time-Out Alarm, Bank B, Channel A. When PRBSTOUT_BA = 1, then timeout has occurred.	—	—	—	—	00
30110	—	Reserved	LKI_BB Receive PLL Lock Indication, Bank B, Channel B. When LKI_BB = 1, then PLL receive is locked.	PRBSCHK_BB PRBS Check Pass/Fail Indication, Bank B, Channel B. When PRBSCHK_BB = 0, then it is a pass indication.	PRBSTOUT_BB PRBS Checker Watchdog Timer Time-Out Alarm, Bank B, Channel B. When PRBSTOUT_BB = 1, then timeout has occurred.	—	—	—	—	00
30120	—	Reserved	LKI_BC Receive PLL Lock Indication, Bank B, Channel C. When LKI_BC = 1, then PLL receive is locked.	PRBSCHK_BC PRBS Check Pass/Fail Indication, Bank B, Channel C. When PRBSCHK_BC = 0, then it is a pass indication.	PRBSTOUT_BC PRBS Checker Watchdog Timer Time-Out Alarm, Bank B, Channel C. When PRBSTOUT_BC = 1, then timeout has occurred.	—	—	—	—	00
30130	—	Reserved	LKI_BD Receive PLL Lock Indication, Bank B, Channel D. When LKI_BD = 1, then PLL receive is locked.	PRBSCHK_BD PRBS Check Pass/Fail Indication, Bank B, Channel D. When PRBSCHK_BD = 0, then it is a pass indication.	PRBSTOUT_BD PRBS Checker Watchdog Timer Time-Out Alarm, Bank B, Channel D. When PRBSTOUT_BD = 1, then timeout has occurred.	—	—	—	—	00
SERDES B Alarm Mask Registers										
30101	—	Reserved	MLKI_BA Mask Receive PLL Lock Indication, Bank B, Channel A.	MPRBSCHK_BA. Mask PRBS Check Pass/Fail Indication, Bank B, Channel A.	MPRBSTOUT_BA Mask PRBS Checker Watchdog Timer Time-Out Alarm, Bank B, Channel A.	—	—	—	—	FF
30111	—	Reserved	MLKI_BB Mask Receive PLL Lock Indication, Bank B, Channel B.	MPRBSCHK_BB. Mask PRBS Check Pass/Fail Indication, Bank B, Channel B.	MPRBSTOUT_BB Mask PRBS Checker Watchdog Timer Time-Out Alarm, Bank B, Channel B.	—	—	—	—	FF
30121	—	Reserved	MLKI_BC Mask Receive PLL Lock Indication, Bank B, Channel C.	MPRBSCHK_BC. Mask PRBS Check Pass/Fail Indication, Bank B, Channel C.	MPRBSTOUT_BC Mask PRBS Checker Watchdog Timer Time-Out Alarm, Bank B, Channel C.	—	—	—	—	FF
30131	—	Reserved	MLKI_BD Mask Receive PLL Lock Indication, Bank B, Channel D.	MPRBSCHK_BD. Mask PRBS Check Pass/Fail Indication, Bank B, Channel D.	MPRBSTOUT_BD Mask PRBS Checker Watchdog Timer Time-Out Alarm, Bank B, Channel D.	—	—	—	—	FF

Memory Map (continued)

Table 18. Memory Map (continued)

Addr (Hex)	Reg #	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	Default Value
SERDES B Transmit Channel Configuration Registers										
30102	—	TXHR_BA Transmit Half Rate Selection Bit, Bank B, Channel A. When TXHR = 1, the transmitter samples data on the falling edge of the TBC clock. When TXHR = 0, the transmitter samples data on the falling edge of the double rate clock (derived from TBC). TXHR = 0 on device reset.	PWRDNT_BA Transmit Power-down Control Bit, Bank B, Channel A. When PWRDNT = 1, sections of the transmit hardware are powered down to conserve power. PWRDNT = 0 on device reset.	PE0_BA Transmit Pre-emphasis Selection Bit 0, Bank B, Channel A. PE0, together with PE1, selects one of three preemphasis settings for the transmit section. PE0 = 0 on device reset.	PE1_BA Transmit Pre-emphasis Selection Bit 1, Bank B, Channel A. PE1, together with PE0, selects one of three preemphasis settings for the transmit section. PE1 = 0 on device reset.	HAMP_BA Transmit Half Amplitude Selection Bit, Bank B, Channel A. When HAMP = 1, the transmit output buffer voltage swing is limited to half its amplitude. Otherwise, the transmit output buffer maintains its full voltage swing. HAMP = 0 on device reset.	TBCKSEL_BA Transmit Byte Clock Selection Bit, Bank B, Channel A. When TBCKSEL = 0, the internal XCK is selected. Otherwise, the TBC clock is selected. TBCKSEL = 0 on device reset.	RSVD	8B10BT_BA Transmit 8B/10B Encoder Enable Bit, Bank B, Channel A. When 8B10BT = 1, the 8B/10B encoder on the transmit path is enabled. Otherwise, it is bypassed. 8B10BT = 0 on device reset.	00
30112	—	TXHR_BB Transmit Half Rate Selection Bit, Bank B, Channel B. When TXHR = 1, the transmitter samples data on the falling edge of the TBC clock. When TXHR = 0, the transmitter samples data on the falling edge of the double rate clock (derived from TBC). TXHR = 0 on device reset.	PWRDNT_BB Transmit Power-down Control Bit, Bank B, Channel B. When PWRDNT = 1, sections of the transmit hardware are powered down to conserve power. PWRDNT = 0 on device reset.	PE0_BB Transmit Pre-emphasis Selection Bit 0, Bank B, Channel B. PE0, together with PE1, selects one of three preemphasis settings for the transmit section. PE0 = 0 on device reset.	PE1_BB Transmit Pre-emphasis Selection Bit 1, Bank B, Channel B. PE1, together with PE0, selects one of three preemphasis settings for the transmit section. PE1 = 0 on device reset.	HAMP_BB Transmit Half Amplitude Selection Bit, Bank B, Channel B. When HAMP = 1, the transmit output buffer voltage swing is limited to half its amplitude. Otherwise, the transmit output buffer maintains its full voltage swing. HAMP = 0 on device reset.	TBCKSEL_BB Transmit Byte Clock Selection Bit, Bank B, Channel B. When TBCKSEL = 0, the internal XCK is selected. Otherwise, the TBC clock is selected. TBCKSEL = 0 on device reset.	RSVD	8B10BT_BB Transmit 8B/10B Encoder Enable Bit, Bank B, Channel B. When 8B10BT = 1, the 8B/10B encoder on the transmit path is enabled. Otherwise, it is bypassed. 8B10BT = 0 on device reset.	00
30122	—	TXHR_BC Transmit Half Rate Selection Bit, Bank B, Channel C. When TXHR = 1, the transmitter samples data on the falling edge of the TBC clock. When TXHR = 0, the transmitter samples data on the falling edge of the double rate clock (derived from TBC). TXHR = 0 on device reset.	PWRDNT_BC Transmit Power-down Control Bit, Bank B, Channel C. When PWRDNT = 1, sections of the transmit hardware are powered down to conserve power. PWRDNT = 0 on device reset.	PE0_BC Transmit Pre-emphasis Selection Bit 0, Bank B, Channel C. PE0, together with PE1, selects one of three preemphasis settings for the transmit section. PE0 = 0 on device reset.	PE1_BC Transmit Pre-emphasis Selection Bit 1, Bank B, Channel C. PE1, together with PE0, selects one of three preemphasis settings for the transmit section. PE1 = 0 on device reset.	HAMP_BC Transmit Half Amplitude Selection Bit, Bank B, Channel C. When HAMP = 1, the transmit output buffer voltage swing is limited to half its amplitude. Otherwise, the transmit output buffer maintains its full voltage swing. HAMP = 0 on device reset.	TBCKSEL_BC Transmit Byte Clock Selection Bit, Bank B, Channel C. When TBCKSEL = 0, the internal XCK is selected. Otherwise, the TBC clock is selected. TBCKSEL = 0 on device reset.	RSVD	8B10BT_BC Transmit 8B/10B Encoder Enable Bit, Bank B, Channel C. When 8B10BT = 1, the 8B/10B encoder on the transmit path is enabled. Otherwise, it is bypassed. 8B10BT = 0 on device reset.	00
30132	—	TXHR_BD Transmit Half Rate Selection Bit, Bank B, Channel D. When TXHR = 1, the transmitter samples data on the falling edge of the TBC clock. When TXHR = 0, the transmitter samples data on the falling edge of the double rate clock (derived from TBC). TXHR = 0 on device reset.	PWRDNT_BD Transmit Power-down Control Bit, Bank B, Channel D. When PWRDNT = 1, sections of the transmit hardware are powered down to conserve power. PWRDNT = 0 on device reset.	PE0_BD Transmit Pre-emphasis Selection Bit 0, Bank B, Channel D. PE0, together with PE1, selects one of three preemphasis settings for the transmit section. PE0 = 0 on device reset.	PE1_BD Transmit Pre-emphasis Selection Bit 1, Bank B, Channel D. PE1, together with PE0, selects one of three preemphasis settings for the transmit section. PE1 = 0 on device reset.	HAMP_BD Transmit Half Amplitude Selection Bit, Bank B, Channel D. When HAMP = 1, the transmit output buffer voltage swing is limited to half its amplitude. Otherwise, the transmit output buffer maintains its full voltage swing. HAMP = 0 on device reset.	TBCKSEL_BD Transmit Byte Clock Selection Bit, Bank B, Channel D. When TBCKSEL = 0, the internal XCK is selected. Otherwise, the TBC clock is selected. TBCKSEL = 0 on device reset.	RSVD	8B10BT_BD Transmit 8B/10B Encoder Enable Bit, Bank B, Channel D. When 8B10BT = 1, the 8B/10B encoder on the transmit path is enabled. Otherwise, it is bypassed. 8B10BT = 0 on device reset.	00

Memory Map (continued)

Table 18. Memory Map (continued)

Addr (Hex)	Reg #	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	Default Value
SERDES B Receive Channel Configuration Registers										
30103	—	RXHR_BA Receive Half Rate Selection Bit, Bank B, Channel A. When RXHR = 1, the RBC[1:0] clocks are issued at half the scheduled rate of the reference clock. RXHR = 0 on device reset.	PWRDNR_BA Receiver Power Down Control Bit, Bank B, Channel A. When PWRDNR = 1, sections of the receive hardware are powered down to conserve power. PWRDNR = 0 on device reset.	SDOVRIDE_BA Receive Signal Detect Alarm Override Bit, Bank B, Channel A. When SDOVRIDE = 1, the energy detector output from the receiver is masked. Thus, when there is no receive data, the powerdown function is disabled and the corresponding SDON alarm is suppressed. SDOVRIDE = 1 on device reset.	8B10BR_BA Receive 8B/10B Decoder Enable Bit, Bank B, Channel A. When 8B10BR = 1, the 8B/10B decoder on the receive path is enabled. Otherwise, it is bypassed. 8B10BR = on device reset.	LINKSM_BA Link State Machine Enable Bit, Bank B, Channel A. When LINKSM = 1, the receiver link state machine is enabled. Otherwise, the link state machine is disables. LINKSM = 0 on device reset.	—	—	—	20
30113	—	RXHR_BB Receive Half Rate Selection Bit, Bank B, Channel B. When RXHR = 1, the RBC[1:0] clocks are issued at half the scheduled rate of the reference clock. RXHR = 0 on device reset.	PWRDNR_BB Receiver Power Down Control Bit, Bank B, Channel B. When PWRDNR = 1, sections of the receive hardware are powered down to conserve power. PWRDNR = 0 on device reset.	SDOVRIDE_BB Receive Signal Detect Alarm Override Bit, Bank B, Channel B. When SDOVRIDE = 1, the energy detector output from the receiver is masked. Thus, when there is no receive data, the powerdown function is disabled and the corresponding SDON alarm is suppressed. SDOVRIDE = 1 on device reset.	8B10BR_BB Receive 8B/10B Decoder Enable Bit, Bank B, Channel B. When 8B10BR = 1, the 8B/10B decoder on the receive path is enabled. Otherwise, it is bypassed. 8B10BR = on device reset.	LINKSM_BB Link State Machine Enable Bit, Bank B, Channel B. When LINKSM = 1, the receiver link state machine is enabled. Otherwise, the link state machine is disables. LINKSM = 0 on device reset.	—	—	—	20
30123	—	RXHR_BC Receive Half Rate Selection Bit, Bank B, Channel C. When RXHR = 1, the RBC[1:0] clocks are issued at half the scheduled rate of the reference clock. RXHR = 0 on device reset.	PWRDNR_BC Receiver Power Down Control Bit, Bank B, Channel C. When PWRDNR = 1, sections of the receive hardware are powered down to conserve power. PWRDNR = 0 on device reset.	SDOVRIDE_BC Receive Signal Detect Alarm Override Bit, Bank B, Channel C. When SDOVRIDE = 1, the energy detector output from the receiver is masked. Thus, when there is no receive data, the powerdown function is disabled and the corresponding SDON alarm is suppressed. SDOVRIDE = 1 on device reset.	8B10BR_BC Receive 8B/10B Decoder Enable Bit, Bank B, Channel C. When 8B10BR = 1, the 8B/10B decoder on the receive path is enabled. Otherwise, it is bypassed. 8B10BR = on device reset.	LINKSM_BC Link State Machine Enable Bit, Bank B, Channel C. When LINKSM = 1, the receiver link state machine is enabled. Otherwise, the link state machine is disables. LINKSM = 0 on device reset.	—	—	—	20
30133	—	RXHR_BD Receive Half Rate Selection Bit, Bank B, Channel D. When RXHR = 1, the RBC[1:0] clocks are issued at half the scheduled rate of the reference clock. RXHR = 0 on device reset.	PWRDNR_BD Receiver Power Down Control Bit, Bank B, Channel D. When PWRDNR = 1, sections of the receive hardware are powered down to conserve power. PWRDNR = 0 on device reset.	SDOVRIDE_BD Receive Signal Detect Alarm Override Bit, Bank B, Channel D. When SDOVRIDE = 1, the energy detector output from the receiver is masked. Thus, when there is no receive data, the powerdown function is disabled and the corresponding SDON alarm is suppressed. SDOVRIDE = 1 on device reset.	8B10BR_BD Receive 8B/10B Decoder Enable Bit, Bank B, Channel D. When 8B10BR = 1, the 8B/10B decoder on the receive path is enabled. Otherwise, it is bypassed. 8B10BR = on device reset.	LINKSM_BD Link State Machine Enable Bit, Bank B, Channel D. When LINKSM = 1, the receiver link state machine is enabled. Otherwise, the link state machine is disables. LINKSM = 0 on device reset.	—	—	—	20

Memory Map (continued)

Table 18. Memory Map (continued)

Addr (Hex)	Reg #	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	Default Value
SERDES B Common Transmit and Receive Channel Configuration Registers										
30104	—	PRBS_BA Transmit and Receive PRBS Enable Bit, Bank B, Channel A. When PRBS = 1, the PRBS generator on the transmitter and the PRBS checker on the receiver are enabled. PRBS = 0 on device reset.	MASK_BA Transmit and Receive Alarm Mask Bit, Bank B, Channel A. When MASK = 1, the transmit and receive alarms of a channel are prevented from generating an interrupt. This MASK bit overrides the individual alarm mask bits in the Alarm Mask Registers. MASK = 1 on device reset.	SWRST_BA Transmit and Receive Software Reset Bit, Bank B, Channel A. When SWRST = 1, this bit provides the same function as the hardware reset, except all configuration register settings are preserved. This is not a self-clearing bit. Once set, this bit must be cleared by writing a 0 to it. SWRST = 0 on device reset.	—	—	—	—	TESTEN_BA Transmit and Receive Test Enable Bit, Bank B, Channel A. When TESTEN = 1, the transmit and receive sections are placed in test mode. TESTEN = 0 on device reset. When the global test enable bit GTESTEN = 0, the individual channel test enable bits are used to selectively place a channel in test or normal mode. When GTESTEN = 1, all channels are set to test mode regardless of their TESTEN setting.	40
30114	—	PRBS_BB Transmit and Receive PRBS Enable Bit, Bank B, Channel B. When PRBS = 1, the PRBS generator on the transmitter and the PRBS checker on the receiver are enabled. PRBS = 0 on device reset.	MASK_BB Transmit and Receive Alarm Mask Bit, Bank B, Channel B. When MASK = 1, the transmit and receive alarms of a channel are prevented from generating an interrupt. This MASK bit overrides the individual alarm mask bits in the Alarm Mask Registers. MASK = 1 on device reset.	SWRST_BB Transmit and Receive Software Reset Bit, Bank B, Channel B. When SWRST = 1, this bit provides the same function as the hardware reset, except all configuration register settings are preserved. This is not a self-clearing bit. Once set, this bit must be cleared by writing a 0 to it. SWRST = 0 on device reset.	—	—	—	—	TESTEN_BB Transmit and Receive Test Enable Bit, Bank B, Channel B. When TESTEN = 1, the transmit and receive sections are placed in test mode. TESTEN = 0 on device reset. When the global test enable bit GTESTEN = 0, the individual channel test enable bits are used to selectively place a channel in test or normal mode. When GTESTEN = 1, all channels are set to test mode regardless of their TESTEN setting.	40
30124	—	PRBS_BC Transmit and Receive PRBS Enable Bit, Bank B, Channel C. When PRBS = 1, the PRBS generator on the transmitter and the PRBS checker on the receiver are enabled. PRBS = 0 on device reset.	MASK_BC Transmit and Receive Alarm Mask Bit, Bank B, Channel C. When MASK = 1, the transmit and receive alarms of a channel are prevented from generating an interrupt. This MASK bit overrides the individual alarm mask bits in the Alarm Mask Registers. MASK = 1 on device reset.	SWRST_BC Transmit and Receive Software Reset Bit, Bank B, Channel C. When SWRST = 1, this bit provides the same function as the hardware reset, except all configuration register settings are preserved. This is not a self-clearing bit. Once set, this bit must be cleared by writing a 0 to it. SWRST = 0 on device reset.	—	—	—	—	TESTEN_BC Transmit and Receive Test Enable Bit, Bank B, Channel C. When TESTEN = 1, the transmit and receive sections are placed in test mode. TESTEN = 0 on device reset. When the global test enable bit GTESTEN = 0, the individual channel test enable bits are used to selectively place a channel in test or normal mode. When GTESTEN = 1, all channels are set to test mode regardless of their TESTEN setting.	40
30134	—	PRBS_BD Transmit and Receive PRBS Enable Bit, Bank B, Channel D. When PRBS = 1, the PRBS generator on the transmitter and the PRBS checker on the receiver are enabled. PRBS = 0 on device reset.	MASK_BD Transmit and Receive Alarm Mask Bit, Bank B, Channel D. When MASK = 1, the transmit and receive alarms of a channel are prevented from generating an interrupt. This MASK bit overrides the individual alarm mask bits in the Alarm Mask Registers. MASK = 1 on device reset.	SWRST_BD Transmit and Receive Software Reset Bit, Bank B, Channel D. When SWRST = 1, this bit provides the same function as the hardware reset, except all configuration register settings are preserved. This is not a self-clearing bit. Once set, this bit must be cleared by writing a 0 to it. SWRST = 0 on device reset.	—	—	—	—	TESTEN_BD Transmit and Receive Test Enable Bit, Bank B, Channel D. When TESTEN = 1, the transmit and receive sections are placed in test mode. TESTEN = 0 on device reset. When the global test enable bit GTESTEN = 0, the individual channel test enable bits are used to selectively place a channel in test or normal mode. When GTESTEN = 1, all channels are set to test mode regardless of their TESTEN setting.	40

Memory Map (continued)

Table 18. Memory Map (continued)

Addr (Hex)	Reg #	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	Default Value
SERDES B Global Control Register (Acts on Channels A, B, C, and D)										
30105	—	GPRBS_B Global Enable. The GPRBS bit globally enables the PRBS generators and checkers all four channels of SERDES B when GPRBS = 1. GPRBS = 0 on device reset.	GMASK_B Global Mask. The GMASK globally masks all the channel alarms of SERDES B when GMASK = 1. This prevents all the transmit and receive alarms from generating an interrupt. GMASK = 1 on device reset.	GSWRST_B RESET Function. The GSWRST bit provides the same function as the hardware reset for the transmit and receive sections of all four channels of ASERDES B, except that the device configuration settings are not affected when GSWRST is asserted. GSWRST = 0 on device reset. This is not a self-clearing bit. Once set, it must be cleared by writing a 0 to it.	GPWRDNT_B Powerdown Transmit Function. When GPWRDNT = 1, sections of the transmit hardware for all four channels of SERDES B are powered down to conserve power. GPWRDNT = 0 on device reset.	GPWRDNR_B Powerdown Receive Function. When GPWRDNR = 1, sections of the receive hardware for all four channels of SERDES B are powered down to conserve power. GPWRDNR = 0 on device reset.	GTRISTN_B Active-Low TRISTN Function. When GTRISTN = 0, the CMOS output buffers for SERDES B are 3-stated. GTRISTN = 1 on device reset.	—	GTESTEN_B Test Enable Control. When GTESTEN = 1, the transmit and receive sections of all four channels of SERDES B are placed in test mode. GTESTEN = 0 on device reset.	44
30106	—	TestMode	TestMode	TestMode	TestMode	TestMode	—	RSVD	RSVD	00

Memory Map (continued)

Table 18. Memory Map (continued)

Addr (Hex)	Reg #	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	Default Value
Control Registers B										
30900	B0	ENBYSYNC_BA 1 = Byte Alignments bank B, channelA	ENBYSYNC_BB 1 = Byte Alignments bank B, channel B	ENBYSYNC_BC 1 = Byte Alignments bank B, channel C	ENBYSYNC_BD 1 = Byte Alignments bank B, channel D	LCKREFN_BA 0 = Lock receiver to ref. clock 1 = Lock receiver to data for bank B channel A	LCKREFN_BB 0 = Lock receiver to ref. clock 1 = Lock receiver to data for bank B channel B	LCKREFN_BC 0 = Lock receiver to ref. clock 1 = Lock receiver to data for bank B channel C	LCKREFN_BD 0 = Lock receiver to ref. clock 1 = Lock receiver to data for bank B channel D	00
30901	B1	LOOPENB_BA Enable loopback mode for bank B, channel A	LOOPENB_BB Enable loopback mode for bank B, channel B	LOOPENB_BC Enable loopback mode for bank B, channel C	LOOPENB_BD Enable loopback mode for bank B, channel D	NOWDALIGN_BA Defeats deMUX alignment for bank B, channel A	NOWDALIGN_BB Defeats deMUX alignment for bank B, channel B	NOWDALIGN_BC Defeats deMUX alignment for bank B, channel C	NOWDALIGN_BD Defeats deMUX alignment for bank B, channel D	00
30902	B2	Reserved for future use								
30903	B3	Reserved for future use								
30910	B4	DOWDALIGN_BA Force new deMUX word alignment for bank B, channel A	DOWDALIGN_BB Force new deMUX word alignment for bank B, channel B	DOWDALIGN_BC Force new deMUX word alignment for bank B, channel C	DOWDALIGN_BD Force new deMUX word alignment for bank B, channel D	FMPU_STR_EN_BA Enable alignment function for channel BA	FMPU_STR_E_BB Enable alignment function for channel BB	FMPU_STR_EN_BC Enable alignment function for channel BC	FMPU_STR_EN_BD Enable alignment function for channel BD	00
30911	B5*	FMPU_SYNMODE_BA[0:1] Sync mode for BA		FMPU_SYNMODE_BB[0:1] Sync mode for BB		FMPU_SYNMODE_BC[0:1] Sync mode for BC		FMPU_SYNMODE_BD[0:1] Sync mode for BD		00
30912	B6	Reserved for future use								
30913	B7	Reserved for future use								
30920	B8	FMPU_RESYNC1_BA Resync a single channel, BA. Write a 0, then write a 1.	FMPU_RESYNC1_BB Resync a single channel, BB. Write a 0, then write a 1.	FMPU_RESYNC1_BC Resync a single channel, BC. Write a 0, then write a 1.	FMPU_RESYNC1_BD Resync a single channel, BD. Write a 0, then write a 1.	FMPU_RESYNC2_B1 Resync 2 channels, BA and BB. Write a 0, then write a 1.	FMPU_RESYNC2_B2 Resync 2 channels, BC and BD. Write a 0, then write a 1.	FMPU_RESYNC4_B Resync 4 channels B[A:D]. Write a 0, then write a 1.	XAUI_MODE B Controls use of XAUI link state machine vs. SERDES link State machine for bank B	00
30921	B9	NOCHALGN B Bypass channel alignment deMUXed data directly to FPGA for bank B	Reserved for future use							00
30922	B10	Reserved for future use								
30923	B11	Reserved for future use								
30930	B12	Reserved for future use								
30931	B13	Reserved for future use								
30932	B14	Reserved for future use								
30933	B15†	Reserved for future use				SCHAR_CHAN[0:1] Select channel to test		SCHAR_TXSEL 1=Select TX option 0=Select RX option	SCHAR_ENA 1=Enable Characterization of SERDES B	00

* FMPU_SYNMODE_xx[0:1]
00 = No channel alignment
10 = Twin channel alignment
01 = Quad channel alignment
11 = 8 channel alignment

† SCHAR_CHAN[0:1]
00 = Channel BA
10 = Channel BB
01 =Channel BC
11 = Channel BD

Memory Map (continued)

Table 18. Memory Map (continued)

Addr (Hex)	Reg #	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	Default Value
Status Register B										
30904	B16	XAUISTAT_BA[0:1]* Status of XAUI link state machine for bank B, channel A		XAUISTAT_BB[0:1]* Status of XAUI link state machine for bank B, channel B		XAUISTAT_BC[0:1]* Status of XAUI link state machine for bank B, channel C		XAUISTAT_BD[0:1]* Status of XAUI link state machine for bank B, channel D		00
30905	B17	DEMUXWAS_BA Status of deMUX word alignment for bank B, channel A	DEMUXWAS_BB Status of deMUX word alignment for bank B, channel B	DEMUXWAS_BC Status of deMUX word alignment for bank B, channel C	DEMUXWAS_BD Status of deMUX word alignment for bank B, channel D	CH248_SYNC_BA Alignment completed for BA	CH248_SYNC_BB Alignment completed for BB	CH248_SYNC_BC Alignment completed for BC	CH248_SYNC_BD Alignment completed for BD	00
30906	B18	Reserved for future use								
30907	B19	Reserved for future use								
30914	B20	SYNC2_B1_OVFL Alignment FIFO overflow for BA and BB	SYNC2_B2_OVFL Alignment FIFO overflow for BD and BC	SYNC4_B_OVFL Alignment FIFO overflow for B[A:D]	SYNC2_B1_OOS Alignment out of sync for BB and BA	SYNC2_B2_OOS Alignment out of sync for BC and BD	SYNC4_B_OOS Alignment out of sync for B[A:D]	Reserved for Future Use		00
30915	B21	Reserved for future use								
30916	B22	Reserved for future use								
30917	B23	Reserved for future use								
30924	B24	Reserved for future use								
30925	B25	Reserved for future use								
30926	B26	Reserved for future use								
30927	B27	Reserved for future use								
30934	B28	Reserved for future use								
30935	B29	Reserved for future use								
30936	B30	Reserved for future use								
30937	B31	Reserved for future use								

* For XAUISTAT_By[0:1] (address 0x30904), the definitions of these bits are:
00—No synchronization.
10—Synchronization done.
01,11—Not used.

Memory Map (continued)

Table 18. Memory Map (continued)

Addr (Hex)	Reg #	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	Default Value
Common Control Registers										
30A00	C0	TCKSELA* Controls source of 78 MHz TCK78 for bank A		RCKSELA † Controls source of 78 MHz RCK78 for bank A		TCKSELB Controls source of 78 MHz TCK78 for bank B		RCKSELB controls source of 78 MHz RCK78 for bank B		00
30A01	C1‡	Reserved for future use					RX_FIFO_MIN - Bits x, y, z Threshold for low address in RX_FIFO's			00
30A02	C2	RX_FIFO_MIN - Bits u, w Threshold for low address in RX_FIFO's		FMPU_RESYNC8 Resync 8 channels, A[A:D], B[A:D]	Reserved for future use					00
Common Status Registers										
30A04	C4	SYNC8_OVFL Alignment FIFO over-flow for A[A:D], B[A:D]	SYNC8_OOS Alignment out of sync for A[A:D], B[A:D]	Reserved for future use						00
30A05	C5	Reserved for future use								

* TCKSEL(A,B)[0:1]
  00 = Channel A
  10 = Channel B
  01 = Channel C
  11 = Channel D

† RCKSEL(A,B)[0:1]
  00 = Channel A
  10 = Channel B
  01 = Channel C
  11 = Channel D

‡ RX_FIFO_MIN[0:4] = Bits {w, u, z, y, x}

Clocking Recommendations for ORT82G5

This document describes all the clocks in the ORT82G5 design and recommends clocking strategies for various applications.

Recommended Board-level Clocking for the ORT82G5

Option 1: Asynchronous Reference Clocks Between Rx and Tx Devices

Each board that uses the ORT82G5 as a transmit or receive device will have its own local reference clock as shown in Figure 19. Figure 19 shows the ORT82G5 device on the switch card receiving data on two of its channels from a separate source. Data tx1 is transmitted from a tx device with refclk1 as the reference clock and Data tx2 is transmitted from a tx device with refclk2 as the reference clock. Receive channel AA locks to the incoming data tx1 and receive channel AB locks to the incoming data tx2.

The advantage of this clocking scheme is the fact that it is not necessary to distribute a reference clock (typically 156 MHz for 10GE and 155.52 MHz for OC-192 applications) across a backplane.

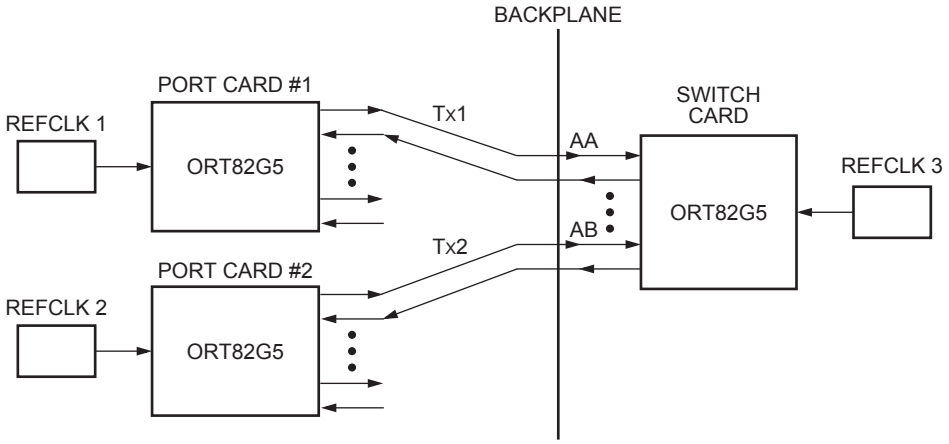


Figure 19. Asynchronous Clocking Between Rx and Tx Devices

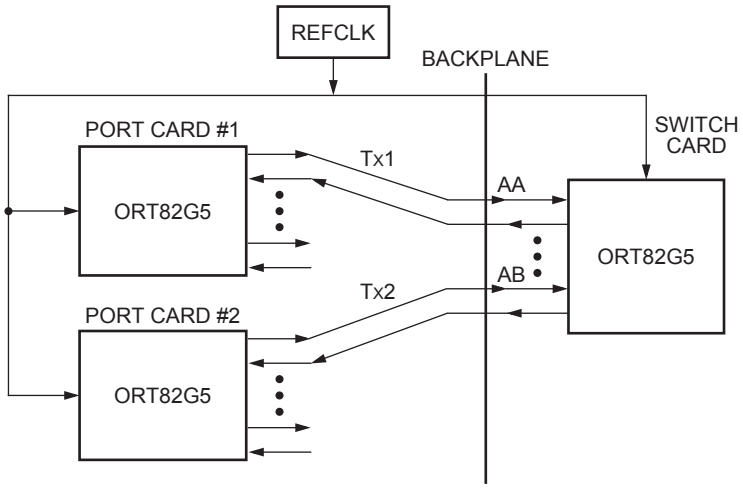
Clocking Recommendations for ORT82G5 (continued)

Option 2: Synchronous Reference Clocks to Rx and Tx Devices

In this type of clocking, a single reference clock is distributed to all receive and transmit devices in a system (Figure 20). This distributed clocking scheme will permit maximum flexibility in the usage of transmit and receive channels in the current silicon such as:

- All transmit and receive channels can be used within any quad in receive channel alignment or alignment bypass mode.
- In channel alignment mode, each receive channel operates on its own independent clock domain.

The disadvantage with this scheme is the fact that it is difficult to distribute a 156 MHz reference clock across a backplane. This may require expensive clock driver chips on the board to drive clocks to different destinations within the specified jitter limits for the reference clock.



2730(F)

Figure 20. Distributed Reference Clock to Rx And Tx Devices

Clocking Recommendations for ORT82G5 (continued)

On-board Clocking Strategies

The clocking diagrams shown in Figure 21 and Figure 23 involve the following:

- There are 2 clocks to the receive alignment fifos within a quad. Every twin within a quad can have a separate clock (Figure 21). These clocks are RSYS_CLK_A1 and RSYS_CLK_A2 for quad A which are used by channel pairs AA,AB and AC,AD respectively. RSYS_CLK_B1 and RSYS_CLK_B2 are clocks in quad B which are used by channel pairs BA,BB and BC,BD respectively.
- Every transmit channel has its own independent 77.76 MHz clock from FPGA to the low-speed MUX in the core. These clocks are TSYS_CLK_[AA, AB, . . . BD] as shown in Figure 23.

This enables the following clocking possibilities:

- All Rx and Tx channels within a quad can be used when channel alignment feature is enabled.
- In Rx channel alignment bypass mode, each receive channel operates on its own low speed clock domain RWCKxx. Note that the Rx alignment FIFO per channel cannot be used in this mode.
- When Rx twin-channel alignment is enabled, both twins within a quad can be sourced by clocks that are different from the other channels, but each pair of SERDES in Rx twin alignment must have the same clock, as shown in Figure 26. RSYS_CLK_A1 can be sourced from either RWCKAA or RWCKAB. For example, channel pairs AA and AB can be sourced from a work port card and channel pairs AC and AD can be sourced from a protect port card. Each of these port cards have their own local reference clock.
- For Rx quad alignment, RSYS_CLK_[A1,B1] and RSYS_CLK_[A2,B2] can be tied together as shown for quad A and B in Figure 25.
- In Rx eight-channel alignment, either RCK78A or RCK78B can be used to source RSYS_CLK_[A1,A2] and RSYS_CLK_[B1,B2] as shown in Figure 27.
- For Tx, TSYS_CLK_A[A:D] can be sourced by TCK78A and TSYS_CLK_B[A:D] can be sourced by TCK78B if the same transmit line rate exists for all 4 channels in a quad.
- If the transmit line rate is mixed between half and full-rate among the channels, then the scheme shown in Figure 24 can be used. The figure shows TSYS_CLK_AA being sourced by TCK78A and TSYS_CLK_AB being sourced by TCK78A/2 (the division is done in FPGA logic).
- In the Rx path, the channel alignment bypass mode allows mixing of half and full line rates among the 8 channels. The eight RWCKxx clock signals can be used to clock low speed receive data from the respective channel xx. Note that the Rx alignment FIFO per channel cannot be used in this mode.
- In Rx channel alignment mode, there are two levels of inputs that lead to multiple possibilities:
  — Each twin can be configured either in half-rate or full-rate mode as shown in Figure 22. The figure shows channel pair AA and AB configured in full-rate mode at 2.0 Gbits/s. This pair is sourced on the low speed side by RSYS_CLK_A1. Either RWCKAA or RWCKAB can be connected to RSYS_CLK_A1. Channel pair AC and AD are configure in half-rate mode at 1.0 Gbits/s and are sourced on the low speed side by RSYS_CLK_A2. Either RWCKAC or RWCKAD can be connected to RSYS_CLK_A2.
  — In addition each quad can be configured in any line rate (1.0—3.5 Gbits/s), since each quad has its own reference clock input pins.

Clocking Recommendations for ORT82G5 (continued)

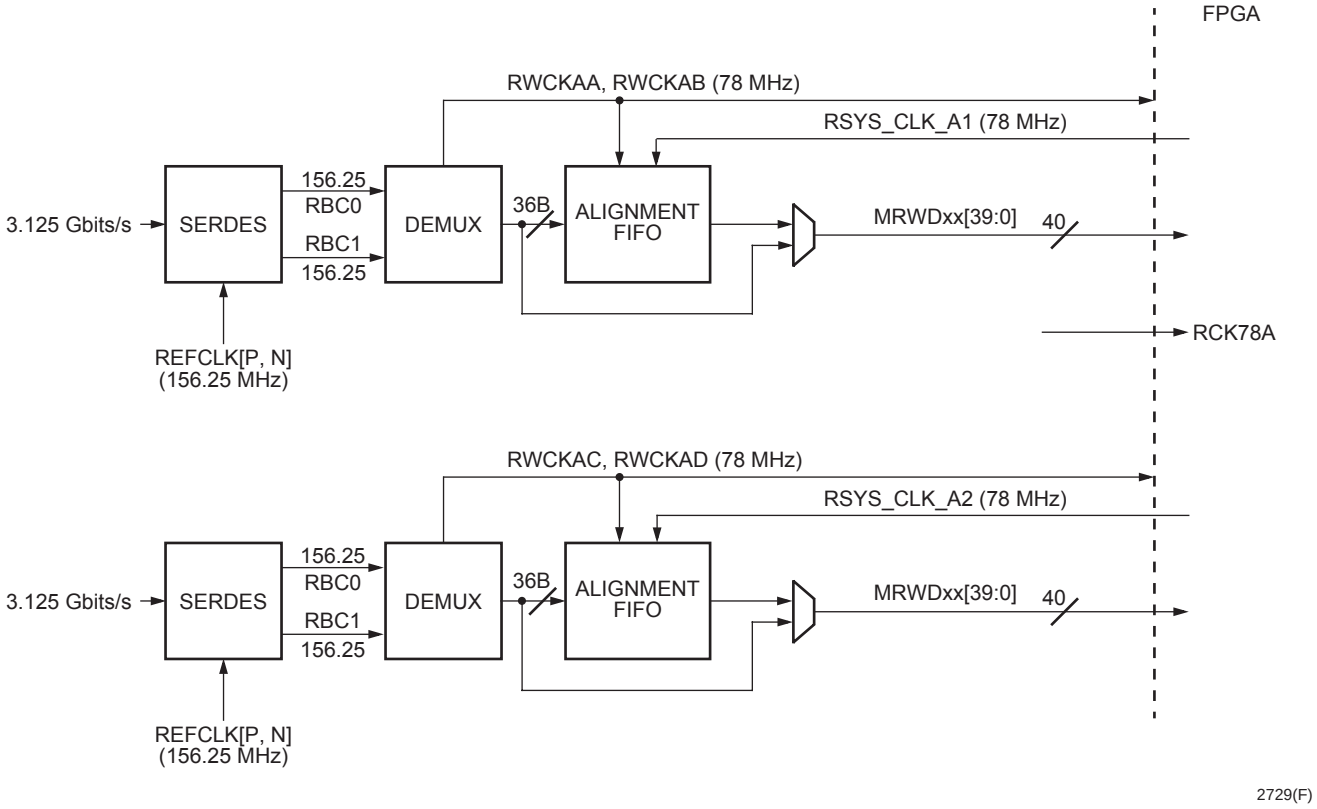


Figure 21. Receive Clocking for a Single Quad

Clocking Recommendations for ORT82G5 (continued)

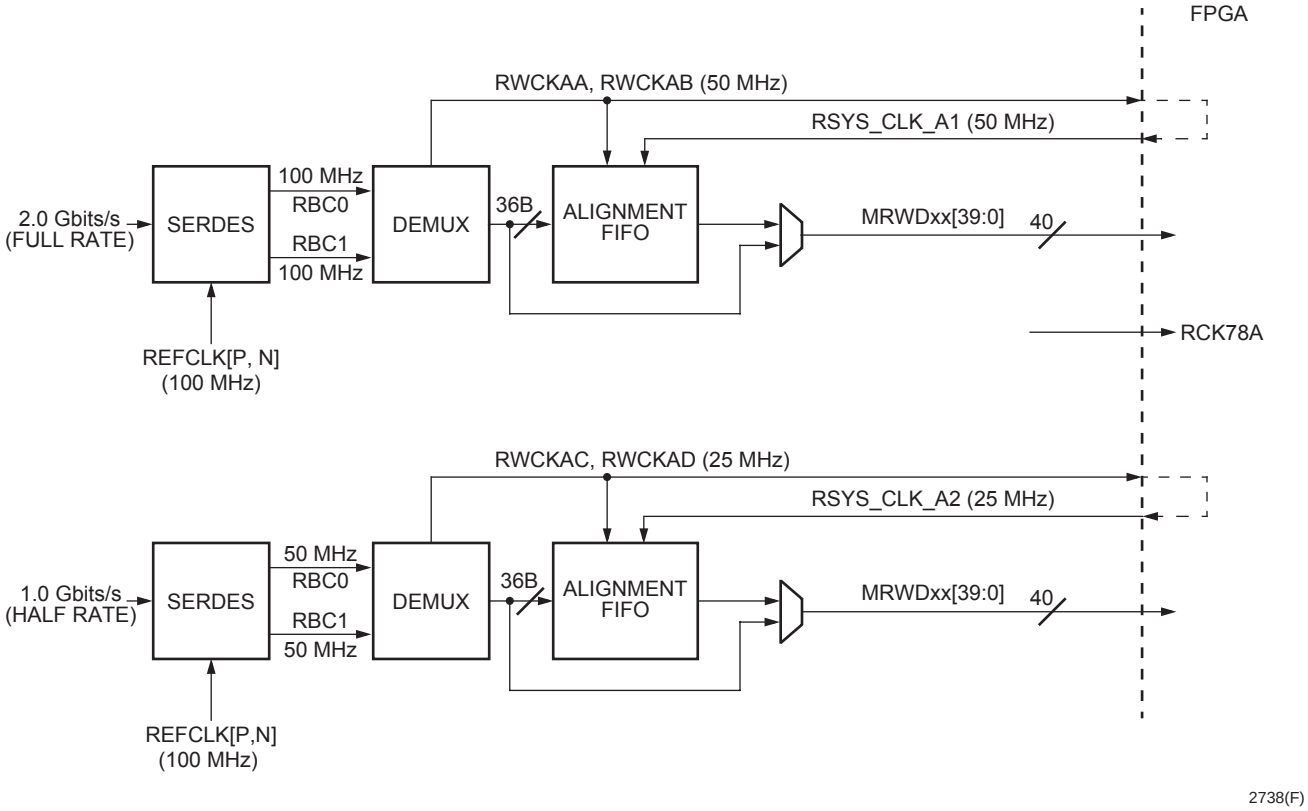
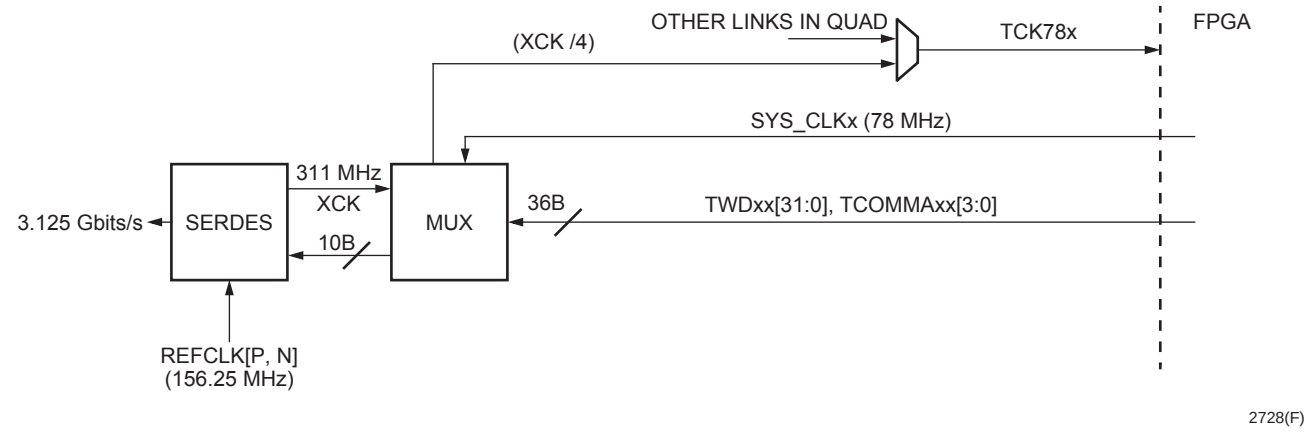


Figure 22. Receive Clocking Example for Mixed Line Rates



Total clocks from core to FPGA
TCK78x - 1 for each quad where x = A, B
Total clocks from FPGA to core
TSYS_CLK_xx - 1 for each channel
xx = (AA, AB,. . . BD)

Figure 23. Transmit Clocking in a Single Quad

Clocking Recommendations for ORT82G5 (continued)

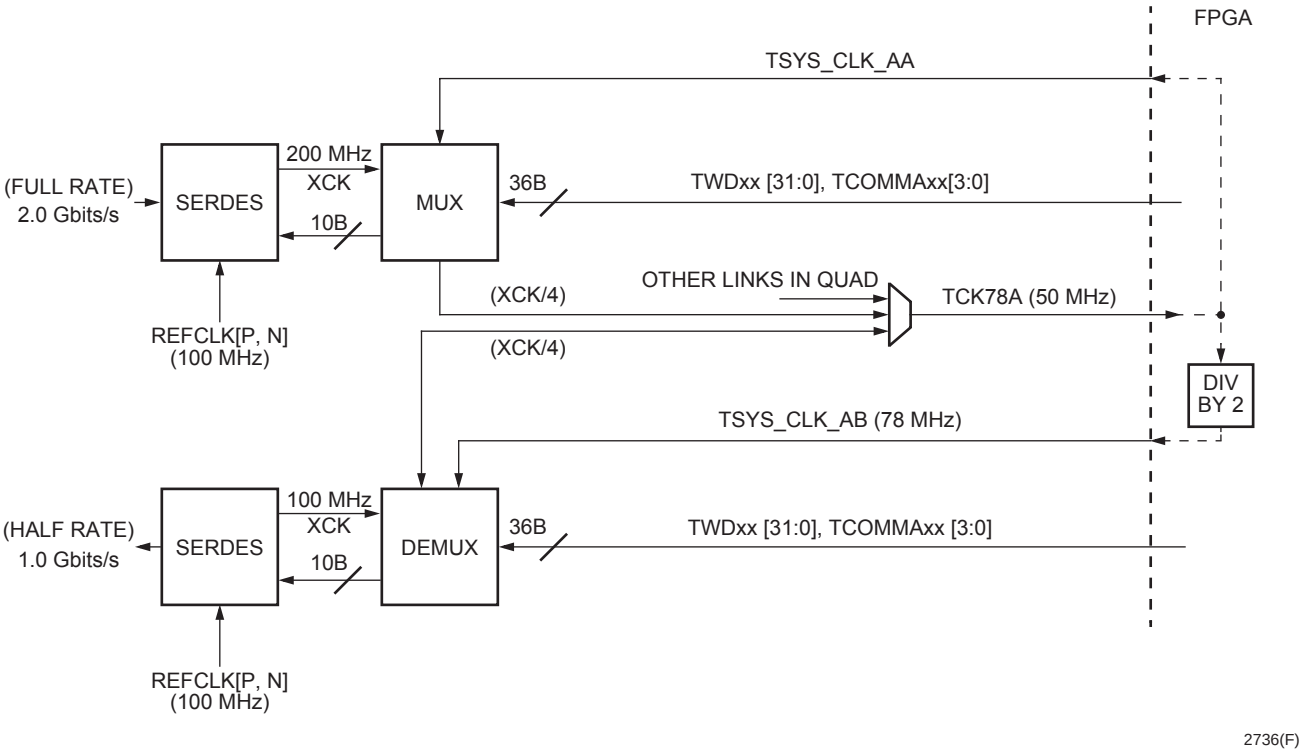


Figure 24. Transmit Clocking Strategy for Mixed Line Rates (Half- and Full-Rate)

Clocking Recommendations for ORT82G5 (continued)

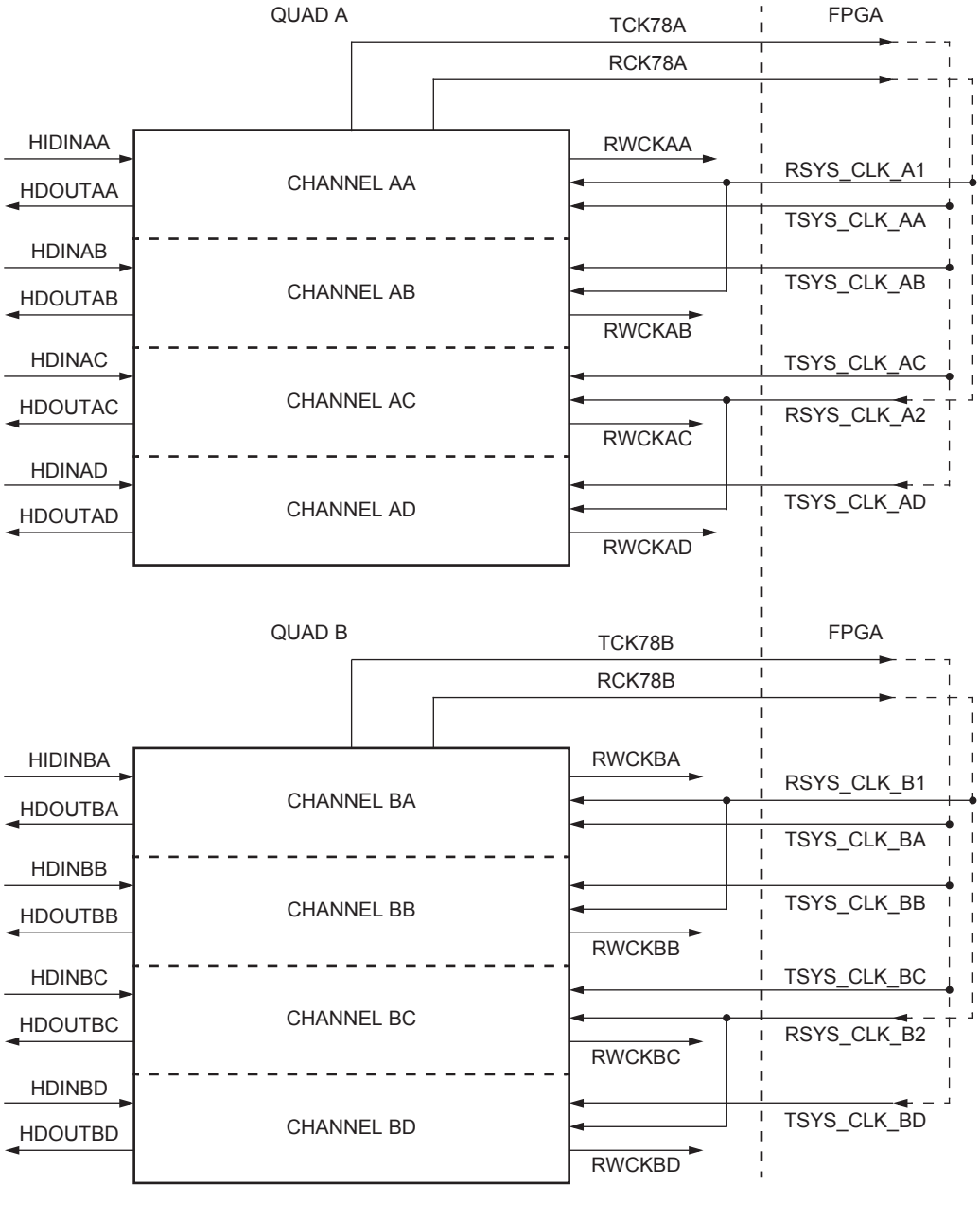


Figure 25. Example of Quad-Channel Alignment Clocking

Clocking Recommendations for ORT82G5 (continued)

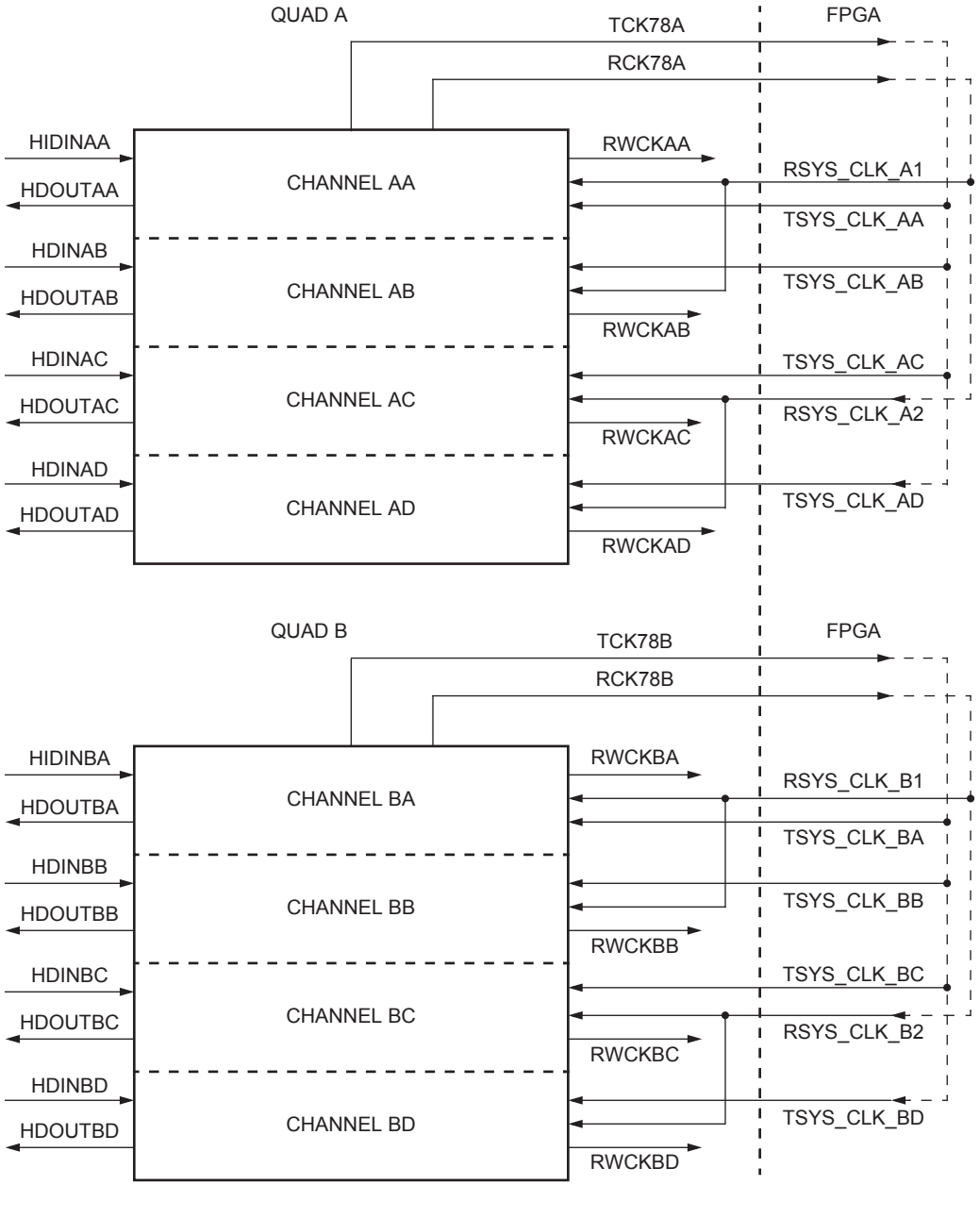


Figure 26. Example Twin-Channel Clocking Strategy

Clocking Recommendations for ORT82G5 (continued)

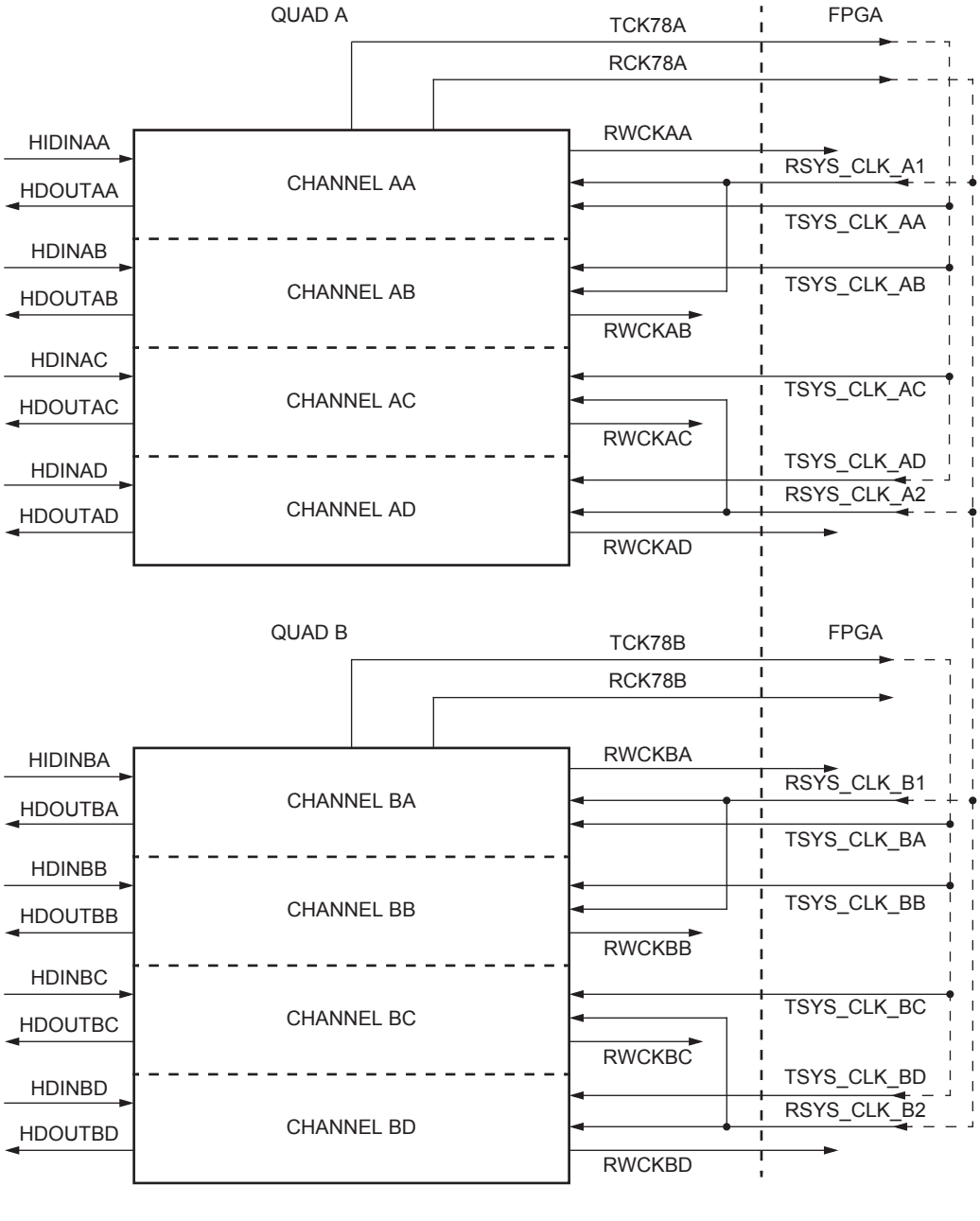


Figure 27. Example of Eight-channel Alignment

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

The *ORCA* Series 4 FPSCs include circuitry designed to protect the chips from damaging substrate injection currents and to prevent accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

Table 19. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	– 65	150	°C
Power Supply Voltage with Respect to Ground	$V_{DD}33$	– 0.3	4.2	V
	$V_{DD}IO$	– 0.3	4.2	V
	$V_{DD}15$	—	2	V
Input Signal with Respect to Ground	V_{IN}	V_{SS} – 0.3	$V_{DD}IO$ + 0.3	V
Signal Applied to High-impedance Output	—	V_{SS} – 0.3	$V_{DD}IO$ + 0.3	V
Maximum Package Body Temperature	—	—	220	°C

Recommended Operating Conditions

Table 20. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage with Respect to Ground*	$V_{DD}33$	3.0	3.6	V
	$V_{DD}15$	1.425	1.575	V
Input Voltages	V_{IN}	V_{SS} – 0.3	V_{DDIO} + 0.3	V
Junction Temperature†	T_J	– 40	125	°C

* For recommended operating conditions for $V_{DD}IO$, see the *Series 4 FPGA* Data Sheet and the *Series 4 I/O Buffer* Application Note.
† Designed for greater than 10 year electromigration life at 3.125 Gbits/s at 100 ˚C junction temperature.

SERDES Electrical and Timing Characteristics

Table 21. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Unit
Power Dissipation	SERDES, MUX/deMUX, Align FIFO, and I/O (per channel)	—	—	225	mW
	8b/10b encoder/decoder (per channel)	—	—	50	mW

Table 22. Recommended Operating Conditions

Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}15$ Supply Voltage ($V_{DD}15$, $V_{DD}Rx$, $V_{DD}Tx$, $V_{DD}AUX$, $V_{DD}GB$)	—	1.425	—	1.575	V
CML I/O Supply Voltage ($V_{DD}IB$, $V_{DD}OB$)	—	1.425	—	1.890	V

Note: $V_{DD}IB$ is the center tap of the CML input buffer. In some cases this signal may be left floating, or tied to another voltage level when not interfacing to CML output buffers. See the *SERDES CML Buffer Interface* Application note for details.

SERDES Electrical and Timing Characteristics (continued)

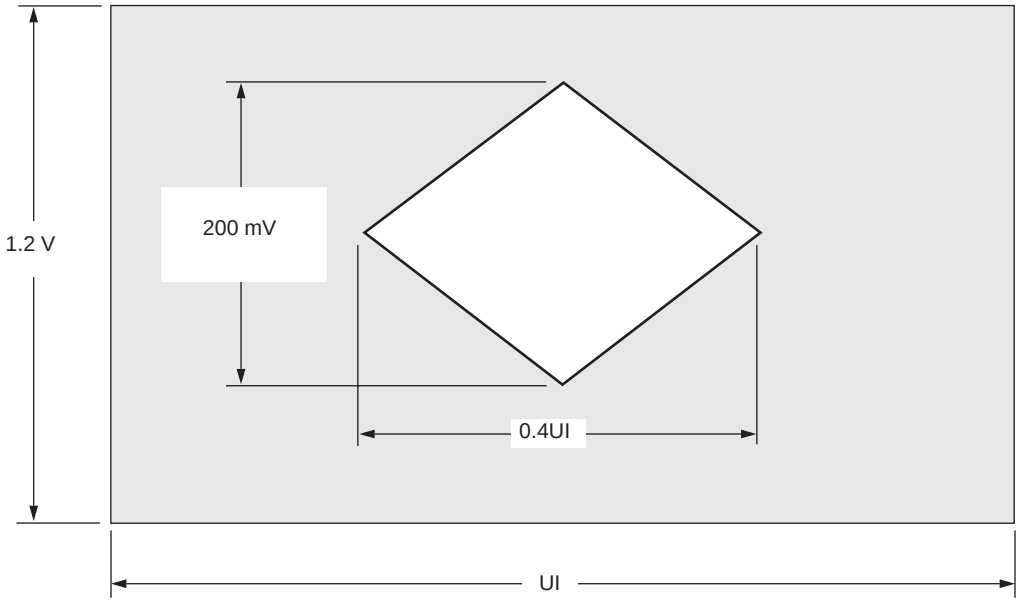


Figure 28. Receive Data Eye-Diagram Template (Differential)

Figure 28 provides a graphical characterization of the SERDES receiver input requirements. It provides guidance on a number of input parameters, including signal amplitude and rise time limits, noise and jitter limits, and P and N input skew tolerance. it is believed that incoming data patterns falling within the shaded region of the template will be received without error (BER < 10E-12), over all specified operating conditions.

Data pattern eye-opening at the receive end of a link is considered the ultimate measures of received signal quality. Almost all detrimental characteristics of transmit signal and the interconnection link design result in eye-closure. This combined with the eye-opening limitations of the line receiver can provide a good indication of a links ability to transfer data error-free.

Signal jitter is of special interest to system designers. It is often the primary limiting characteristic of long digital links and of systems with high noise level environments. An interesting characteristic of the clock and data recovery (CDR) portion of the ORT82G5 SERDES receiver is its ability to filter incoming signal jitter that is below the clock recovery PLL bandwidth (estimated to be about 3 MHz). For signals with high levels of low frequency jitter the receiver can detect incoming data, error-free, with eye-openings significantly less than that of Figure 28. This phenomena has been observed in the laboratory.

Eye-diagram measurement and simulation are excellent tools of design. They are both highly recommended when designing serial link interconnections and evaluating signal integrity.

Table 23. Receiver Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Input Data					
Stream of Nontransitions	—	—	—	60	Bits
Eye Opening Interval	—	0.4	—	—	U_{IP-P}
Eye Opening Voltage	—	200	—	—	mV_{P-P}

HSI Electrical and Timing Characteristics (continued)

Table 24. Reference Clock Specifications (REFINP and REFINN)

Parameter	Min	Typ	Max	Unit
Frequency Range	100	—	175	MHz
Frequency Tolerance	– 100	—	100	ppm
Duty Cycle (Measured at 50% Amplitude Point)	40	50	60	%
Rise Time	—	500	1000	ps
Fall Time	—	500	1000	ps
P–N Input Skew	—	—	75	ps
Differential Amplitude	500	800	2 x V_{DD}	mV_{p-p}
Common Mode Level	$V_{single-ended/2}$	0.75	$V_{DD}15 – (V_{single-ended/2})$	V
Single-Ended Amplitude	250	400	$V_{DD}15$	mV_{p-p}
Input Capacitance (at REFINP)	—	—	5	pF
Input Capacitance (at REFINPIT)	—	—	3	pF
Inband (< 10 MHz) Jitter (2.5 Gbits/s)	—	—	30	ps_{p-p}
Inband (< 10 MHz) Jitter (1.25 Gbits/s)	—	—	60	ps_{p-p}

Note: Additional (<10 MHz) REFCLK jitter will increase the total transmit output jitter.

Table 25. Channel Output Jitter (1.25 Gbits/s)

Parameter	Min	Typ	Max	Unit
Deterministic	—	—	0.08	UI_{p-p}
Random	—	—	0.12	UI_{p-p}
Total	—	—	0.20	UI_{p-p}

Table 26. Channel Output Jitter (2.5 Gbits/s)

Parameter	Min	Typ	Max	Unit
Deterministic	—	—	0.10	UI_{p-p}
Random	—	—	0.14	UI_{p-p}
Total	—	—	0.24	UI_{p-p}

Table 27. Serial Output Timing and Levels (CML I/O)

Parameter	Min	Typ	Max	Unit
Rise Time (20%—80%)	50	80	110	ps
Fall Time (80%—20%)	50	80	110	ps
Common Mode	$V_{DD}OB$ –0.30	$V_{DD}OB$ –0.25	$V_{DD}OB$ –0.15	V
Differential Swing (Full Amplitude)	800	900	1100	mV_{p-p}
Differential Swing (Half Amplitude)	400	500	600	mV_{p-p}
Output Load	—	50	—	Ω

Note: Differential swings are based on direct CML to CML connections.

HSI Electrical and Timing Characteristics (continued)

Table 28. Serial Input Timing and Levels (CML I/O)

Parameter	Min	Typ	Max	Unit
Rise Time (See Eye Diagram in Table 28)	—	—	—	ps
Fall Time (See Eye Diagram in Table 28)	—	—	—	ps
Differential Swing	200	—	—	mV_{p-p}
Common-mode Level	0.5	—	$V_{DD}15$	V
Internal Buffer Resistance (Each input to $V_{DD}IB$)	40	50	60	Ω

Pin Information

Pin Descriptions

This section describes the pins found on the Series 4 FPGAs. Any pin not described in this table is a user-programmable I/O. During configuration, the user-programmable I/Os are 3-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also 3-stated with an internal pull-up resistor enabled after configuration. The pin descriptions in Table 29 and throughout this data sheet show active-low signals with an overscore. The package pinout tables that follow, show this as a signal ending with _N. For example $\overline{\text{LDC}}$ and LDC_N are equivalent.

Table 29. Pin Descriptions

Symbol	I/O	Description
Dedicated Pins		
$V_{DD}33$	—	3.3 V positive power supply. This power supply is used for 3.3 V configuration RAMs and internal PLLs. When using PLLs, this power supply should be well isolated from all other power supplies on the board for proper operation.
$V_{DD}15$	—	1.5 V positive power supply for internal logic.
$V_{DD}IO$	—	Positive power supply used by I/O banks.
V_{SS}	—	Ground.
PTEMP	I	Temperature sensing diode pin. Dedicated input.
$\overline{\text{RESET}}$	I	During configuration, $\overline{\text{RESET}}$ forces the restart of configuration and a pull-up is enabled. After configuration, $\overline{\text{RESET}}$ can be used as a general FPGA input or as a direct input, which causes all PLC latches/FFs to be asynchronously set/reset.
CCLK	O	In the master and asynchronous peripheral modes, CCLK is an output which strobes configuration data in.
	I	In the slave or readback after configuration, CCLK is input synchronous with the data on DIN or D[7:0]. CCLK is an output for daisy-chain operation when the lead device is in master, peripheral, or system bus modes.
DONE	I	As an input, a low level on DONE delays FPGA start-up after configuration.*
	O	As an active-high, open-drain output, a high level on this signal indicates that configuration is complete. DONE has an optional pull-up resistor.
$\overline{\text{PRGM}}$	I	$\overline{\text{PRGM}}$ is an active-low input that forces the restart of configuration and resets the boundary-scan circuitry. This pin always has an active pull-up.
$\overline{\text{RD\_CFG}}$	I	This pin must be held high during device initialization until the $\overline{\text{INIT}}$ pin goes high. This pin always has an active pull-up. During configuration, $\overline{\text{RD\_CFG}}$ is an active-low input that activates the TS_ALL function and 3-states all of the I/O. After configuration, $\overline{\text{RD\_CFG}}$ can be selected (via a bit stream option) to activate the TS_ALL function as described above, or, if readback is enabled via a bit stream option, a high-to-low transition on $\overline{\text{RD\_CFG}}$ will initiate readback of the configuration data, including PFU output states, starting with frame address 0.
RD_DATA/TDO	O	RD_DATA/TDO is a dual-function pin. If used for readback, RD_DATA provides configuration data out. If used in boundary-scan, TDO is test data out.
$\overline{\text{CFG\_IRQ}}$/MPI_IRQ	O	During JTAG, slave, master, and asynchronous peripheral configuration assertion on this $\overline{\text{CFG\_IRQ}}$ (active-low) indicates an error or errors for block RAM or FPSC initialization. MPI active-low interrupt request output, when the MPI is used.

* The FPGA States of Operation section contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Pin Information (continued)

Table 29. Pin Descriptions (continued)

Symbol	I/O	Description
Special-Purpose Pins		
M[3:0]	I	During powerup and initialization, M0—M3 are used to select the configuration mode with their values latched on the rising edge of $\overline{\text{INIT}}$. During configuration, a pull-up is enabled.
	I/O	After configuration, these pins are user-programmable I/O.*
PLL_CK[0:7][TC]	I	Semi-dedicated PLL clock pins. During configuration they are 3-stated with a pull up.
	I/O	These pins are user-programmable I/O pins if not used by PLLs after configuration.
P[TBLR]CLK[1:0][TC]	I	Pins dedicated for the primary clock. Input pins on the middle of each side with differential pairing.
	I/O	After configuration these pins are user programmable I/O, if not used for clock inputs.
TDI, TCK, TMS	I	If boundary-scan is used, these pins are test data in, test clock, and test mode select inputs. If boundary-scan is not selected, all boundary-scan functions are inhibited once configuration is complete. Even if boundary-scan is not used, either TCK or TMS must be held at logic 1 during configuration. Each pin has a pull-up enabled during configuration.
	I/O	After configuration, these pins are user-programmable I/O if boundary scan is not used.*
RDY/$\overline{\text{BUSY}}$/RCLK	O	During configuration in asynchronous peripheral mode, RDY/RCLK indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D7 in asynchronous peripheral mode. During the master parallel configuration mode, RCLK is a read output signal to an external memory. This output is not normally used.
	I/O	After configuration this pin is a user-programmable I/O pin.*
HDC	O	High during configuration is output high until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.*
$\overline{\text{LDC}}$	O	$\overline{\text{Low during configuration}}$ is output low until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.*
$\overline{\text{INIT}}$	I/O	$\overline{\text{INIT}}$ is a bidirectional signal before and during configuration. During configuration, a pull-up is enabled, but an external pull-up resistor is recommended. As an active-low open-drain output, $\overline{\text{INIT}}$ is held low during power stabilization and internal clearing of memory. As an active-low input, $\overline{\text{INIT}}$ holds the FPGA in the wait-state before the start of configuration. After configuration, this pin is a user-programmable I/O pin.*
$\overline{\text{CS0}}$, CS1	I	$\overline{\text{CS0}}$ and CS1 are used in the asynchronous peripheral, slave parallel, and microprocessor configuration modes. The FPGA is selected when $\overline{\text{CS0}}$ is low and CS1 is high. During configuration, a pull-up is enabled.
	I/O	After configuration, if MPI is not used, these pins are user-programmable I/O pins.*
$\overline{\text{RD}}$/$\overline{\text{MPI\_STRB}}$	I	$\overline{\text{RD}}$ is used in the asynchronous peripheral configuration mode. A low on $\overline{\text{RD}}$ changes D[7:3] into a status output. $\overline{\text{WR}}$ and $\overline{\text{RD}}$ should not be used simultaneously. If they are, the write strobe overrides. This pin is also used as the MPI data transfer strobe. As a status indication, a high indicates ready, and a low indicates busy.
	I/O	After configuration, if the MPI is not used, this pin is a user-programmable I/O pin.*

* The FPGA States of Operation section contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Pin Information (continued)

Table 29. Pin Descriptions (continued)

Symbol	I/O	Description
Special-Purpose Pins (continued)		
$\overline{WR}$/MPI_RW	I	$\overline{WR}$ is used in asynchronous peripheral mode. A low on $\overline{WR}$ transfers data on D[7:0] to the FPGA. In MPI mode, a high on MPI_RW allows a read from the data bus, while a low causes a write transfer to the FPGA.
	I/O	After configuration, if the MPI is not used, $\overline{WR}$/MPI_RW is a user-programmable I/O pin.*
PPC_A[14:31]	I	During MPI mode the PPC_A[14:31] are used as the address bus driven by the *PowerPC* bus master utilizing the least-significant bits of the *PowerPC* 32-bit address.
$\overline{MPI\_BURST}$	I	$\overline{MPI\_BURST}$ is driven low to indicate a burst transfer is in progress in MPI mode. Driven high indicates that the current transfer is not a burst.
$\overline{MPI\_BDIP}$	I	$\overline{MPI\_BDIP}$ is driven by the *PowerPC* processor in MPI mode. Assertion of this pin indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase.
MPI_TSZ[0:1]	I	MPI_TSZ[0:1] signals are driven by the bus master in MPI mode to indicate the data transfer size for the transaction. Set 01 for byte, 10 for half-word, and 00 for word.
A[21:0]	O	During master parallel mode A[21:0] address the configuration EPROMs up to 4M bytes.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.*
$\overline{MPI\_ACK}$	O	In MPI mode this is driven low indicating the MPI received the data on the write cycle or returned data on a read cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.*
MPI_CLK	I	This is the *PowerPC* synchronous, positive-edge bus clock used for the MPI interface. It can be a source of the clock for the embedded system bus. If MPI is used this will be the *AMBA* bus clock.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.*
$\overline{MPI\_TEA}$	O	A low on the MPI transfer error acknowledge indicates that the MPI detects a bus error on the internal system bus for the current transaction.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.*
$\overline{MPI\_RTRY}$	O	This pin requests the MPC860 to relinquish the bus and retry the cycle.
	I/O	If not used for MPI these pins are user-programmable I/O pins after configuration.*
D[0:31]	I/O	Selectable data bus width from 8, 16, 32-bit in MPI mode. Driven by the bus master in a write transaction and driven by MPI in a read transaction.
	I	D[7:0] receive configuration data during master parallel, peripheral, and slave parallel configuration modes when $\overline{WR}$ is low and each pin has a pull-up enabled. During serial configuration modes, D0 is the DIN input.
	O	D[7:3] output internal status for asynchronous peripheral mode when $\overline{RD}$ is low.
	I/O	After configuration, if MPI is not used, the pins are user-programmable I/O pins.*
DP[0:3]	I/O	Selectable parity bus width in MPI mode from 1, 2, 4-bit, DP[0] for D[0:7], DP[1] for D[8:15], DP[2] for D[16:23], and DP[3] for D[24:31]. After configuration, if MPI is not used, the pins are user-programmable I/O pin.*

* The FPGA States of Operation section contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Pin Information (continued)

Table 29. Pin Descriptions (continued)

Symbol	I/O	Description
Special-Purpose Pins (continued)		
DIN	I	During slave serial or master serial configuration modes, DIN accepts serial configuration data synchronous with CCLK. During parallel configuration modes, DIN is the D0 input. During configuration, a pull-up is enabled.
	I/O	After configuration, this pin is a user-programmable I/O pin.*
DOUT	O	During configuration, DOUT is the serial data output that can drive the DIN of daisy-chained slave devices. Data out on DOUT changes on the rising edge of CCLK.
	I/O	After configuration, DOUT is a user-programmable I/O pin.*
TESTCFG	I	During configuration this pin should be held high, to allow configuration to occur. A pull up is enabled during configuration.
	I/O	After configuration, TESTCFG is a user programmable I/O pin.*

* The FPGA States of Operation section contains more information on how to control these signals during start-up. The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Pin Information (continued)

This section describes device I/O signals to/from the embedded core excluding the signals at the CIC boundary.

Table 30. FPSC Function Pin Description

Symbol	I/O	Description
Common Signals for Both SERDES A and B		
PASB_RESETN	I	Active low reset for the embedded core. All non-SERDES specific registers (addresses 308***, 309***, 30A***) in the embedded core are not reset.
PASB_TRISTN	I	Active low 3-state for embedded core output buffers.
PASB_PDN	I	Active low power down of all SERDES blocks and associated I/Os.
PASB_TESTCLK	I	Clock input for BIST and loopback test.
PBIST_TEST_ENN	I	Selection of PASB_TESTCLK input for BIST test.
PLOOP_TEST_ENN	I	Selection of PASB_TESTCLK input for loopback test.
PMP_TESTCLK	I	Clock input for microprocessor in test mode.
PMP_TESTCLK_ENN	I	Selection of PMP_TESTCLK in test mode.
PSYS_DOBISTN	I	Input to start BIST test.
PSYS_RSSIG_ALL	O	Output result of BIST test.
SERDES A and B Pins		
REFCLKN_A	I	CML reference clock input—SERDES A.
REFCLKP_A	I	CML reference clock input—SERDES A.
REFCLKN_B	I	CML reference clock input—SERDES B.
REFCLKP_B	I	CML reference clock input—SERDES B.
REXT_A	I	Reference resistor—SERDES A.
REXT_B	I	Reference resistor—SERDES B.
REXTN_A	I	Reference resistor—SERDES A. A 3.32 K Ω ± 1% resistor must be connected across REXT_A and REXTN_A.
REXTN_B	I	Reference resistor—SERDES B. A 3.32 K Ω ± 1% resistor must be connected across REXT_B and REXTN_B.
HDINN_AA	I	High-speed CML receive data input—SERDES A, channel A.
HDINP_AA	I	High-speed CML receive data input—SERDES A, channel A.
HDINN_AB	I	High-speed CML receive data input—SERDES A, channel B.
HDINP_AB	I	High-speed CML receive data input—SERDES A, channel B.
HDINN_AC	I	High-speed CML receive data input—SERDES A, channel C.
HDINP_AC	I	High-speed CML receive data input—SERDES A, channel C.
HDINN_AD	I	High-speed CML receive data input—SERDES A, channel D.
HDINP_AD	I	High-speed CML receive data input—SERDES A, channel D.
HDINN_BA	I	High-speed CML receive data input—SERDES B, channel A.
HDINP_BA	I	High-speed CML receive data input—SERDES B, channel A.
HDINN_BB	I	High-speed CML receive data input—SERDES B, channel B.
HDINP_BB	I	High-speed CML receive data input—SERDES B, channel B.
HDINN_BC	I	High-speed CML receive data input—SERDES B, channel C.
HDINP_BC	I	High-speed CML receive data input—SERDES B, channel C.
HDINN_BD	I	High-speed CML receive data input—SERDES B, channel D.
HDINP_BD	I	High-speed CML receive data input—SERDES B, channel D.

Pin Information (continued)

Table 30. FPSC Function Pin Description (continued)

Symbol	I/O	Description
SERDES A and B Pins		
HDOUTN_AA	O	High-speed CML transmit data output—SERDES A, channel A.
HDOUTP_AA	O	High-speed CML transmit data output—SERDES A, channel A.
HDOUTN_AB	O	High-speed CML transmit data output—SERDES A, channel B.
HDOUTP_AB	O	High-speed CML transmit data output—SERDES A, channel B.
HDOUTN_AC	O	High-speed CML transmit data output—SERDES A, channel C.
HDOUTP_AC	O	High-speed CML transmit data output—SERDES A, channel C.
HDOUTN_AD	O	High-speed CML transmit data output—SERDES A, channel D.
HDOUTP_AD	O	High-speed CML transmit data output—SERDES A, channel D.
HDOUTN_BA	O	High-speed CML transmit data output—SERDES B, channel A.
HDOUTP_BA	O	High-speed CML transmit data output—SERDES B, channel A.
HDOUTN_BB	O	High-speed CML transmit data output—SERDES B, channel B.
HDOUTP_BB	O	High-speed CML transmit data output—SERDES B, channel B.
HDOUTN_BC	O	High-speed CML transmit data output—SERDES B, channel C.
HDOUTP_BC	O	High-speed CML transmit data output—SERDES B, channel C.
HDOUTN_BD	O	High-speed CML transmit data output—SERDES B, channel D.
HDOUTP_BD	O	High-speed CML transmit data output—SERDES B, channel D.
Power and Ground		
V_{DD}IB_AA	—	1.8 V/1.5 V power supply for high-speed serial input buffers.
V_{DD}IB_AB	—	1.8 V/1.5 V power supply for high-speed serial input buffers.
V_{DD}IB_AC	—	1.8 V/1.5 V power supply for high-speed serial input buffers.
V_{DD}IB_AD	—	1.8 V/1.5 V power supply for high-speed serial input buffers.
V_{DD}IB_BA	—	1.8 V/1.5 V power supply for high-speed serial input buffers.
V_{DD}IB_BB	—	1.8 V/1.5 V power supply for high-speed serial input buffers.
V_{DD}IB_BC	—	1.8 V/1.5 V power supply for high-speed serial input buffers.
V_{DD}IB_BD	—	1.8 V/1.5 V power supply for high-speed serial input buffers.
V_{DD}OB_AA	—	1.8 V/1.5 V power supply for high-speed serial output buffers.
V_{DD}OB_AB	—	1.8 V/1.5 V power supply for high-speed serial output buffers.

Pin Information (continued)

Table 30. FPSC Function Pin Description (continued)

Symbol	I/O	Description
VDDOB_AC	—	1.8 V/1.5 V power supply for high-speed serial output buffers.
VDDOB_AD	—	1.8 V/1.5 V power supply for high-speed serial output buffers.
VDDOB_BA	—	1.8 V/1.5 V power supply for high-speed serial output buffers.
VDDOB_BB	—	1.8 V/1.5 V power supply for high-speed serial output buffers.
VDDOB_BC	—	1.8 V/1.5 V power supply for high-speed serial output buffers.
VDDOB_BD	—	1.8 V/1.5 V power supply for high-speed serial output buffers.
VSSRX_AA	—	SERDES analog receive circuitry ground.
VSSRX_AB	—	SERDES analog receive circuitry ground.
VSSRX_AC	—	SERDES analog receive circuitry ground.
VSSRX_AD	—	SERDES analog receive circuitry ground.
VSSRX_BA	—	SERDES analog receive circuitry ground.
VSSRX_BB	—	SERDES analog receive circuitry ground.
VSSRX_BC	—	SERDES analog receive circuitry ground.
VSSRX_BD	—	SERDES analog receive circuitry ground.
VSSGB_A	—	Guard band ground.
VSSGB_B	—	Guard band ground.
VDDGB_A	—	1.5 V guard band power supply.
VDDGB_B	—	1.5 V guard band power supply.
VSSAUX_A	—	SERDES auxiliary circuit ground (no external pin).
VSSAUX_B	—	SERDES auxiliary circuit ground.
VSSIB_AA	—	High-speed input receive buffer ground (no external pin).
VSSIB_AB	—	High-speed input receive buffer ground.
VSSIB_AC	—	High-speed input receive buffer ground.
VSSIB_AD	—	High-speed input receive buffer ground.
VSSIB_BA	—	High-speed input receive buffer ground.
VSSIB_BB	—	High-speed input receive buffer ground.
VSSIB_BC	—	High-speed input receive buffer ground.
VSSIB_BD	—	High-speed input receive buffer ground.
VSSOB_AA	—	High-speed output transmit buffer ground (no external pin).
VSSOB_AB	—	High-speed output transmit buffer ground.
VSSOB_AC	—	High-speed output transmit buffer ground.
VSSOB_AD	—	High-speed output transmit buffer ground.
VSSOB_BA	—	High-speed output transmit buffer ground.
VSSOB_BB	—	High-speed output transmit buffer ground.
VSSOB_BC	—	High-speed output transmit buffer ground.
VSSOB_BD	—	High-speed output transmit buffer ground.
VSSTX_AA	—	SERDES analog transmit circuitry ground (no external pin).
VSSTX_AB	—	SERDES analog transmit circuitry ground.
VSSTX_AC	—	SERDES analog transmit circuitry ground.
VSSTX_AD	—	SERDES analog transmit circuitry ground.
VSSTX_BA	—	SERDES analog transmit circuitry ground.

Pin Information (continued)

Table 30. FPSC Function Pin Description (continued)

Symbol	I/O	Description
VSSTX_BB	—	SERDES analog transmit circuitry ground.
VSSTX_BC	—	SERDES analog transmit circuitry ground.
VSSTX_BD	—	SERDES analog transmit circuitry ground.
VDDRX_AA	—	1.5 V Power supply for SERDES analog receive circuitry.
VDDRX_AB	—	1.5 V Power supply for SERDES analog receive circuitry.
VDDRX_AC	—	1.5 V Power supply for SERDES analog receive circuitry.
VDDRX_AD	—	1.5 V Power supply for SERDES analog receive circuitry.
VDDRX_BA	—	1.5 V Power supply for SERDES analog receive circuitry.
VDDRX_BB	—	1.5 V Power supply for SERDES analog receive circuitry.
VDDRX_BC	—	1.5 V Power supply for SERDES analog receive circuitry.
VDDRX_BD	—	1.5 V Power supply for SERDES analog receive circuitry.
VDDAUX_A	—	1.5 V power supply for SERDES auxiliary circuit.
VDDAUX_B	—	1.5 V power supply for SERDES auxiliary circuit.

Pin Information (continued)

Power Supplies for ORT82G5

Power Supply Descriptions

Table 31 shows the ORT82G5 embedded core power supply connection groupings. The Tx-Rx digital power supplies are used for transmit and receive digital logic including the microprocessor logic. The Tx-Rx analog power supplies are used for high-speed analog circuitry between the I/O buffers and the digital logic. The Rx input buffer power supplies are used to power the input (receive) buffers. The Tx output buffer supplies are used to power the output (transmit) buffers. The Rx and Tx buffer power supplies can be independently set to 1.5 V or 1.8 V, depending on the end application. The auxiliary and guard band supplies are independent connection brought out to pins. In the ORT82G5, many of the VDD pins shown in Table 31 are connected together at the package substrate level. The same also applies for various VSS pins. At the package ball level in Table 33, the following names appear instead of the names in Table 31: VDDT, VDDR, VDDOB, VDDIB, VSST, VSSRX.

Table 31. Power Supply Pin Groupings

Tx-Rx Digital 1.5 V	Tx-Rx Analog 1.5 V (VDDT, VDDR)	Tx Output Buffers 1.5/1.8 V (VDDOB)	Rx Input Buffers 1.5 V/1.8 V (VDDIB)	Auxiliary 1.5 V (VDDAUX)	Guard Band 1.5 V (VDDGB)
VDD15	VDDRX_AA	VDDOB_AA	VDDIB_AA	VDDAUX_A	VDDGB_A
—	VDDTX_AA	VDDOB_AB	VDDIB_AB	VDDAUX_B	VDDGB_B
—	VDDRX_AB	VDDOB_AC	VDDIB_AC	—	—
—	VDDTX_AB	VDDOB_AD	VDDIB_AD	—	—
—	VDDRX_AC	VDDOB_BA	VDDIB_BA	—	—
—	VDDTX_AC	VDDOB_BB	VDDIB_BB	—	—
—	VDDRX_AD	VDDOB_BC	VDDIB_BC	—	—
—	VDDTX_AD	VDDOB_BD	VDDIB_BD	—	—
—	VDDRX_BA	—	—	—	—
—	VDDTX_BA	—	—	—	—
—	VDDRX_BB	—	—	—	—
—	VDDTX_BB	—	—	—	—
—	VDDRX_BC	—	—	—	—
—	VDDTX_BC	—	—	—	—
—	VDDRX_BD	—	—	—	—
—	VDDTX_BD	—	—	—	—

Pin Information (continued)

Recommended Power Supply Connections

Ideally, a board should have four separate power supplies as described below:

- Tx-Rx digital auxiliary supplies.

The Tx-Rx digital and auxiliary power supply nodes should be supplied by a 1.5 V source. A single 1.5 V source can supply power to Tx-Rx digital and auxiliary nodes.

- Tx-Rx analog, guardband supplies.

A dedicated 1.5 V power supply should be provided to the analog power pins. This will allow the end user to minimize noise. The guard band pins can also be sourced from the analog power supplies.

- Tx output buffers.

The power supplies to the Tx output buffers should be isolated from the rest of the board power supplies. Special care must be taken to minimize noise when providing board level power to these output buffers. The power supply can be 1.5 V or 1.8 V depending on the end application.

- Rx input buffers.

The power supplies to the Rx input buffers should be isolated from the rest of the board power supplies. Special care must be taken to minimize noise when providing board level power to these input buffers. The power supply can be 1.5 V or 1.8 V depending on the end application.

Recommended Power Supply Filtering Scheme

The board connections of the various SERDES V_{DD} and V_{SS} pins are critical to system performance. An example demonstration board schematic is available at:

http://www.latticesemi.com

Power supply filtering is in the form of:

- A parallel bypass capacitor network consisting of 10 uf, 0.1 uf, and 1.0 uf caps close to the power source.
- A parallel bypass capacitor network consisting of 0.01 uf and 0.1 uf close to the pin on the ORT82G5.

Example connections are shown in Figure 29. The naming convention for the power supply sources shown in the figure are as follows:

- Supply_1.5 V—Tx-Rx digital, auxiliary power pins.
- Supply_V_{DD}RX—Rx analog power pins, guard band power pins.
- Supply V_{DD}TX—Tx analog power pins.
- Supply V_{DD}IB—Input Rx buffer power pins.
- Supply_V_{DD}OB—Output Tx buffer power pins.

Pin Information (continued)

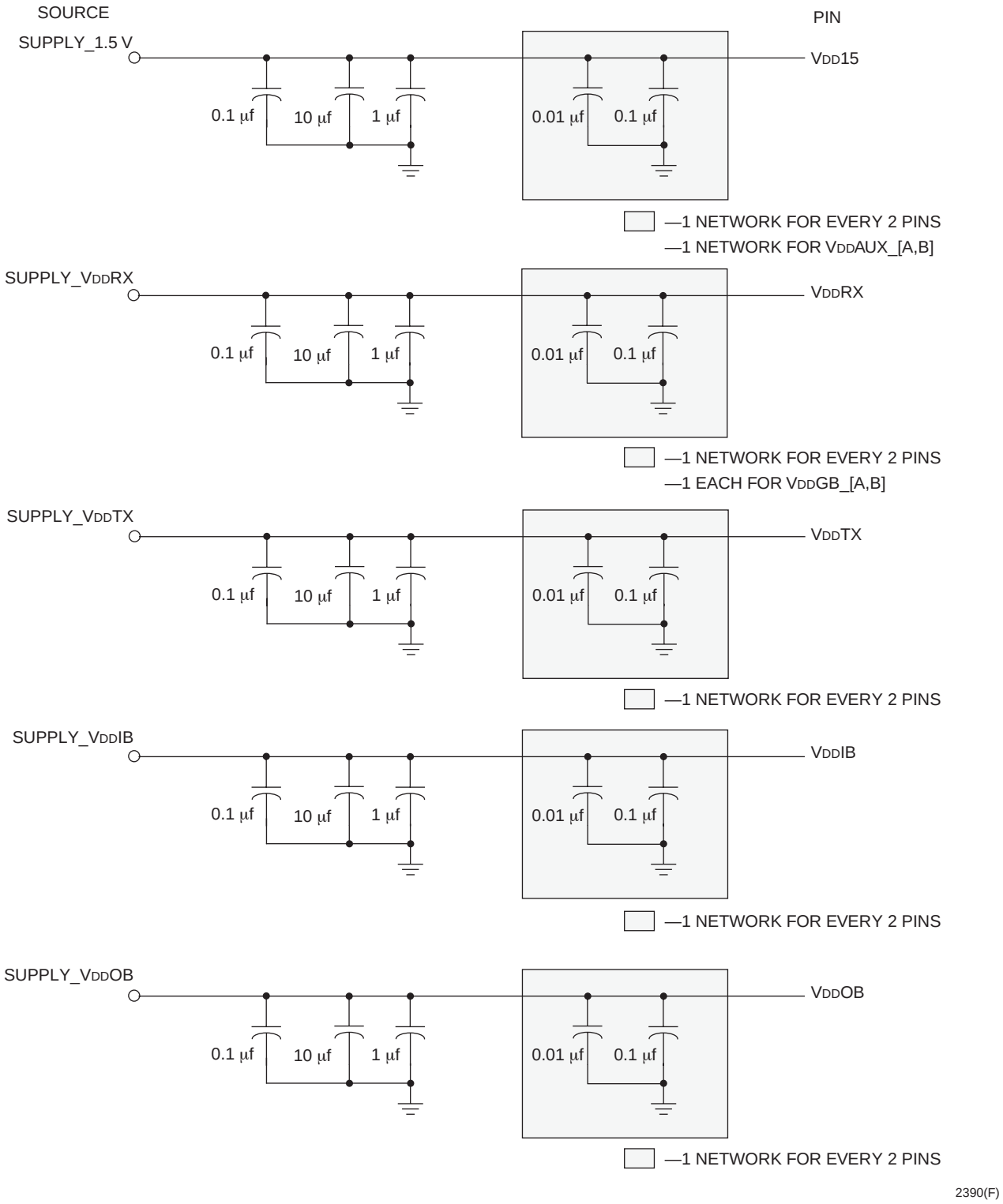


Figure 29. Power Supply Filtering

Pin Information (continued)

In Table 32, an input refers to a signal flowing into the embedded core and an output refers to a signal flowing out of the embedded core.

Table 32. Embedded Core/FPGA Interface Signal Description

Pin Name	I/O	Description
Memory Block Interface Signals		
AR_A[10:0]	I	Read address—memory block A.
AR_B[10:0]	I	Read address—memory block B.
AW_A[10:0]	I	Write address—memory block A.
AW_B[10:0]	I	Write address—memory block B.
BYTEWN_A[3:0]	I	Write control pins for byte-at-a-time write-memory block A.
BYTEWN_B[3:0]	I	Write control pins for byte-at-a-time write-memory block B.
CKR_A	I	Read clock—memory block A.
CKR_B	I	Read clock—memory block B.
CKW_A	I	Write clock—memory block A.
CKW_B	I	Write clock—memory block A.
CSR_A	I	Read chip select—memory block A.
CSR_B	I	Read chip select—memory block B.
CSWA_A	I	Write chip select A—memory block A.
CSWA_B	I	Write chip select A—memory block B.
CSWB_A	I	Write chip select B—memory block A.
CSWB_B	I	Write chip select B—memory block B.
D_A[35:0]	I	Data in—memory block A
D_B[35:0]	I	Data in—memory block B.
Q_A[35:0]	O	Data out—memory block A.
Q_B[35:0]	O	Data out—memory block B.

Pin Information (continued)

Table 32. Embedded Core/FPGA Interface Signal Description (continued)

Pin Name	I/O	Description
Transmit Path Signals		
TWDAA[31:0]	I	Transmit data—SERDES A, channel A.
TWDAB[31:0]	I	Transmit data—SERDES A, channel B.
TWDAC[31:0]	I	Transmit data—SERDES A, channel C.
TWDAD[31:0]	I	Transmit data—SERDES A, channel D.
TWDBA[31:0]	I	Transmit data—SERDES B, channel A.
TWDBB[31:0]	I	Transmit data—SERDES B, channel B.
TWDBC[31:0]	I	Transmit data—SERDES B, channel C.
TWDBD[31:0]	I	Transmit data—SERDES B, channel D.
TCOMMAAA[3:0]	I	Transmit comma character—SERDES A, channel A.
TCOMMAAB[3:0]	I	Transmit comma character—SERDES A, channel B.
TCOMMAAC[3:0]	I	Transmit comma character—SERDES A, channel C.
TCOMMAAD[3:0]	I	Transmit comma character—SERDES A, channel D.
TCOMMABA[3:0]	I	Transmit comma character—SERDES B, channel A.
TCOMMABB[3:0]	I	Transmit comma character—SERDES B, channel B.
TCOMMABC[3:0]	I	Transmit comma character—SERDES B, channel C.
TCOMMABD[3:0]	I	Transmit comma character—SERDES B, channel D.
TCK78A	O	Transmit low-speed clock to FPGA—SERDES A.
TCK78B	O	Transmit low-speed clock to FPGA—SERDES B.
TSYS_CLK_AA	I	Low-speed transmit FIFO clock Channel AA
TSYS_CLK_AB	I	Low-speed transmit FIFO clock Channel AB
TSYS_CLK_AC	I	Low-speed transmit FIFO clock Channel AC
TSYS_CLK_AD	I	Low-speed transmit FIFO clock Channel AD
TSYS_CLK_BA	I	Low-speed transmit FIFO clock Channel BA
TSYS_CLK_BB	I	Low-speed transmit FIFO clock Channel BB
TSYS_CLK_BC	I	Low-speed transmit FIFO clock Channel BC
TSYS_CLK_BD	I	Low-speed transmit FIFO clock Channel BD

Pin Information (continued)

Table 32. Embedded Core/FPGA Interface Signal Description (continued)

Pin Name	I/O	Description
Receive Path Signals		
MRWDAA[39:0]	O	Receive data—SERDES A, channel A.
MRWDAB[39:0]	O	Receive data—SERDES A, channel B.
MRWDAC[39:0]	O	Receive data—SERDES A, channel C.
MRWDAD[39:0]	O	Receive data—SERDES A, channel D.
MRWDBA[39:0]	O	Receive data—SERDES B, channel A.
MRWDBB[39:0]	O	Receive data—SERDES B, channel B.
MRWDBC[39:0]	O	Receive data—SERDES B, channel C.
MRWDBD[39:0]	O	Receive data—SERDES B, channel D.
RWCKAA	O	Low-speed receive clock—SERDES A, channel A.
RWCKAB	O	Low-speed receive clock—SERDES A, channel B.
RWCKAC	O	Low-speed receive clock—SERDES A, channel C.
RWCKAD	O	Low-speed receive clock—SERDES A, channel D.
RWCKBA	O	Low-speed receive clock—SERDES B, channel A.
RWCKBB	O	Low-speed receive clock—SERDES B, channel B.
RWCKBC	O	Low-speed receive clock—SERDES B, channel C.
RWCKBD	O	Low-speed receive clock—SERDES B, channel D.
RCK78A	O	Receive low-speed clock to FPGA—SERDES A.
RCK78B	O	Receive low-speed clock to FPGA—SERDES B.
RSYS_CLK_A1	I	Low-speed receive FIFO clock for channels AA, AB—SERDES A.
RSYS_CLK_A2	I	Low-speed receive FIFO clock for channels AC, AD—SERDES A.
RSYS_CLK_B1	I	Low-speed receive FIFO clock for channels BA, BB—SERDES B.
RSYS_CLK_B2	I	Low-speed receive FIFO clock for channels BC, BD—SERDES B
SYS_RST_N	I	Synchronous reset of the channel alignment blocks.

Pin Information (continued)

Package Pinouts

Table 33 provides the package pin and pin function for the ORT82G5 FPSC and packages. The bond pad name is identified in the PIO nomenclature used in the *ORCA* Foundry design editor. The Bank column provides information as to which output voltage level bank the given pin is in. The Group column provides information as to the group of pins the given pin is in. This is used to show which VREF pin is used to provide the reference voltage for single-ended limited-swing I/Os. If none of these buffer types (such as SSTL, GTL, HSTL) are used in a given group, then the VREF pin is available as an I/O pin.

When the number of FPGA bond pads exceeds the number of package pins, bond pads are unused. When the number of package pins exceeds the number of bond pads, package pins are left unconnected (no connects). When a package pin is to be left as a no connect for a specific die, it is indicated as a note in the device column for the FPGA. The tables provide no information on unused pads.

As shown in the pair columns in Table 33, differential pairs and physical locations are numbered within each bank (e.g., L19C-A0 is the nineteenth pair in an associated bank). A C indicates complementary differential, whereas a T indicates true differential. An _A0 indicates the physical location of adjacent balls in either the horizontal or vertical direction. Other physical indicators are as follows:

- _A1 indicates one ball between pairs.
- _A2 indicates two balls between pairs.
- _D0 indicates balls are diagonally adjacent.
- _D1 indicates balls are diagonally adjacent, separated by one physical ball.

V_{REF} pins, shown in the Pin Description column in Table 33, are associated to the bank and group (e.g., VREF_TL_01 is the V_{REF} for group one of the top left (TL) bank.

Pin Information (continued)

Table 33. ORT82G5 680-Pin PBGAM Pinout

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
AB20	—	—	VSS	VSS	—	—
C3	—	—	VDD33	VDD33	—	—
E4	—	—	O	PRD_DATA	RD_DATA/TDO	—
F5	—	—	I	PRESET_N	RESET_N	—
G5	—	—	I	PRD_CFG_N	RD_CFG_N	—
D3	—	—	I	PPRGRM_N	PRGRM_N	—
A2	0 (TL)	—	VDDIO0	VDDIO0	—	—
F4	0 (TL)	7	IO	PL2D	PLL_CK0C/HPPLL	L21C_A0
G4	0 (TL)	7	IO	PL2C	PLL_CK0T/HPPLL	L21T_A0
B3	0 (TL)	—	VDDIO0	VDDIO0	—	—
C2	0 (TL)	7	IO	PL3D	—	L22C_D0
B1	0 (TL)	7	IO	PL3C	VREF_0_07	L22T_D0
A1	—	—	VSS	VSS	—	—
J5	0 (TL)	7	IO	PL4D	D5	L23C_A0
H5	0 (TL)	7	IO	PL4C	D6	L23T_A0
B7	0 (TL)	—	VDDIO0	VDDIO0	—	—
E3	0 (TL)	8	IO	PL4B	—	L24C_A0
F3	0 (TL)	8	IO	PL4A	VREF_0_08	L24T_A0
C1	0 (TL)	8	IO	PL5D	HDC	L25C_D0
D2	0 (TL)	8	IO	PL5C	LDC_N	L25T_D0
A34	—	—	VSS	VSS	—	—
G3	0 (TL)	8	IO	PL5B	—	L26C_D0
H4	0 (TL)	8	IO	PL5A	—	L26T_D0
E2	0 (TL)	9	IO	PL6D	TESTCFG	L27C_D0
D1	0 (TL)	9	IO	PL6C	D7	L27T_D0
C5	0 (TL)	—	VDDIO0	VDDIO0	—	—
F2	0 (TL)	9	IO	PL7D	VREF_0_09	L28C_D0
E1	0 (TL)	9	IO	PL7C	A17/PPC_A31	L28T_D0
AA13	—	—	VSS	VSS	—	—
J4	0 (TL)	9	IO	PL7B	—	L29C_D0
K5	0 (TL)	9	IO	PL7A	—	L29T_D0
H3	0 (TL)	9	IO	PL8D	CS0_N	L30C_D0
G2	0 (TL)	9	IO	PL8C	CS1	L30T_D0
C9	0 (TL)	—	VDDIO0	VDDIO0	—	—
L5	0 (TL)	9	IO	PL8B	—	L31C_D0
K4	0 (TL)	9	IO	PL8A	—	L31T_D0
H2	0 (TL)	10	IO	PL9D	—	L32C_D0
J3	0 (TL)	10	IO	PL9C	—	L32T_D0
AA14	—	—	VSS	VSS	—	—
M5	0 (TL)	10	IO	PL9B	—	—
F1	0 (TL)	10	IO	PL10D	INIT_N	L33C_A0
G1	0 (TL)	10	IO	PL10C	DOUT	L33T_A0

Pin Information (continued)

Table 33. ORT82G5 680-Pin PBGAM Pinout (continued)

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
K3	0 (TL)	10	IO	PL11D	VREF_0_10	L34C_D0
J2	0 (TL)	10	IO	PL11C	A16/PPC_A30	L34T_D0
AA15	—	—	VSS	VSS	—	—
L4	0 (TL)	10	IO	PL11B	—	—
N5	7 (CL)	1	IO	PL12D	A15/PPC_A29	L1C_D0
M4	7 (CL)	1	IO	PL12C	A14/PPC_A28	L1T_D0
AA3	7 (CL)	—	VDDIO7	VDDIO7	—	—
L3	7 (CL)	1	IO	PL12B	—	L2C_D0
K2	7 (CL)	1	IO	PL12A	—	L2T_D0
H1	7 (CL)	1	IO	PL13D	VREF_7_01	L3C_A0
J1	7 (CL)	1	IO	PL13C	D4	L3T_A0
V18	—	—	VSS	VSS	—	—
N4	7 (CL)	2	IO	PL13B	—	L4C_D0
P5	7 (CL)	2	IO	PL13A	—	L4T_D0
M3	7 (CL)	2	IO	PL14D	RDY/BUSY_N/RCLK	L5C_D0
L2	7 (CL)	2	IO	PL14C	VREF_7_02	L5T_D0
AC2	7 (CL)	—	VDDIO7	VDDIO7	—	—
K1	7 (CL)	2	IO	PL14B	—	L6C_A0
L1	7 (CL)	2	IO	PL14A	—	L6T_A0
P4	7 (CL)	2	IO	PL15D	A13/PPC_A27	L7C_A0
P3	7 (CL)	2	IO	PL15C	A12/PPC_A26	L7T_A0
V19	—	—	VSS	VSS	—	—
M2	7 (CL)	2	IO	PL15B	—	L8C_A0
M1	7 (CL)	2	IO	PL15A	—	L8T_A0
N2	7 (CL)	3	IO	PL16D	—	L9C_A0
N1	7 (CL)	3	IO	PL16C	—	L9T_A0
N3	7 (CL)	—	VDDIO7	VDDIO7	—	—
R4	7 (CL)	3	IO	PL16B	—	—
P2	7 (CL)	3	IO	PL17D	A11/PPC_A25	L10C_D0
R3	7 (CL)	3	IO	PL17C	VREF_7_03	L10T_D0
W16	—	—	VSS	VSS	—	—
R5	7 (CL)	3	IO	PL17B	—	—
P1	7 (CL)	3	IO	PL18D	—	L11C_A0
R1	7 (CL)	3	IO	PL18C	—	L11T_A0
T5	7 (CL)	3	IO	PL18B	—	L12C_A0
T4	7 (CL)	3	IO	PL18A	—	L12T_A0
T3	7 (CL)	4	IO	PL19D	RD_N/MPI_STRB_N	L13C_A0
T2	7 (CL)	4	IO	PL19C	VREF_7_04	L13T_A0
W17	—	—	VSS	VSS	—	—
U1	7 (CL)	4	IO	PL19B	—	L14C_A0
T1	7 (CL)	4	IO	PL19A	—	L14T_A0
U4	7 (CL)	4	IO	PL20D	PLCK0C	L15C_A0

Pin Information (continued)

Table 33. ORT82G5 680-Pin PBGAM Pinout (continued)

BM680	$V_{DD}IO$ Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
U5	7 (CL)	4	IO	PL20C	PLCK0T	L15T_A0
R2	7 (CL)	—	$V_{DD}IO7$	$V_{DD}IO7$	—	—
U2	7 (CL)	4	IO	PL20B	—	L16C_D0
V1	7 (CL)	4	IO	PL20A	—	L16T_D0
W18	—	—	V_{SS}	V_{SS}	—	—
V2	7 (CL)	5	IO	PL21D	A10/PPC_A24	L17C_A0
V3	7 (CL)	5	IO	PL21C	A9/PPC_A23	L17T_A0
W19	—	—	V_{SS}	V_{SS}	—	—
V4	7 (CL)	5	IO	PL21B	—	L18C_A0
V5	7 (CL)	5	IO	PL21A	—	L18T_A0
W4	7 (CL)	5	IO	PL22D	A8/PPC_A22	L19C_A0
W3	7 (CL)	5	IO	PL22C	VREF_7_05	L19T_A0
W1	7 (CL)	5	IO	PL22B	—	L20C_A0
Y1	7 (CL)	5	IO	PL22A	—	L20T_A0
Y2	7 (CL)	5	IO	PL23D	—	L21C_D0
AA1	7 (CL)	5	IO	PL23C	—	L21T_D0
Y13	—	—	V_{SS}	V_{SS}	—	—
Y4	7 (CL)	5	IO	PL23B	—	L22C_A0
Y3	7 (CL)	5	IO	PL23A	—	L22T_A0
Y5	7 (CL)	6	IO	PL24D	PLCK1C	L23C_A0
W5	7 (CL)	6	IO	PL24C	PLCK1T	L23T_A0
U3	7 (CL)	—	$V_{DD}IO7$	$V_{DD}IO7$	—	—
AB1	7 (CL)	6	IO	PL24B	—	L24C_D0
AA2	7 (CL)	6	IO	PL24A	—	L24T_D0
AB2	7 (CL)	6	IO	PL25D	VREF_7_06	L25C_D0
AC1	7 (CL)	6	IO	PL25C	A7/PPC_A21	L25T_D0
Y14	—	—	V_{SS}	V_{SS}	—	—
AA4	7 (CL)	6	IO	PL25B	—	—
AB4	7 (CL)	6	IO	PL26D	A6/PPC_A20	L26C_A0
AB3	7 (CL)	6	IO	PL26C	A5/PPC_A19	L26T_A0
W2	7 (CL)	—	$V_{DD}IO7$	$V_{DD}IO7$	—	—
AD1	7 (CL)	7	IO	PL26B	—	—
AE1	7 (CL)	7	IO	PL27D	WR_N/MPI_RW	L27C_D0
AD2	7 (CL)	7	IO	PL27C	VREF_7_07	L27T_D0
AC3	7 (CL)	7	IO	PL27B	—	L28C_A0
AC4	7 (CL)	7	IO	PL27A	—	L28T_A0
AF1	7 (CL)	8	IO	PL28D	A4/PPC_A18	L29C_D0
AE2	7 (CL)	8	IO	PL28C	VREF_7_08	L29T_D0
AB5	7 (CL)	8	IO	PL29D	A3/PPC_A17	L30C_A0
AA5	7 (CL)	8	IO	PL29C	A2/PPC_A16	L30T_A0
Y15	—	—	V_{SS}	V_{SS}	—	—
AD3	7 (CL)	8	IO	PL29B	—	—

Pin Information (continued)

Table 33. ORT82G5 680-Pin PBGAM Pinout (continued)

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
AG1	7 (CL)	8	IO	PL30D	A1/PPC_A15	L31C_D0
AF2	7 (CL)	8	IO	PL30C	A0/PPC_A14	L31T_D0
AD4	7 (CL)	8	IO	PL30B	—	L32C_D0
AE3	7 (CL)	8	IO	PL30A	—	L32T_D0
AD5	7 (CL)	8	IO	PL31D	DP0	L33C_A0
AC5	7 (CL)	8	IO	PL31C	DP1	L33T_A0
Y20	—	—	VSS	VSS	—	—
AG2	7 (CL)	8	IO	PL31B	—	L34C_D0
AH1	7 (CL)	8	IO	PL31A	—	L34T_D0
AF3	6 (BL)	1	IO	PL32D	D8	L1C_A0
AG3	6 (BL)	1	IO	PL32C	VREF_6_01	L1T_A0
AL7	6 (BL)	—	VDDIO6	VDDIO6	—	—
AE4	6 (BL)	1	IO	PL32B	—	L2C_A0
AF4	6 (BL)	1	IO	PL32A	—	L2T_A0
AE5	6 (BL)	1	IO	PL33D	D9	L3C_A0
AF5	6 (BL)	1	IO	PL33C	D10	L3T_A0
R21	—	—	VSS	VSS	—	—
AJ1	6 (BL)	2	IO	PL34D	—	L4C_D0
AH2	6 (BL)	2	IO	PL34C	VREF_6_02	L4T_D0
AM5	6 (BL)	—	VDDIO6	VDDIO6	—	—
AK1	6 (BL)	2	IO	PL34B	—	L5C_D0
AJ2	6 (BL)	2	IO	PL34A	—	L5T_D0
R22	—	—	VSS	VSS	—	—
AG4	6 (BL)	3	IO	PL35B	D11	L6C_D0
AH3	6 (BL)	3	IO	PL35A	D12	L6T_D0
AL1	6 (BL)	3	IO	PL36D	—	L7C_D0
AK2	6 (BL)	3	IO	PL36C	—	L7T_D0
AM9	6 (BL)	—	VDDIO6	VDDIO6	—	—
AM1	6 (BL)	3	IO	PL36B	VREF_6_03	L8C_D0
AL2	6 (BL)	3	IO	PL36A	D13	L8T_D0
AJ3	6 (BL)	4	IO	PL37D	—	—
T16	—	—	VSS	VSS	—	—
AJ4	6 (BL)	4	IO	PL37B	—	L9C_A0
AH4	6 (BL)	4	IO	PL37A	VREF_6_04	L9T_A0
AK3	6 (BL)	4	IO	PL38C	—	—
AN2	6 (BL)	—	VDDIO6	VDDIO6	—	—
AG5	6 (BL)	4	IO	PL38B	—	L10C_A0
AH5	6 (BL)	4	IO	PL38A	—	L10T_A0
AN1	6 (BL)	4	IO	PL39D	PLL_CK7C/HPPLL	L11C_D0
AM2	6 (BL)	4	IO	PL39C	PLL_CK7T/HPPLL	L11T_D0
T17	—	—	VSS	VSS	—	—
AL3	6 (BL)	4	IO	PL39B	—	L12C_D0

Pin Information (continued)

Table 33. ORT82G5 680-Pin PBGAM Pinout (continued)

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
AK4	6 (BL)	4	IO	PL39A	—	L12T_D0
T18	—	—	VSS	VSS	—	—
AM3	—	—	I	PTEMP	PTEMP	—
AN3	6 (BL)	—	VDDIO6	VDDIO6	—	—
AJ5	—	—	IO	LVDS_R	LVDS_R	—
AL4	—	—	VDD33	VDD33	—	—
T19	—	—	VSS	VSS	—	—
AK5	—	—	VDD33	VDD33	—	—
AM4	6 (BL)	5	IO	PB2A	DP2	L13T_D0
AL5	6 (BL)	5	IO	PB2B	—	L13C_D0
AN7	6 (BL)	—	VDDIO6	VDDIO6	—	—
AP3	6 (BL)	5	IO	PB2C	PLL_CK6T/PPLL	L14T_A0
AP4	6 (BL)	5	IO	PB2D	PLL_CK6C/PPLL	L14C_A0
AN4	6 (BL)	5	IO	PB3B	—	—
U16	—	—	VSS	VSS	—	—
AK6	6 (BL)	5	IO	PB3C	—	L15T_A0
AK7	6 (BL)	5	IO	PB3D	—	L15C_A0
AL6	6 (BL)	5	IO	PB4A	VREF_6_05	L16T_A0
AM6	6 (BL)	5	IO	PB4B	DP3	L16C_A0
AP1	6 (BL)	—	VDDIO6	VDDIO6	—	—
AN5	6 (BL)	6	IO	PB4C	—	L17T_A0
AP5	6 (BL)	6	IO	PB4D	—	L17C_A0
AK8	6 (BL)	6	IO	PB5B	—	—
U17	—	—	VSS	VSS	—	—
AP6	6 (BL)	6	IO	PB5C	VREF_6_06	L18T_D0
AP7	6 (BL)	6	IO	PB5D	D14	L18C_D0
AM7	6 (BL)	6	IO	PB6A	—	L19T_D0
AN6	6 (BL)	6	IO	PB6B	—	L19C_D0
AP2	6 (BL)	—	VDDIO6	VDDIO6	—	—
AL8	6 (BL)	7	IO	PB6C	D15	L20T_A0
AL9	6 (BL)	7	IO	PB6D	D16	L20C_A0
AK9	6 (BL)	7	IO	PB7B	—	—
U18	—	—	VSS	VSS	—	—
AN8	6 (BL)	7	IO	PB7C	D17	L21T_A0
AM8	6 (BL)	7	IO	PB7D	D18	L21C_A0
AN9	6 (BL)	7	IO	PB8A	—	L22T_D0
AP8	6 (BL)	7	IO	PB8B	—	L22C_D0
AK10	6 (BL)	7	IO	PB8C	VREF_6_07	L23T_A0
AL10	6 (BL)	7	IO	PB8D	D19	L23C_A0
AP9	6 (BL)	8	IO	PB9B	—	—
U19	—	—	VSS	VSS	—	—
AM10	6 (BL)	8	IO	PB9C	D20	L24T_A0

Pin Information (continued)

Table 33. ORT82G5 680-Pin PBGAM Pinout (continued)

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
AM11	6 (BL)	8	IO	PB9D	D21	L24C_A0
AK11	6 (BL)	8	IO	PB10B	—	—
AN10	6 (BL)	8	IO	PB10C	VREF_6_08	L25T_A0
AP10	6 (BL)	8	IO	PB10D	D22	L25C_A0
AN11	6 (BL)	9	IO	PB11A	—	L26T_A0
AP11	6 (BL)	9	IO	PB11B	—	L26C_A0
V16	—	—	VSS	VSS	—	—
AL12	6 (BL)	9	IO	PB11C	D23	L27T_A0
AK12	6 (BL)	9	IO	PB11D	D24	L27C_A0
AN12	6 (BL)	9	IO	PB12A	—	L28T_A0
AM12	6 (BL)	9	IO	PB12B	—	L28C_A0
AP12	6 (BL)	9	IO	PB12C	VREF_6_09	L29T_A0
AP13	6 (BL)	9	IO	PB12D	D25	L29C_A0
AM13	6 (BL)	9	IO	PB13A	—	L30T_D0
AN14	6 (BL)	9	IO	PB13B	—	L30C_D0
V17	—	—	VSS	VSS	—	—
AP14	6 (BL)	10	IO	PB13C	D26	L31T_A0
AP15	6 (BL)	10	IO	PB13D	D27	L31C_A0
AK13	6 (BL)	10	IO	PB14A	—	L32T_A0
AK14	6 (BL)	10	IO	PB14B	—	L32C_A0
AM14	6 (BL)	10	IO	PB14C	VREF_6_10	L33T_A0
AL14	6 (BL)	10	IO	PB14D	D28	L33C_A0
AP17	6 (BL)	11	IO	PB15A	—	L34T_A0
AP16	6 (BL)	11	IO	PB15B	—	L34C_A0
AM15	6 (BL)	11	IO	PB15C	D29	L35T_D0
AN16	6 (BL)	11	IO	PB15D	D30	L35C_D0
AM17	6 (BL)	11	IO	PB16A	—	L36T_A0
AM16	6 (BL)	11	IO	PB16B	—	L36C_A0
AP18	6 (BL)	11	IO	PB16C	VREF_6_11	L37T_A0
AP19	6 (BL)	11	IO	PB16D	D31	L37C_A0
AL16	5 (BC)	1	IO	PB17A	—	L1T_D0
AK15	5 (BC)	1	IO	PB17B	—	L1C_D0
N22	—	—	VSS	VSS	—	—
AN18	5 (BC)	1	IO	PB17C	—	L2T_A0
AN19	5 (BC)	1	IO	PB17D	—	L2C_A0
AP20	5 (BC)	1	IO	PB18A	—	L3T_A0
AP21	5 (BC)	1	IO	PB18B	—	L3C_A0
AL17	5 (BC)	1	IO	PB18C	VREF_5_01	L4T_D0
AK16	5 (BC)	1	IO	PB18D	—	L4C_D0
P13	—	—	VSS	VSS	—	—
AM19	5 (BC)	2	IO	PB19A	—	L5T_A0
AM18	5 (BC)	2	IO	PB19B	—	L5C_A0

Pin Information (continued)

Table 33. ORT82G5 680-Pin PBGAM Pinout (continued)

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
P14	—	—	VSS	VSS	—	—
AN20	5 (BC)	2	IO	PB19C	PBCK0T	L6T_A0
AM20	5 (BC)	2	IO	PB19D	PBCK0C	L6C_A0
AK17	5 (BC)	2	IO	PB20A	—	L7T_D0
AL18	5 (BC)	2	IO	PB20B	—	L7C_D0
AL11	5 (BC)	—	VDDIO5	VDDIO5	—	—
AP22	5 (BC)	2	IO	PB20C	VREF_5_02	L8T_D0
AN21	5 (BC)	2	IO	PB20D	—	L8C_D0
AM22	5 (BC)	2	IO	PB21A	—	L9T_A0
AM21	5 (BC)	2	IO	PB21B	—	L9C_A0
AP23	5 (BC)	3	IO	PB21C	—	L10T_D0
AN22	5 (BC)	3	IO	PB21D	VREF_5_03	L10C_D0
AL19	5 (BC)	3	IO	PB22A	—	L11T_D0
AK18	5 (BC)	3	IO	PB22B	—	L11C_D0
P15	—	—	VSS	VSS	—	—
AP24	5 (BC)	3	IO	PB22C	—	L12T_D0
AN23	5 (BC)	3	IO	PB22D	—	L12C_D0
AP25	5 (BC)	3	IO	PB23A	—	L13T_A0
AP26	5 (BC)	3	IO	PB23B	—	L13C_A0
AL13	5 (BC)	—	VDDIO5	VDDIO5	—	—
AL20	5 (BC)	3	IO	PB23C	PBCK1T	L14T_D0
AK19	5 (BC)	3	IO	PB23D	PBCK1C	L14C_D0
AK20	5 (BC)	3	IO	PB24A	—	L15T_D0
AL21	5 (BC)	3	IO	PB24B	—	L15C_D0
P20	—	—	VSS	VSS	—	—
AN24	5 (BC)	4	IO	PB24C	—	L16T_D0
AM23	5 (BC)	4	IO	PB24D	—	L16C_D0
AN26	5 (BC)	4	IO	PB25A	—	L17T_A0
AN25	5 (BC)	4	IO	PB25B	—	L17C_A0
AL15	5 (BC)	—	VDDIO5	VDDIO5	—	—
AK21	5 (BC)	4	IO	PB25C	—	L18T_D0
AL22	5 (BC)	4	IO	PB25D	VREF_5_04	L18C_D0
AM24	5 (BC)	4	IO	PB26A	—	L19T_D0
AL23	5 (BC)	4	IO	PB26B	—	L19C_D0
P21	—	—	VSS	VSS	—	—
AP27	5 (BC)	5	IO	PB26C	—	L20T_A0
AN27	5 (BC)	5	IO	PB26D	VREF_5_05	L20C_A0
AL24	5 (BC)	5	IO	PB27A	—	L21T_D0
AM25	5 (BC)	5	IO	PB27B	—	L21C_D0
AN13	5 (BC)	—	VDDIO5	VDDIO5	—	—
AP28	5 (BC)	5	IO	PB27C	—	L22T_A0
AP29	5 (BC)	5	IO	PB27D	—	L22C_A0

Pin Information (continued)

Table 33. ORT82G5 680-Pin PBGAM Pinout (continued)

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
AN29	5 (BC)	6	IO	PB28B	—	—
P22	—	—	VSS	VSS	—	—
AM27	5 (BC)	6	IO	PB28C	—	L23T_D0
AN28	5 (BC)	6	IO	PB28D	VREF_5_06	L23C_D0
AM26	5 (BC)	6	IO	PB29B	—	—
AK22	5 (BC)	6	IO	PB29C	—	L24T_A0
AK23	5 (BC)	6	IO	PB29D	—	L24C_A0
AL25	5 (BC)	7	IO	PB30B	—	—
R13	—	—	VSS	VSS	—	—
AP30	5 (BC)	7	IO	PB30C	—	L25T_A0
AP31	5 (BC)	7	IO	PB30D	—	L25C_A0
AK24	5 (BC)	7	IO	PB31B	—	—
AN15	5 (BC)	—	VDDIO5	VDDIO5	—	—
AM29	5 (BC)	7	IO	PB31C	VREF_5_07	L26T_A0
AM28	5 (BC)	7	IO	PB31D	—	L26C_A0
AN30	5 (BC)	7	IO	PB32B	—	—
R14	—	—	VSS	VSS	—	—
AK25	5 (BC)	7	IO	PB32C	—	L27T_D0
AL26	5 (BC)	7	IO	PB32D	—	L27C_D0
AN17	5 (BC)	—	VDDIO5	VDDIO5	—	—
AL27	5 (BC)	8	IO	PB33C	—	L28T_A0
AL28	5 (BC)	8	IO	PB33D	VREF_5_08	L28C_A0
AN31	5 (BC)	8	IO	PB34B	—	—
R15	—	—	VSS	VSS	—	—
AK26	5 (BC)	8	IO	PB34D	—	—
AM30	5 (BC)	9	IO	PB35B	—	—
AL29	5 (BC)	9	IO	PB35D	VREF_5_09	—
AK27	5 (BC)	9	IO	PB36B	—	—
R20	—	—	VSS	VSS	—	—
AL30	5 (BC)	9	IO	PB36C	—	L29T_D0
AK29	5 (BC)	9	IO	PB36D	—	L29C_D0
AK28	—	—	VDD33	VDD33	—	—
AA16	—	—	VDD15	VDD15	—	—
AP32	—	—	IO	PSCHAR_LDIO9	—	—
AP33	—	—	IO	PSCHAR_LDIO8	—	—
AN32	—	—	IO	PSCHAR_LDIO7	—	—
AM31	—	—	IO	PSCHAR_LDIO6	—	—
AA17	—	—	VDD15	VDD15	—	—
AM32	—	—	VDD33	VDD33	—	—
AL31	—	—	IO	PSCHAR_LDIO5	—	—
AM33	—	—	IO	PSCHAR_LDIO4	—	—
AA18	—	—	VDD15	VDD15	—	—

Pin Information (continued)

Table 33. ORT82G5 680-Pin PBGAM Pinout (continued)

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
AK30	—	—	IO	PSCHAR_LDIO3	—	—
AL32	—	—	IO	PSCHAR_LDIO2	—	—
AA19	—	—	VDD15	VDD15	—	—
AB16	—	—	VDD15	VDD15	—	—
AK31	—	—	VDD33	VDD33	—	—
AJ30	—	—	IO	PSCHAR_LDIO1	—	—
AK33	—	—	IO	PSCHAR_LDIO0	—	—
AK34	—	—	IO	PSCHAR_CKIO1	—	—
AJ31	—	—	IO	PSCHAR_CKIO0	—	—
AJ33	—	—	IO	PSCHAR_XCK	—	—
AJ34	—	—	IO	PSCHAR_WDSYNC	—	—
AH30	—	—	IO	PSCHAR_CV	—	—
AH31	—	—	IO	PSCHAR_BYTSYNC	—	—
AH32	—	—	I	ATMOUT_B	—	—
AH33	—	—	VSSGB_B	VSSGB_B	—	—
AH34	—	—	VDDGB_B	VDDGB_B	—	—
AA32	—	—	VDDR	VDDAUX_B	—	—
AF30	—	—	O	REXT_B	—	—
AF31	—	—	O	REXTN_B	—	—
AE30	—	—	I	REFCLKN_B	—	—
AE31	—	—	I	REFCLKP_B	—	—
AB32	—	—	VSST	VSSAUX_B	—	—
AD30	—	—	VDDIB	VDDIB_BA	—	—
AD32	—	—	VDDR	VDDRX_BA	—	—
AF33	—	—	I	HDINN_BA	—	—
AC32	—	—	VSST	VSSIB_BA	—	—
AF34	—	—	I	HDINP_BA	—	—
AE32	—	—	VDDR	VDDRX_BA	—	—
AD31	—	—	VSSRX	VSSRX_BA	—	—
K32	—	—	VDDR	VDDTX_BA	—	—
AC30	—	—	VDDOB	VDDOB_BA	—	—
AE33	—	—	O	HDOUTN_BA	—	—
AF32	—	—	VSST	VSSOB_BA	—	—
AE34	—	—	O	HDOUTP_BA	—	—
AC30	—	—	VDDOB	VDDOB_BA	—	—
AG30	—	—	VSST	VSSTX_BA	—	—
AB30	—	—	VDDIB	VDDIB_BB	—	—
AD33	—	—	I	HDINN_BB	—	—
AG31	—	—	VSST	VSSIB_BB	—	—
AD34	—	—	I	HDINP_BB	—	—
AC31	—	—	VSSRX	VSSRX_BB	—	—
AB31	—	—	VDDOB	VDDOB_BB	—	—

Pin Information (continued)

Table 33. ORT82G5 680-Pin PBGAM Pinout (continued)

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
AC33	—	—	O	HDOUTN_BB	—	—
AG32	—	—	VSST	VSSOB_BB	—	—
AC34	—	—	O	HDOUTP_BB	—	—
AB31	—	—	VDDOB	VDDOB_BB	—	—
AG33	—	—	VSST	VSSTX_BB	—	—
AA30	—	—	VDDIB	VDDIB_BC	—	—
AB33	—	—	I	HDINN_BC	—	—
AG34	—	—	VSST	VSSIB_BC	—	—
AB34	—	—	I	HDINP_BC	—	—
AA31	—	—	VSSRX	VSSRX_BC	—	—
Y30	—	—	VDDOB	VDDOB_BC	—	—
AA33	—	—	O	HDOUTN_BC	—	—
H30	—	—	VSST	VSSOB_BC	—	—
AA34	—	—	O	HDOUTP_BC	—	—
Y31	—	—	VDDOB	VDDOB_BC	—	—
H31	—	—	VSST	VSSTX_BC	—	—
W30	—	—	VDDIB	VDDIB_BD	—	—
Y33	—	—	I	HDINN_BD	—	—
H32	—	—	VSST	VSSIB_BD	—	—
Y34	—	—	I	HDINP_BD	—	—
W31	—	—	VSSRX	VSSRX_BD	—	—
V30	—	—	VDDOB	VDDOB_BD	—	—
W33	—	—	O	HDOUTN_BD	—	—
H33	—	—	VSST	VSSOB_BD	—	—
W34	—	—	O	HDOUTP_BD	—	—
V31	—	—	VDDOB	VDDOB_BD	—	—
H34	—	—	VSST	VSSTX_BD	—	—
J32	—	—	VSST	VSSTX_AD	—	—
U31	—	—	VDDOB	VDDOB_AD	—	—
T34	—	—	O	HDOUTP_AD	—	—
M32	—	—	VSST	VSSOB_AD	—	—
T33	—	—	O	HDOUTN_AD	—	—
U30	—	—	VDDOB	VDDOB_AD	—	—
T31	—	—	VSSRX	VSSRX_AD	—	—
R34	—	—	I	HDINP_AD	—	—
N32	—	—	VSST	VSSIB_AD	—	—
R33	—	—	I	HDINN_AD	—	—
T30	—	—	VDDIB	VDDIB_AD	—	—
U32	—	—	VSST	VSSTX_AC	—	—
R31	—	—	VDDOB	VDDOB_AC	—	—
P34	—	—	O	HDOUTP_AC	—	—
U33	—	—	VSST	VSSOB_AC	—	—

Pin Information (continued)

Table 33. ORT82G5 680-Pin PBGAM Pinout (continued)

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
P33	—	—	O	HDOUTN_AC	—	—
R30	—	—	VDDOB	VDDOB_AC	—	—
P31	—	—	VSSRX	VSSRX_AC	—	—
N34	—	—	I	HDINP_AC	—	—
U34	—	—	VSST	VSSIB_AC	—	—
N33	—	—	I	HDINN_AC	—	—
P30	—	—	VDDIB	VDDIB_AC	—	—
V32	—	—	VSST	VSSTX_AB	—	—
N31	—	—	VDDOB	VDDOB_AB	—	—
M34	—	—	O	HDOUTP_AB	—	—
V33	—	—	VSST	VSSOB_AB	—	—
M33	—	—	O	HDOUTN_AB	—	—
N31	—	—	VDDOB	VDDOB_AB	—	—
M31	—	—	VSSRX	VSSRX_AB	—	—
L34	—	—	I	HDINP_AB	—	—
V34	—	—	VSST	VSSIB_AB	—	—
L33	—	—	I	HDINN_AB	—	—
N30	—	—	VDDIB	VDDIB_AB	—	—
M30	—	—	VDDOB	VDDOB_AA	—	—
K34	—	—	O	HDOUTP_AA	—	—
K33	—	—	O	HDOUTN_AA	—	—
M30	—	—	VDDOB	VDDOB_AA	—	—
L32	—	—	VDDR	VDDTX_AA	—	—
L31	—	—	VSSRX	VSSRX_AA	—	—
P32	—	—	VDDR	VDDRX_AA	—	—
J34	—	—	I	HDINP_AA	—	—
J33	—	—	I	HDINN_AA	—	—
R32	—	—	VDDR	VDDRX_AA	—	—
L30	—	—	VDDIB	VDDIB_AA	—	—
K31	—	—	I	REFCLKP_A	—	—
K30	—	—	I	REFCLKN_A	—	—
J31	—	—	O	REXTN_A	—	—
J30	—	—	O	REXT_A	—	—
Y32	—	—	VDDR	VDDAUX_A	—	—
G34	—	—	VDDGB_A	VDDGB_A	—	—
G33	—	—	VSSGB_A	VSSGB_A	—	—
G32	—	—	I	ATMOUT_A	—	—
G31	—	—	I	PRESERVE01	—	—
F33	—	—	I	PRESERVE02	—	—
G30	—	—	I	PRESERVE03	—	—
F31	—	—	O	PSYS_RSSIG_ALL	—	—
F30	—	—	I	PSYS_DOBISTN	—	—

Pin Information (continued)

Table 33. ORT82G5 680-Pin PBGAM Pinout (continued)

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
E31	—	—	VDD33	VDD33	—	—
AB17	—	—	VDD15	VDD15	—	—
AB18	—	—	VDD15	VDD15	—	—
D32	—	—	I	PBIST_TEST_ENN	—	—
E30	—	—	I	PLOOP_TEST_ENN	—	—
AB19	—	—	VDD15	VDD15	—	—
D31	—	—	I	PASB_PDN	—	—
C32	—	—	I	PMP_TESTCLK	—	—
C31	—	—	VDD33	VDD33	—	—
AJ32	—	—	VDD15	VDD15	—	—
B32	—	—	I	PASB_RESETN	—	—
A33	—	—	I	PASB_TRISTN	—	—
B31	—	—	I	PMP_TESTCLK_ENN	—	—
A32	—	—	I	PASB_TESTCLK	—	—
AK32	—	—	VDD15	VDD15	—	—
AB21	—	—	VSS	VSS	—	—
A31	—	—	VDD33	VDD33	—	—
B30	1 (TC)	7	IO	PT36D	—	—
AB22	—	—	VSS	VSS	—	—
C30	1 (TC)	7	IO	PT36B	—	—
D30	1 (TC)	7	IO	PT35D	—	—
B13	1 (TC)	—	VDDIO1	VDDIO1	—	—
E29	1 (TC)	7	IO	PT35B	—	—
E28	1 (TC)	7	IO	PT34D	VREF_1_07	—
AN33	—	—	VSS	Vss	—	—
D29	1 (TC)	8	IO	PT34B	—	—
B29	1 (TC)	8	IO	PT33D	—	L1C_A0
C29	1 (TC)	8	IO	PT33C	VREF_1_08	L1T_A0
B15	1 (TC)	—	VDDIO1	VDDIO1	—	—
E27	1 (TC)	8	IO	PT32D	—	L2C_A0
E26	1 (TC)	8	IO	PT32C	—	L2T_A0
AP34	—	—	Vss	Vss	—	—
A30	1 (TC)	8	IO	PT32B	—	—
A29	1 (TC)	9	IO	PT31D	—	L3C_D3
E25	1 (TC)	9	IO	PT31C	VREF_1_09	L3T_D3
B17	1 (TC)	—	VDDIO1	VDDIO1	—	—
E24	1 (TC)	9	IO	PT31A	—	—
B28	1 (TC)	9	IO	PT30D	—	L4C_A0
C28	1 (TC)	9	IO	PT30C	—	L4T_A0
B2	—	—	Vss	Vss	—	—
D28	1 (TC)	9	IO	PT30A	—	—
C27	1 (TC)	9	IO	PT29D	—	L5C_A0

Pin Information (continued)

Table 33. ORT82G5 680-Pin PBGAM Pinout (continued)

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
D27	1 (TC)	9	IO	PT29C	—	L5T_A0
E23	1 (TC)	9	IO	PT29B	—	L6C_A0
E22	1 (TC)	9	IO	PT29A	—	L6T_A0
D26	1 (TC)	1	IO	PT28D	—	L7C_A0
D25	1 (TC)	1	IO	PT28C	—	L7T_A0
B33	—	—	VSS	VSS	—	—
D24	1 (TC)	1	IO	PT28B	—	L8C_A0
D23	1 (TC)	1	IO	PT28A	—	L8T_A0
C26	1 (TC)	1	IO	PT27D	VREF_1_01	L9C_A0
C25	1 (TC)	1	IO	PT27C	—	L9T_A0
D11	1 (TC)	—	VDDIO1	VDDIO1	—	—
E21	1 (TC)	1	IO	PT27B	—	L10C_A0
E20	1 (TC)	1	IO	PT27A	—	L10T_A0
D22	1 (TC)	2	IO	PT26D	—	L11C_A0
D21	1 (TC)	2	IO	PT26C	VREF_1_02	L11T_A0
E34	—	—	VSS	VSS	—	—
A28	1 (TC)	2	IO	PT26B	—	—
B26	1 (TC)	2	IO	PT25D	—	L12C_A0
B25	1 (TC)	2	IO	PT25C	—	L12T_A0
D13	1 (TC)	—	VDDIO1	VDDIO1	—	—
B27	1 (TC)	2	IO	PT25B	—	—
A27	1 (TC)	3	IO	PT24D	—	L13C_A0
A26	1 (TC)	3	IO	PT24C	VREF_1_03	L13T_A0
N13	—	—	VSS	VSS	—	—
C24	1 (TC)	3	IO	PT24B	—	—
C22	1 (TC)	3	IO	PT23D	—	L14C_A0
C23	1 (TC)	3	IO	PT23C	—	L14T_A0
D15	1 (TC)	—	VDDIO1	VDDIO1	—	—
B24	1 (TC)	3	IO	PT23B	—	—
D20	1 (TC)	3	IO	PT22D	—	L15C_A0
D19	1 (TC)	3	IO	PT22C	—	L15T_A0
N14	—	—	VSS	VSS	—	—
E19	1 (TC)	3	IO	PT22B	—	L16C_A0
E18	1 (TC)	3	IO	PT22A	—	L16T_A0
C21	1 (TC)	4	IO	PT21D	—	L17C_A0
C20	1 (TC)	4	IO	PT21C	—	L17T_A0
A25	1 (TC)	4	IO	PT21B	—	L18C_A0
A24	1 (TC)	4	IO	PT21A	—	L18T_A0
B23	1 (TC)	4	IO	PT20D	—	L19C_A0
A23	1 (TC)	4	IO	PT20C	—	L19T_A0
N15	—	—	VSS	VSS	—	—
E17	1 (TC)	4	IO	PT20B	—	L20C_A0

Pin Information (continued)

Table 33. ORT82G5 680-Pin PBGAM Pinout (continued)

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
E16	1 (TC)	4	IO	PT20A	—	L20T_A0
B22	1 (TC)	4	IO	PT19D	—	L21C_A0
B21	1 (TC)	4	IO	PT19C	VREF_1_04	L21T_A0
C18	1 (TC)	4	IO	PT19B	—	L22C_A0
C19	1 (TC)	4	IO	PT19A	—	L22T_A0
N20	—	—	Vss	Vss	—	—
A22	1 (TC)	5	IO	PT18D	PTCK1C	L23C_A0
A21	1 (TC)	5	IO	PT18C	PTCK1T	L23T_A0
N21	—	—	Vss	Vss	—	—
D17	1 (TC)	5	IO	PT18B	—	L24C_A0
D18	1 (TC)	5	IO	PT18A	—	L24T_A0
B20	1 (TC)	5	IO	PT17D	PTCK0C	L25C_A0
B19	1 (TC)	5	IO	PT17C	PTCK0T	L25T_A0
A20	1 (TC)	5	IO	PT17B	—	L26C_A0
A19	1 (TC)	5	IO	PT17A	—	L26T_A0
A18	1 (TC)	5	IO	PT16D	VREF_1_05	L27C_A0
B18	1 (TC)	5	IO	PT16C	—	L27T_A0
Y21	—	—	Vss	Vss	—	—
C17	1 (TC)	5	IO	PT16B	—	L28C_D0
D16	1 (TC)	5	IO	PT16A	—	L28T_D0
A17	1 (TC)	6	IO	PT15D	—	L29C_D0
B16	1 (TC)	6	IO	PT15C	—	L29T_D0
E15	1 (TC)	6	IO	PT15B	—	L30C_A0
E14	1 (TC)	6	IO	PT15A	—	L30T_A0
A16	1 (TC)	6	IO	PT14D	—	L31C_A0
A15	1 (TC)	6	IO	PT14C	VREF_1_06	L31T_A0
Y22	—	—	Vss	Vss	—	—
D14	1 (TC)	6	IO	PT14B	—	—
C16	0 (TL)	1	IO	PT13D	MPI_RTRY_N	L1C_A0
C15	0 (TL)	1	IO	PT13C	MPI_ACK_N	L1T_A0
D7	0 (TL)	—	VDDIO0	VDDIO0	—	—
C14	0 (TL)	1	IO	PT13B	—	L2C_A0
B14	0 (TL)	1	IO	PT13A	VREF_0_01	L2T_A0
A14	0 (TL)	1	IO	PT12D	M0	L3C_A0
A13	0 (TL)	1	IO	PT12C	M1	L3T_A0
AA20	—	—	Vss	Vss	—	—
E12	0 (TL)	2	IO	PT12B	MPI_CLK	L4C_A0
E13	0 (TL)	2	IO	PT12A	A21/MPI_BURST_N	L4T_A0
C13	0 (TL)	2	IO	PT11D	M2	L5C_A0
C12	0 (TL)	2	IO	PT11C	M3	L5T_A0
B12	0 (TL)	2	IO	PT11B	VREF_0_02	L6C_A0
A12	0 (TL)	2	IO	PT11A	MPI_TEA_N	L6T_A0

Pin Information (continued)

Table 33. ORT82G5 680-Pin PBGAM Pinout (continued)

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
D12	0 (TL)	3	IO	PT10D	—	L7C_D0
C11	0 (TL)	3	IO	PT10C	—	L7T_D0
B11	0 (TL)	3	IO	PT10B	—	—
A11	0 (TL)	3	IO	PT9D	VREF_0_03	L8C_A0
A10	0 (TL)	3	IO	PT9C	—	L8T_A0
AA21	—	—	Vss	Vss	—	—
B10	0 (TL)	3	IO	PT9B	—	—
E11	0 (TL)	3	IO	PT8D	D0	L9C_D0
D10	0 (TL)	3	IO	PT8C	TMS	L9T_D0
C10	0 (TL)	3	IO	PT8B	—	—
A9	0 (TL)	4	IO	PT7D	A20/MPI_BDIP_N	L10C_A0
B9	0 (TL)	4	IO	PT7C	A19/MPI_TSZ1	L10T_A0
AA22	—	—	Vss	Vss	—	—
E10	0 (TL)	4	IO	PT7B	—	—
A8	0 (TL)	4	IO	PT6D	A18/MPI_TSZ0	L11C_A0
B8	0 (TL)	4	IO	PT6C	D3	L11T_A0
D9	0 (TL)	4	IO	PT6B	VREF_0_04	L12C_D0
C8	0 (TL)	4	IO	PT6A	—	L12T_D0
E9	0 (TL)	5	IO	PT5D	D1	L13C_D0
D8	0 (TL)	5	IO	PT5C	D2	L13T_D0
AB13	—	—	Vss	Vss	—	—
A7	0 (TL)	5	IO	PT5B	—	L14C_A0
A6	0 (TL)	5	IO	PT5A	VREF_0_05	L14T_A0
C7	0 (TL)	5	IO	PT4D	TDI	L15C_D0
B6	0 (TL)	5	IO	PT4C	TCK	L15T_D0
E8	0 (TL)	5	IO	PT4B	—	L16C_A0
E7	0 (TL)	5	IO	PT4A	—	L16T_A0
A5	0 (TL)	6	IO	PT3D	—	L17C_A0
B5	0 (TL)	6	IO	PT3C	VREF_0_06	L17T_A0
AB14	—	—	Vss	Vss	—	—
C6	0 (TL)	6	IO	PT3B	—	L18C_A0
D6	0 (TL)	6	IO	PT3A	—	L18T_A0
C4	0 (TL)	6	IO	PT2D	PLL_CK1C/PPLL	L19C_A0
B4	0 (TL)	6	IO	PT2C	PLL_CK1T/PPLL	L19T_A0
A4	0 (TL)	6	IO	PT2B	—	L20C_A0
A3	0 (TL)	6	IO	PT2A	—	L20T_A0
D5	—	—	O	PCFG_MPI_IRQ	CFG_IRQ_N/MPI_IRQ_N	—
E6	—	—	IO	PCCLK	CCLK	—
D4	—	—	IO	PDONE	DONE	—
E5	—	—	VDD33	VDD33	—	—
AB15	—	—	Vss	Vss	—	—
AL33	—	—	VDD15	VDD15	—	—

Pin Information (continued)

Table 33. ORT82G5 680-Pin PBGAM Pinout (continued)

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
AL34	—	—	VDD15	VDD15	—	—
AM34	—	—	VDD15	VDD15	—	—
AN34	—	—	VDD15	VDD15	—	—
B34	—	—	VDD15	VDD15	—	—
C33	—	—	VDD15	VDD15	—	—
C34	—	—	VDD15	VDD15	—	—
D33	—	—	VDD15	VDD15	—	—
D34	—	—	VDD15	VDD15	—	—
E32	—	—	VDD15	VDD15	—	—
E33	—	—	VDD15	VDD15	—	—
F32	—	—	VDD15	VDD15	—	—
F34	—	—	VDD15	VDD15	—	—
N16	—	—	VDD15	VDD15	—	—
N17	—	—	VDD15	VDD15	—	—
N18	—	—	VDD15	VDD15	—	—
N19	—	—	VDD15	VDD15	—	—
P16	—	—	VDD15	VDD15	—	—
P17	—	—	VDD15	VDD15	—	—
P18	—	—	VDD15	VDD15	—	—
P19	—	—	VDD15	VDD15	—	—
R16	—	—	VDD15	VDD15	—	—
R17	—	—	VDD15	VDD15	—	—
R18	—	—	VDD15	VDD15	—	—
R19	—	—	VDD15	VDD15	—	—
T13	—	—	VDD15	VDD15	—	—
T14	—	—	VDD15	VDD15	—	—
T15	—	—	VDD15	VDD15	—	—
T20	—	—	VDD15	VDD15	—	—
T21	—	—	VDD15	VDD15	—	—
T22	—	—	VDD15	VDD15	—	—
U13	—	—	VDD15	VDD15	—	—
U14	—	—	VDD15	VDD15	—	—
U15	—	—	VDD15	VDD15	—	—
U20	—	—	VDD15	VDD15	—	—
U21	—	—	VDD15	VDD15	—	—
U22	—	—	VDD15	VDD15	—	—
V13	—	—	VDD15	VDD15	—	—
V14	—	—	VDD15	VDD15	—	—
V15	—	—	VDD15	VDD15	—	—
V20	—	—	VDD15	VDD15	—	—
V21	—	—	VDD15	VDD15	—	—
V22	—	—	VDD15	VDD15	—	—

Pin Information (continued)

Table 33. ORT82G5 680-Pin PBGAM Pinout (continued)

BM680	$V_{DD}IO$ Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
W13	—	—	$V_{DD}15$	$V_{DD}15$	—	—
W14	—	—	$V_{DD}15$	$V_{DD}15$	—	—
W15	—	—	$V_{DD}15$	$V_{DD}15$	—	—
W20	—	—	$V_{DD}15$	$V_{DD}15$	—	—
W21	—	—	$V_{DD}15$	$V_{DD}15$	—	—
W22	—	—	$V_{DD}15$	$V_{DD}15$	—	—
Y16	—	—	$V_{DD}15$	$V_{DD}15$	—	—
Y17	—	—	$V_{DD}15$	$V_{DD}15$	—	—
Y18	—	—	$V_{DD}15$	$V_{DD}15$	—	—
Y19	—	—	$V_{DD}15$	$V_{DD}15$	—	—
T32	—	—	NC	NC	—	—
W32	—	—	NC	NC	—	—

Package Thermal Characteristics Summary

There are three thermal parameters that are in common use: ΘJA, ψJC, and ΘJC. It should be noted that all the parameters are affected, to varying degrees, by package design (including paddle size) and choice of materials, the amount of copper in the test board or system board, and system airflow.

ΘJA

This is the thermal resistance from junction to ambient (theta-JA, R-theta, etc.):

$$\Theta JA = \frac{TJ - TA}{Q}$$

where T_J is the junction temperature, T_A, is the ambient air temperature, and Q is the chip power.

Experimentally, ΘJA is determined when a special thermal test die is assembled into the package of interest, and the part is mounted on the thermal test board. The diodes on the test chip are separately calibrated in an oven. The package/board is placed either in a JEDEC natural convection box or in the wind tunnel, the latter for forced convection measurements. A controlled amount of power (Q) is dissipated in the test chip's heater resistor, the chip's temperature (T_J) is determined by the forward drop on the diodes, and the ambient temperature (T_A) is noted. Note that ΘJA is expressed in units of °C/W.

ψJC

This JEDEC designated parameter correlates the junction temperature to the case temperature. It is generally used to infer the junction temperature while the device is operating in the system. It is not considered a true thermal resistance and it is defined by:

$$\psi JC = \frac{TJ - TC}{Q}$$

where T_C is the case temperature at top dead center, T_J is the junction temperature, and Q is the chip power. During the ΘJA measurements described above, besides the other parameters measured, an additional temperature reading, T_C, is made with a thermocouple attached at top-dead-center of the case. ψJC is also expressed in units of °C/W.

ΘJC

This is the thermal resistance from junction to case. It is most often used when attaching a heat sink to the top of the package. It is defined by:

$$\Theta JC = \frac{TJ - TC}{Q}$$

The parameters in this equation have been defined above. However, the measurements are performed with the case of the part pressed against a water-cooled heat sink to draw most of the heat generated by the chip out the top of the package. It is this difference in the measurement process that differentiates ΘJC from ψJC. ΘJC is a true thermal resistance and is expressed in units of °C/W.

ΘJB

This is the thermal resistance from junction to board (ΘJL). It is defined by:

$$\Theta JB = \frac{TJ - TB}{Q}$$

where T_B is the temperature of the board adjacent to a lead measured with a thermocouple. The other parameters on the right-hand side have been defined above. This is considered a true thermal resistance, and the measurement is made with a water-cooled heat sink pressed against the board to draw most of the heat out of the leads. Note that ΘJB is expressed in units of °C/W and that this parameter and the way it is measured are still in JEDEC committee.

FPSC Maximum Junction Temperature

Once the power dissipated by the FPSC has been determined (see the Estimating Power Dissipation section), the maximum junction temperature of the FPSC can be found. This is needed to determine if speed derating of the device from the 85 °C junction temperature used in all of the delay tables is needed. Using the maximum ambient temperature, T_{Amax}, and the power dissipated by the device, Q (expressed in °C), the maximum junction temperature is approximated by:

$$T_{Jmax} = T_{Amax} + (Q \bullet \Theta JA)$$

Table 34 lists the thermal characteristics for all packages used with the *ORCA* ORT82G5 Series of FPSCs.

Package Thermal Characteristics

Table 34*. ORCA* ORT82G5 Plastic Package Thermal Guidelines

Package	ΘJA (°C/W)			T = 85°C Max TJ = 125 °C Max 0 fpm (W)
	0 fpm	200 fpm	500 fpm	
680-Pin PBGAM	9.8	7.8	6.8	4.1

Note: The 680-pin PBGAM package for the ORT82G5 includes a heat spreader.

Package Coplanarity

The coplanarity limits of packages are as follows:

- PBGAM: 8.0 mils

Heat Sink Vendors for BGA Packages

In some cases the power required by the customers application is greater than the package can dissipate. Below, in alphabetical order, is a list of heat sink vendors who advertise heat sinks aimed at the BGA market.

Table 35. Heat Sink Vendors

Vendor	Location	Phone
Aavid Thermalloy	Concord, NH	(603) 224-9988
Chip Coolers (Tyco Electronics)	Harrisburg, PA	(800) 468-2023
IERC (CTS Corp.)	Burbank, CA	(818) 842-7277
R-Theta	Buffalo, NY	(800) 388-5428
Sanyo Denki	Torrance, CA	(310) 783-5400
Wakefield Thermal Solutions	Pelham, NH	(603) 635-2800

Package Parasitics

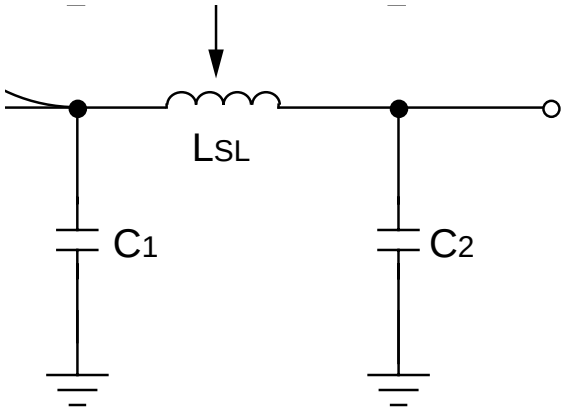
The electrical performance of an IC package, such as signal quality and noise sensitivity, is directly affected by the package parasitics. Table 36 lists eight parasitics associated with the *ORCA* packages. These parasitics represent the contributions of all components of a package, which include the bond wires, all internal package routing, and the external leads.

Four inductances in nH are listed: L_{SW} and L_{SL}, the self-inductance of the lead; and L_{MW} and L_{ML}, the mutual inductance to the nearest neighbor lead. These parameters are important in determining ground bounce noise and inductive crosstalk noise. Three capacitances in pF are listed: C_M, the mutual capacitance of the lead to the nearest neighbor lead; and C_1 and C_2, the total capacitance of the lead to all other leads (all other leads are assumed to be grounded). These parameters are important in determining capacitive crosstalk and the capacitive loading effect of the lead. Resistance values are in mΩ.

The parasitic values in Table 36 are for the circuit model of bond wire and package lead parasitics. If the mutual capacitance value is not used in the designer's model, then the value listed as mutual capacitance should be added to each of the C_1 and C_2 capacitors.

Table 36. *ORCA* ORT82G5 Package Parasitics

Package Type	L_{SW}	L_{MW}	R_W	C_1	C_2	C_M	L_{SL}	L_{ML}
680-Pin PBGAM	3.8	1.3	250	1.0	1.0	0.3	2.8—5	0.5—1



5-3862(C)r2

Figure 30. Package Parasitics

Package Outline Diagrams

Terms and Definitions

Basic Size (BSC): The basic size of a dimension is the size from which the limits for that dimension are derived by the application of the allowance and the tolerance.

Design Size: The design size of a dimension is the actual size of the design, including an allowance for fit and tolerance.

Typical (TYP): When specified after a dimension, this indicates the repeated design size if a tolerance is specified or repeated basic size if a tolerance is not specified.

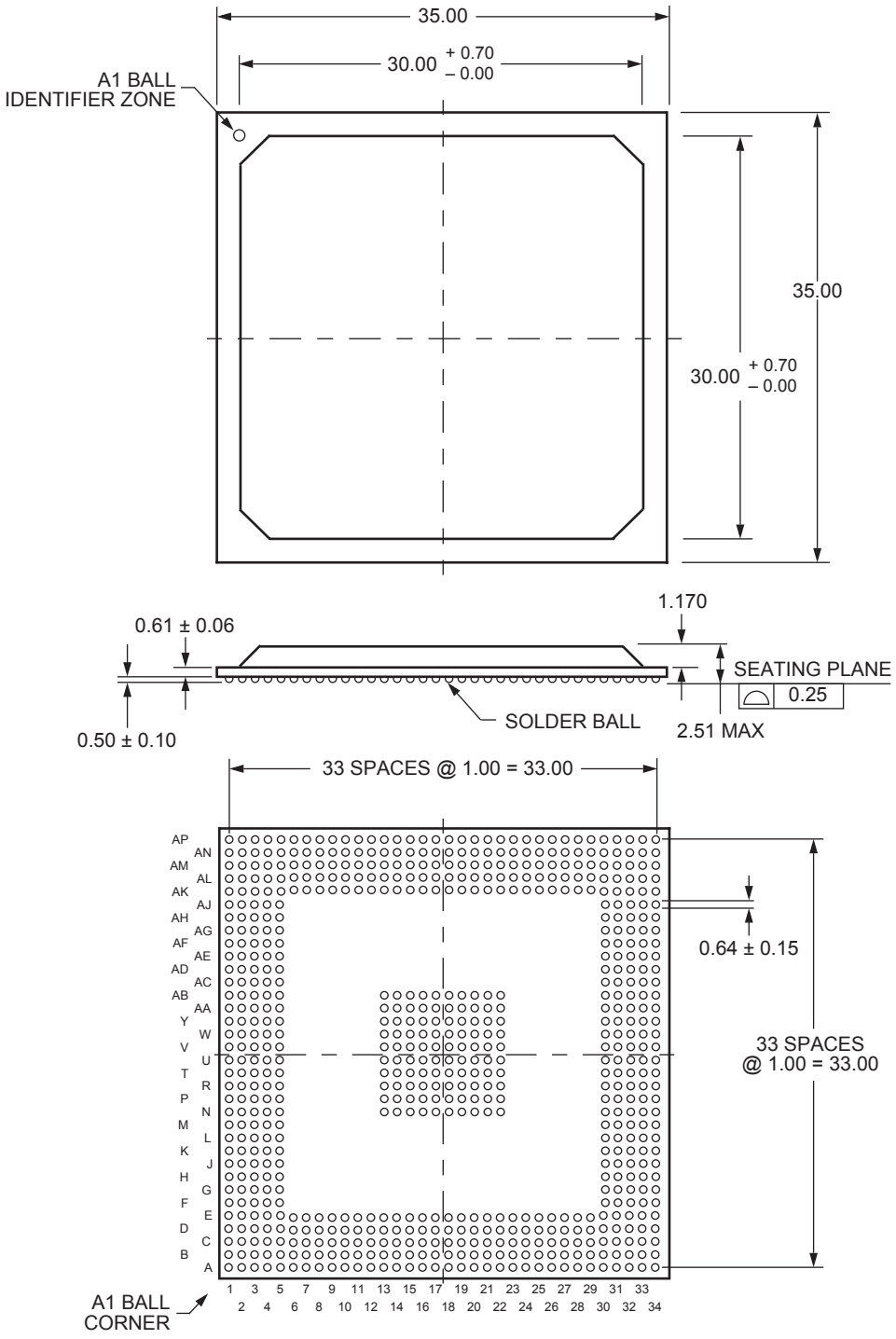
Reference (REF): The reference dimension is an untoleranced dimension used for informational purposes only. It is a repeated dimension or one that can be derived from other values in the drawing.

Minimum (MIN) or Maximum (MAX): Indicates the minimum or maximum allowable size of a dimension.

Package Outline Diagrams (continued)

680-Pin PBGAM

Dimensions are in millimeters.



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Ordering Information

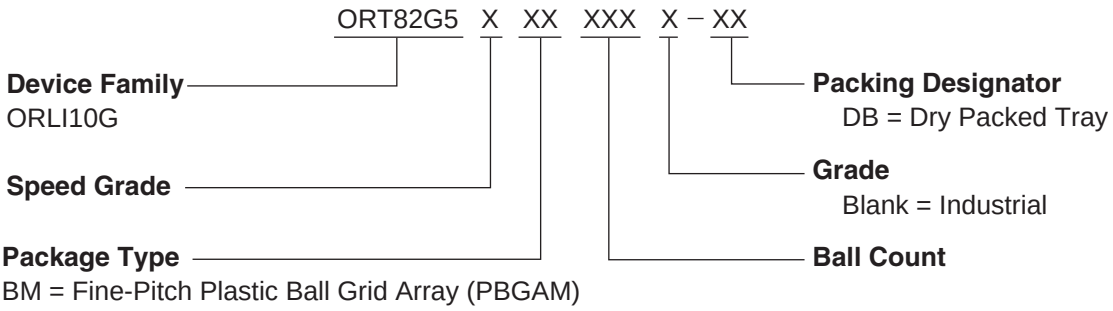

Table 37. Device Type Options

Device	Voltage
ORT82G5	1.5 V internal 3.3 V/2.5 V/1.8 V/1.5 V I/O

Table 38. Temperature Range

Symbol	Description	Ambient Temperature
(Blank)	Industrial	–40 ˚C to +85 ˚C

Note: Device junction temperature of –40 ˚C to +125 ˚C are recommended

Table 39. Ordering Information

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade	Packing Designator
ORT82G5	ORT82G53BM680-DB	3	PBGAM	680	I	DB
	ORT82G52BM680-DB	2	PBGAM	680	I	DB
	ORT82G51BM680-DB	1	PBGAM	680	I	DB

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