DMC96101 (Tentative)

Silicon NPN epitaxial planar type

For digital circuits

■ Absolute Maximum Ratings $T_a = 25°C$

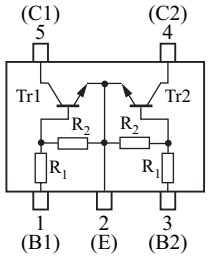
Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	V_{CBO}	50	V
Collector-emitter voltage (Base open)	V_{CEO}	50	V
Collector current	I_C	100	mA
Total power dissipation	P_T	125	mW
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	–55 to +150	°C

■ Package

- Code
  SSMini5-F4-B
- Pin Name
  1: Base (Tr1) 4: Collector (Tr2)
  2: Emitter (Common) 5: Collector (Tr1)
  3: Base (Tr2)

■ Marking Symbol: E1

■ Internal Connection



Resistance value	R_1	10	kΩ
	R_2	10	

■ Electrical Characteristics $T_a = 25°C \pm 3°C$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	V_{CBO}	$I_C = 10\ \mu A$, $I_E = 0$	50			V
Collector-emitter voltage (Base open)	V_{CEO}	$I_C = 2$ mA, $I_B = 0$	50			V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{CB} = 50$ V, $I_E = 0$			0.1	μA
Collector-emitter cutoff current (Base open)	I_{CEO}	$V_{CE} = 50$ V, $I_B = 0$			0.5	μA
Emitter-base cutoff current (Collector open)	I_{EBO}	$V_{EB} = 6$ V, $I_C = 0$			0.5	mA
Forward current transfer ratio	h_{FE}	$V_{CE} = 10$ V, $I_C = 5$ mA	35			—
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = 10$ mA, $I_B = 0.5$ mA			0.25	V
Output voltage high-level	V_{OH}	$V_{CC} = 5$ V, $V_B = 0.5$ V, $R_L = 1$ kΩ	4.9			V
Output voltage low-level	V_{OL}	$V_{CC} = 5$ V, $V_B = 2.5$ V, $R_L = 1$ kΩ			0.2	V
Input resistance	R_1		–30%	10	+30%	kΩ
Resistance ratio	R_1 / R_2		0.8	1.0	1.2	—

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

SSMini5-F4-B

Unit: mm