

DATA SHEET

CBTD3253

Dual 1-of-4 FET multiplexer/demultiplexer
with level shifting

Preliminary data

2002 Sep 09

Dual 1-of-4 FET multiplexer/demultiplexer with level shifting

CBTD3253

FEATURES

- 5 Ω switch connection between two ports
- TTL-compatible input levels
- Designed to be used in level shifting applications
- Minimal propagation delay through the switch
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA

DESCRIPTION

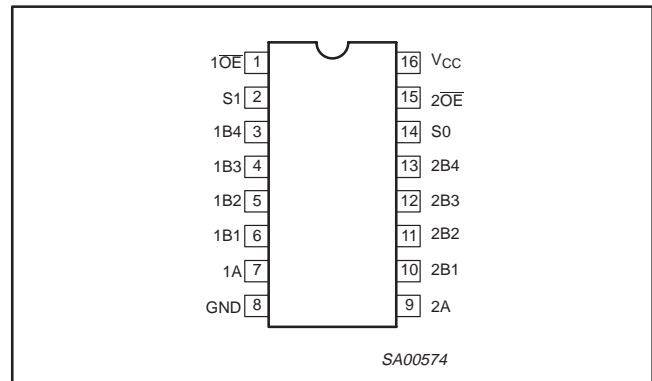
The CBTD3253 is a dual 1-of-4 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

$1\overline{OE}$, $2\overline{OE}$, S0, and S1 select the appropriate B output for the A-input data.

Internal diode allows voltage level shifting from 5 V inputs to 3.3 V outputs.

The CBTD3253 is characterized for operation from -40 to $+85^{\circ}\text{C}$.

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	Output enable
2	S1	Select-control input
3, 4, 5, 6	1B[1–4]	B outputs
7	1A	A input
8	GND	Ground (0 V)
9	2A	A input
10, 11, 12, 13	2B[1–4]	Select-control input
14	S0	Select-control input
15	$2\overline{OE}$	Output enable
16	V_{CC}	Positive supply voltage

ORDERING INFORMATION

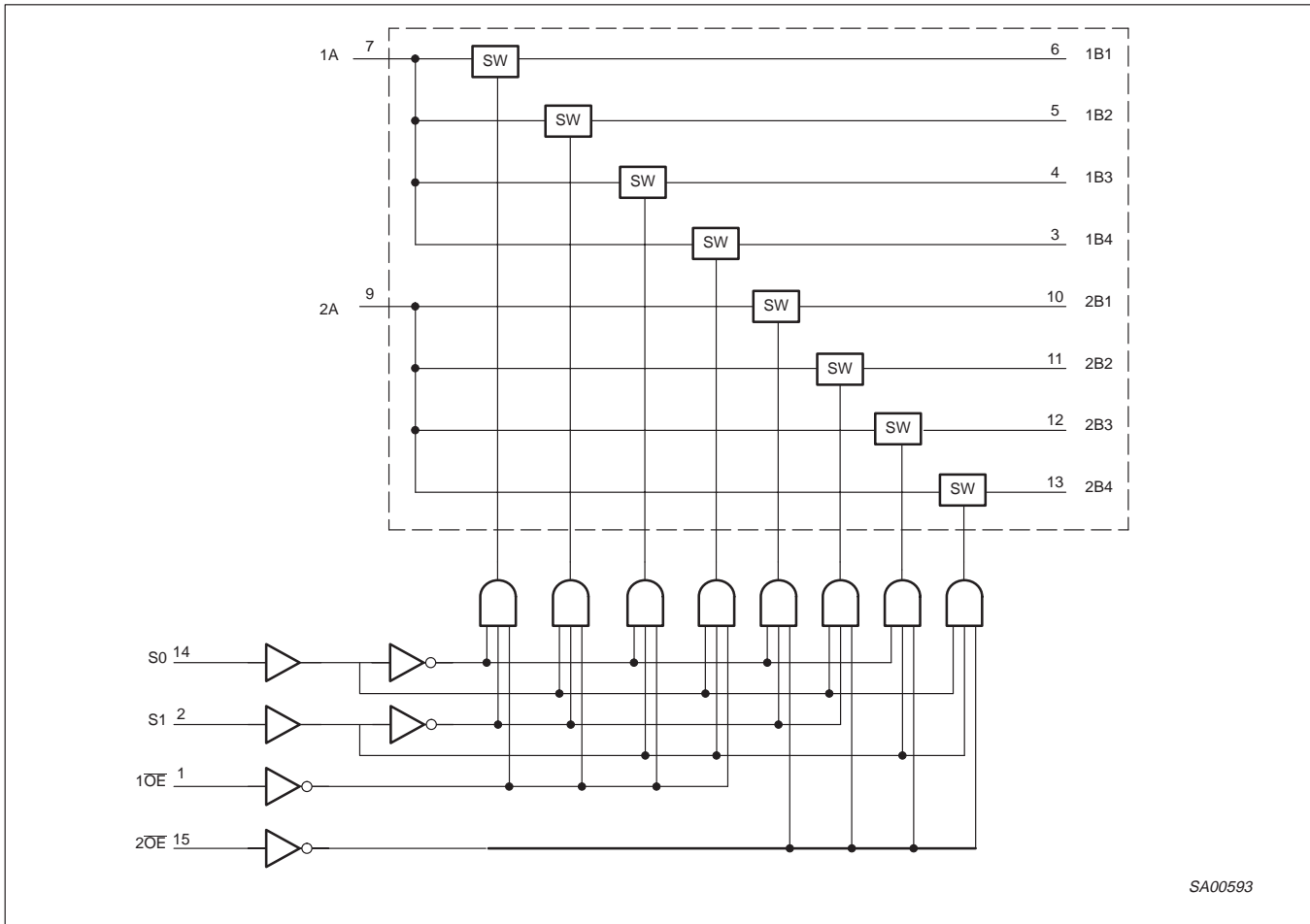
PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DWG NUMBER
16-pin plastic SOIC	-40 to 85°C	CBTD3253D	CBTD3253	SOT109-1
16-pin plastic SSOP	-40 to 85°C	CBTD3253DB	CD3253	SOT338-1
16-pin plastic SSOP (QSOP)	-40 to 85°C	CBTD3253DS	CBD3253	SOT519-1
16-pin plastic TSSOP	-40 to 85°C	CBTD3253PW	CBD3253	SOT403-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

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LOGIC DIAGRAM (positive logic)



FUNCTION TABLE

INPUTS				FUNCTION
OE1	OE2	S1	S0	
H	X	X	X	Disconnect 1A
X	H	X	X	Disconnect 2A
L	L	L	L	1A to 1B1 and 2A to 2B1
L	L	L	H	1A to 1B2 and 2A to 2B2
L	L	H	L	1A to 1B3 and 2A to 2B3
L	L	H	H	1A to 1B4 and 2A to 2B4

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ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
V_I	DC input voltage ²		-0.5 to +7.0	V
	Continuous channel current		128	mA
I_K	Input clamp current	$V_{I/O} < 0$	-50	mA
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2	—	V
V_{IL}	Low-level Input voltage	—	0.8	V
T_{amb}	Operating free-air temperature range	-40	+85	°C

NOTE:

- All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
			$T_{amb} = -40 \text{ to } +85 \text{ °C}$				
			MIN	TYP ¹	MAX		
V_{IK}	Input clamp voltage	$V_{CC} = 4.5 \text{ V}; I_I = -18 \text{ mA}$	—	—	-1.2	V	
V_P	Pass voltage	$V_I = V_{CC} = 5.5 \text{ V}; I/O = -100 \text{ mA}$	3.4	3.6	3.9	V	
I_I	Input leakage current	$V_{CC} = 5 \text{ V}; V_I = 5.5 \text{ or GND}$	—	—	± 1	μA	
I_{CC}	Quiescent supply current	$V_{CC} = 5.5 \text{ V}; I_O = 0, V_I = V_{CC} \text{ or GND}$	—	—	15	mA	
ΔI_{CC}	Control inputs ²	$V_{CC} = 5.5 \text{ V}$, one input at 3.4 V, other inputs at V_{CC} or GND	—	—	1.5	mA	
C_I	Control pins	$V_I = 3 \text{ V or } 0$	—	4.5	—	pF	
$C_{IO(OFF)}$	Power-off leakage current	A port	—	23.5	—	pF	
		B port	—	6.5	—		
r_{on}^3	On-resistance	$V_{CC} = 4.5 \text{ V}$	$V_I = 0 \text{ V}; I_I = 64 \text{ mA}$	—	5	7	Ω
			$V_I = 0 \text{ V}; I_I = 30 \text{ mA}$	—	5	7	
			$V_I = 2.4 \text{ V}; I_I = 15 \text{ mA}$	—	16	50	

NOTES:

- All typical values are at $V_{CC} = 5 \text{ V}$, $T_{amb} = 25 \text{ °C}$.
- This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND
- Measured by the voltage drop between the A and the B terminals at the indicated current through the switch.
On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

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AC CHARACTERISTICS

T_{amb} = -40 to +85 °C; C_L = 50 pF

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	LIMITS		UNIT
				V _{CC} = +5.0 V ±0.5 V		
				MIN	MAX	
t _{pd}	Propagation delay ¹	A or B	B or A	—	0.25	ns
		S	A or B	1.6	11.0	
t _{en}	Output enable time to High and Low level	S	A or B	1.6	11.0	ns
		\overline{OE}		1.6	11.4	
t _{dis}	Output disable time from High and Low level	S	A or B	2.2	8	ns
		\overline{OE}		2.0	7	

NOTE:

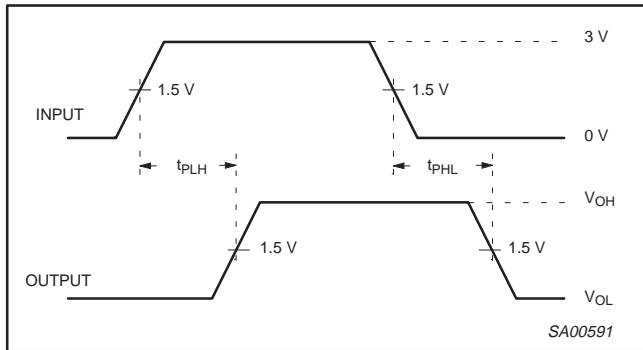
1. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Dual 1-of-4 FET multiplexer/demultiplexer with level shifting

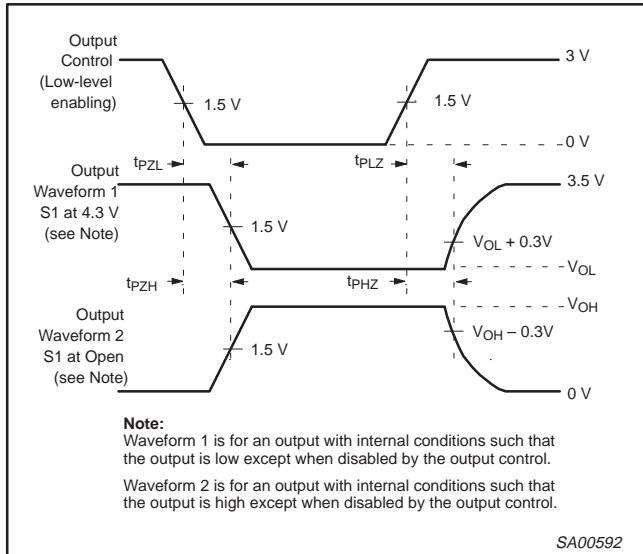
CBTD3253

AC WAVEFORMS

$V_M = 1.5\text{ V}$, $V_{IN} = \text{GND to } 3.0\text{ V}$



Waveform 1. Pulse duration

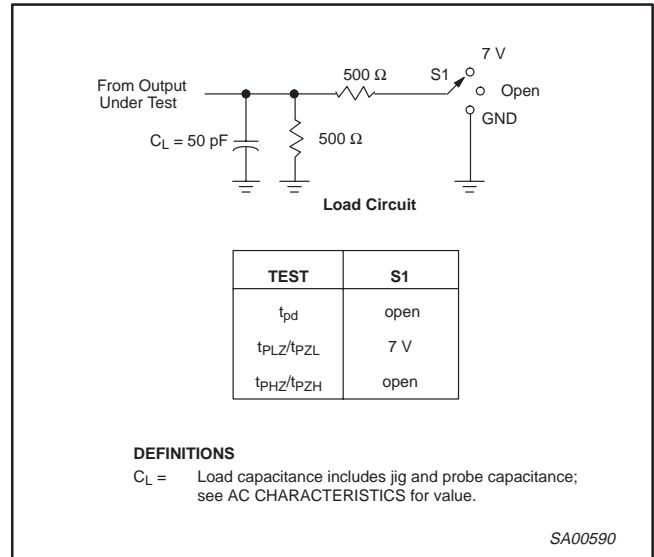


Waveform 2. 3-State Output Enable and Disable Times

NOTES:

1. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
2. t_{PZL} and t_{PZH} are the same as t_{en} .
3. t_{PLH} and t_{PHL} are the same as t_{pd} .

TEST CIRCUIT AND WAVEFORMS



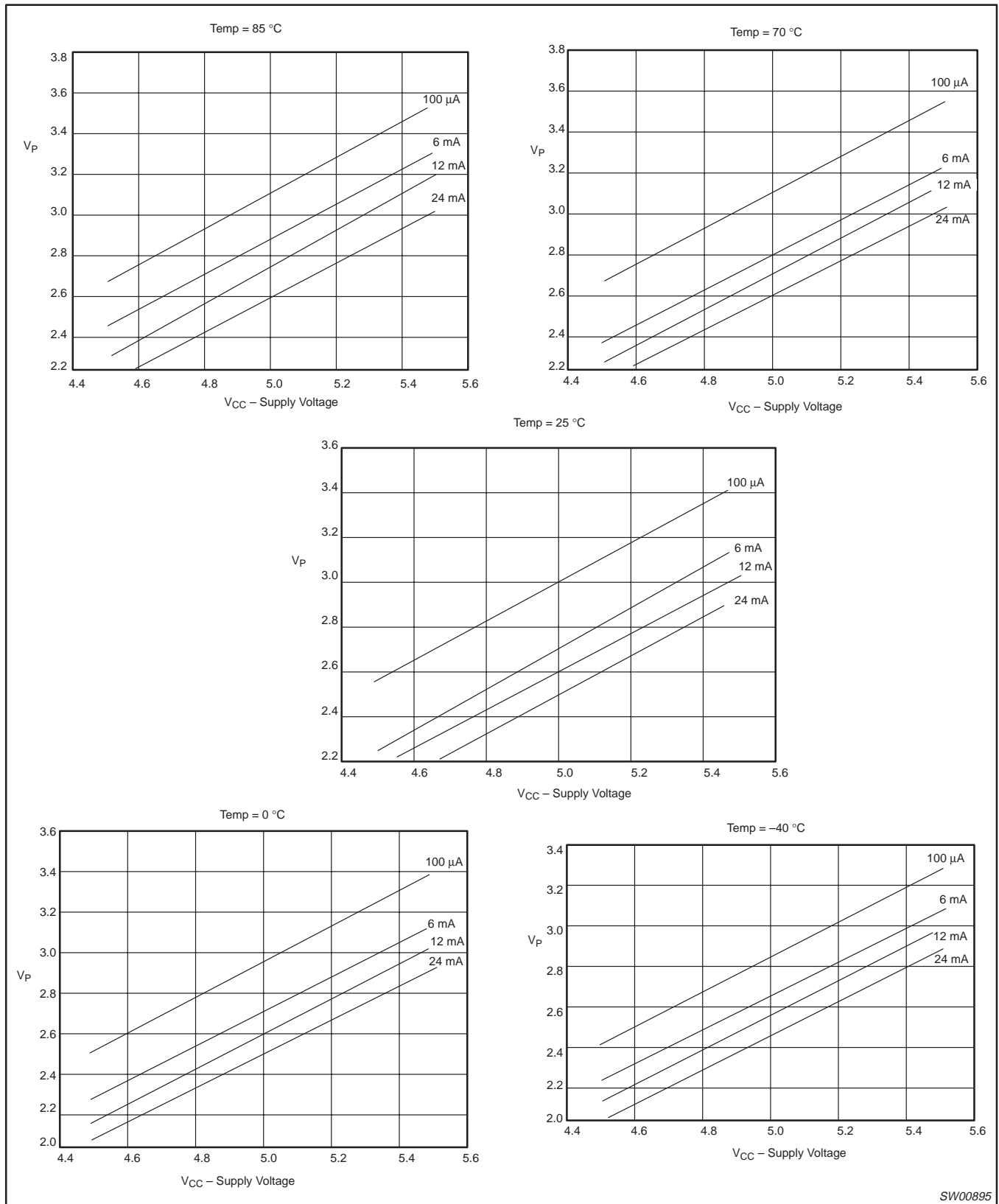
NOTES:

1. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
2. The outputs are measured one at a time with one transition per measurement.

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TYPICAL CHARACTERISTICS



SW00895

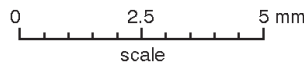
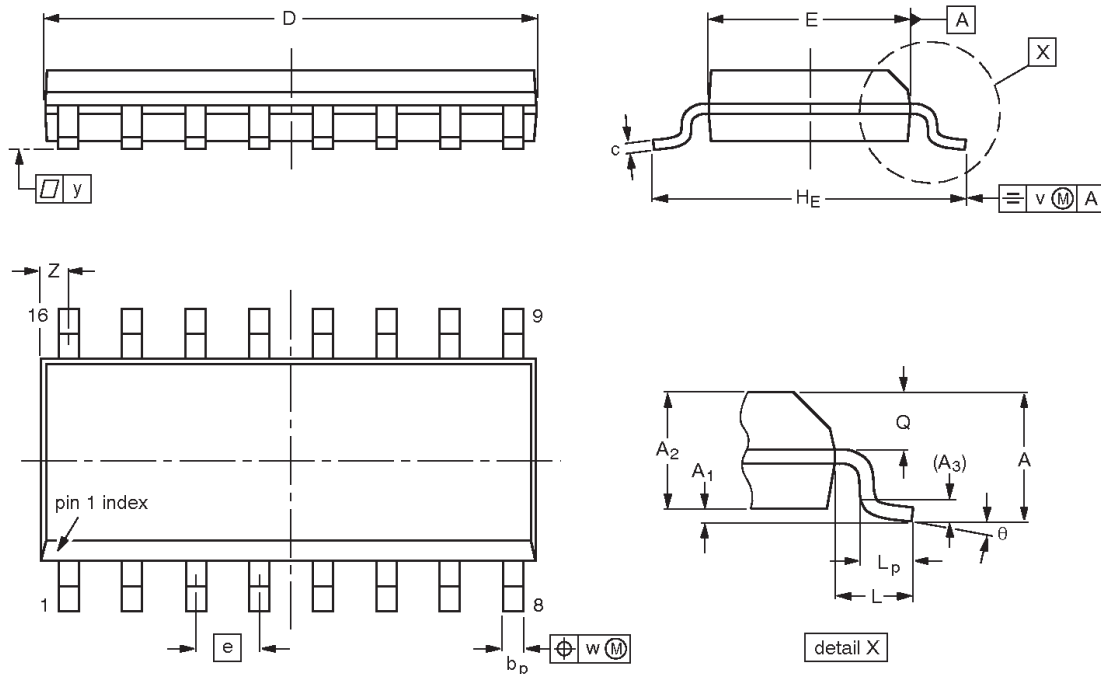
Figure 1. V_{OH} values ($V_{in} = V_{CC}$)

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

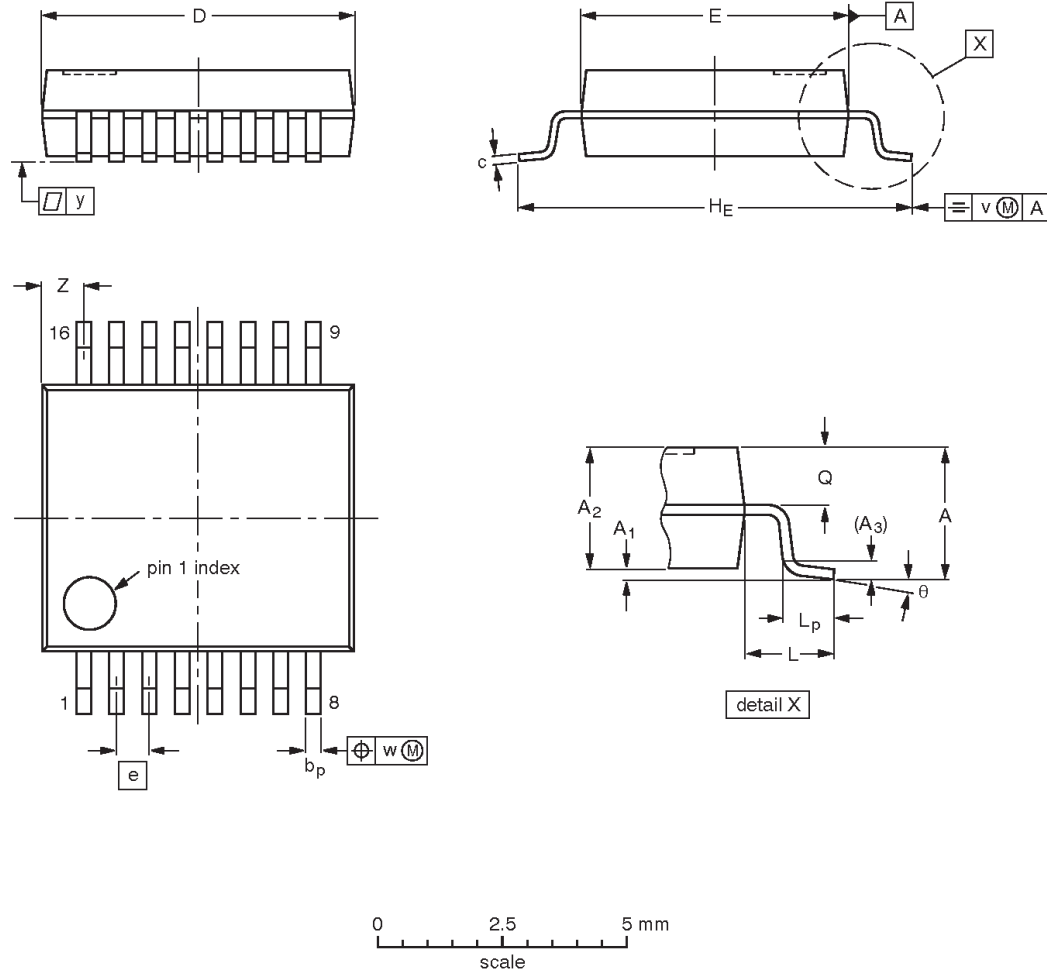
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07	MS-012				97-05-22- 99-12-27

Dual 1-of-4 FET multiplexer/demultiplexer with level shifting

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SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

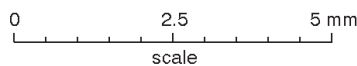
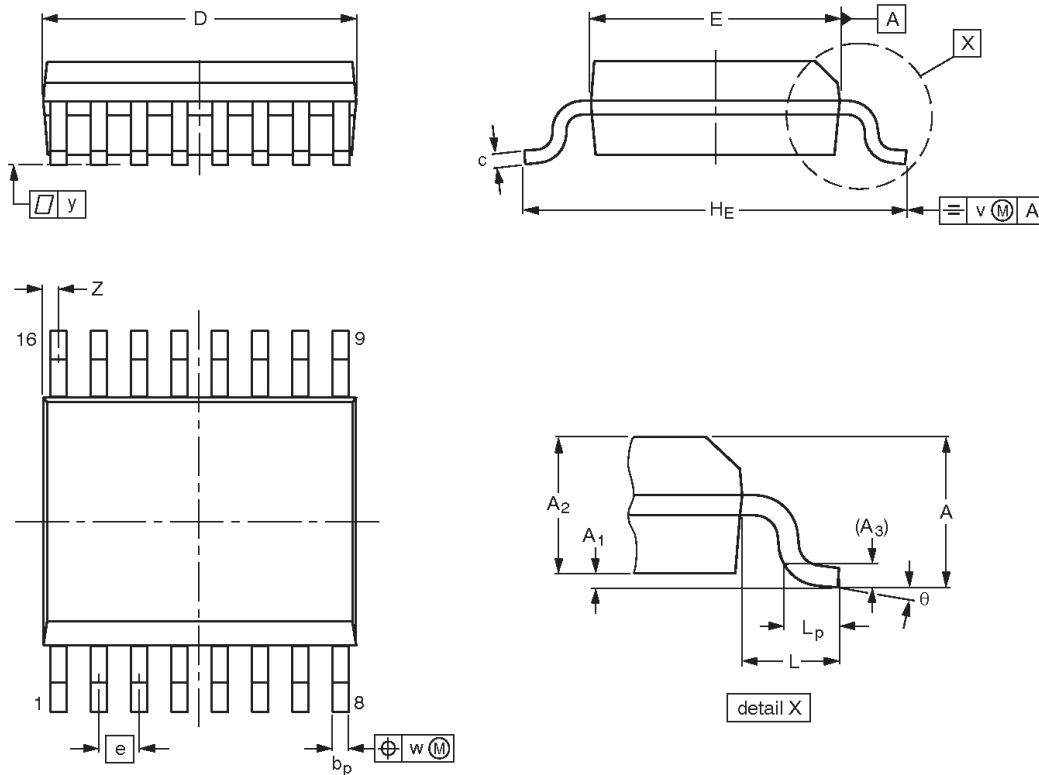
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150				95-02-04 99-12-27

Dual 1-of-4 FET multiplexer/demultiplexer with level shifting

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SSOP16: plastic shrink small outline package; 16 leads;
body width 3.9 mm; lead pitch 0.635 mm

SOT519-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	5.0 4.8	4.0 3.8	0.635	6.2 5.8	1.0	0.89 0.41	0.2	0.18	0.09	0.18 0.05	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

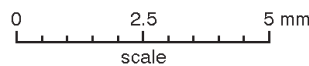
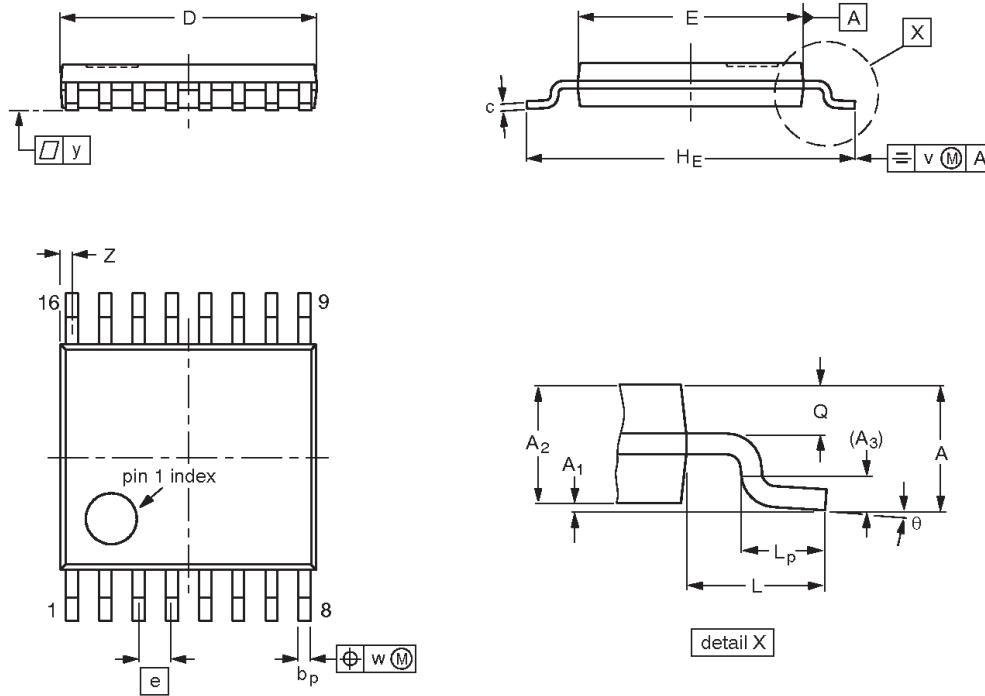
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT519-1						99-05-04

Dual 1-of-4 FET multiplexer/demultiplexer with level shifting

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				95-04-04 99-12-27

Dual 1-of-4 FET multiplexer/demultiplexer with level shifting

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Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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^[1] Please consult the most recently issued datasheet before initiating or completing a design.

^[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

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