e2v technologies

CCD97-00 Back Illuminated 2-Phase IMO Series Peltier Pack Electron Multiplying CCD Sensor

INTRODUCTION

The CCD97 is part of the new L3Vision™ range of products from e2v technologies. This device uses a novel output amplifier circuit that is capable of operating at an equivalent output noise of less than one electron at pixel rates of over 11 MHz. This makes the sensor well suited for scientific imaging where the illumination is limited.

The sensor is a frame transfer device and can operate in inverted mode to suppress dark current as this is now the dominant noise source (even at high readout rate). The image and store sections are designed to operate in 2-phase mode, to maximise the highest achievable parallel transfer frequency.

The sensor functions by converting photons to charge in the image area during the integration time period, then transferring this charge through the image and store sections into the readout register. Following transfer through the readout register, the charge is multiplied in the gain register before conversion to a voltage by an output amplifier.

The sensor has two output amplifiers; a low noise, high responsivity output for normal CCD operation and a large signal amplifier for when multiplication gain is employed.

Operation of the high gain mode is controlled by adjustment of the multiplication phase amplitude R∅2HV.

GENERAL DATA

Active image area	8.192 x 8.192 mm
Image section active pixels	512 (H) x 512 (V)
Image pixel size	16 x 16 µm
Number of output amplifiers	2
Fill factor	100%
Additional dark reference columns	24
Additional overscan rows	16

PACKAGE DETAILS (nominal, see Fig. 15)

Peltier Cooled Package

Overall dimensions	34.2 x 30.48 mm
Number of pins	32
Inter-pin spacing	1.778 mm
Opposite row spacing	30.48 mm
Window material	sapphire
Mounting position	any

STORAGE AND OPERATION TEMPERATURE EXTREMES

	MIN	MAX
Storage temperature (°C)	−55	+125
Operating temperature (°C)	−55	+60
Temperature ramping (°C/min)	-	5

Users wishing to operate the device outside this range are advised to consult e2v technologies.

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TYPICAL PERFORMANCE SPECIFICATIONS

Except where otherwise specified, the following are measured for operation at a pixel rate of 11 MHz, with typical operating voltages. Parameters are given at 223 K unless specified otherwise. Where parameters are different in the normal and high gain mode, both are given.

PARAMETER	UNIT	MIN	TYPICAL	MAX
Output amplifier responsivity, HR amplifier (normal mode) (see note 1)	$\mu V/e^-$	-	5.3	-
Output amplifier responsivity, LS amplifier (normal mode) (see note 1)	$\mu V/e^-$	-	1.1	-
Multiplication register gain, LS amplifier (high gain mode) (see notes 2 and 3)		1	-	1000
Peak signal - 2-phase IMO	e^-/pixel	90k	130k	-
Charge handling capacity of multiplication register (see note 4)	e^-/pixel	-	800k	-
Readout noise at 50 kHz with CDS, HR amplifier (normal mode) (see note 5)	e^- rms	-	2.2	-
Readout noise at 1 MHz with CDS, HR amplifier (normal mode) (see note 5)	e^- rms	-	5.4	-
Amplifier reset noise (without CDS), HR amplifier (normal mode) (see note 5)	e^- rms	-	50	-
Readout noise at 50 kHz with CDS, LS amplifier (normal mode) (see note 5)	e^- rms	-	6	-
Readout noise at 1 MHz with CDS, LS amplifier (normal mode) (see note 5)	e^- rms	-	14	-
Amplifier reset noise (without CDS), LS amplifier (normal mode) (see note 5)	e^- rms	-	120	-
Readout noise at 1 MHz (high gain mode) (see note 5)	e^- rms	-	<1	-
Maximum frequency (settling to 1%), HR amplifier (see notes 5 and 6)	MHz	-	-	3
Maximum frequency (settling to 5%), HR amplifier (see notes 5 and 6)	MHz	-	-	4.5
Maximum frequency (settling to 1%), LS amplifier (see notes 5 and 6)	MHz	-	-	9
Maximum frequency (settling to 5%), LS amplifier (see notes 5 and 6)	MHz	-	-	15
Maximum parallel transfer frequency (see note 1)	MHz	-	1.6	-
Dark signal at 293 K (see note 7)	e^-/pixel/s	-	400	800
Dark signal non-uniformity (DSNU) at 293 K (see note 8)	e^-/pixel/s	-	60	-
Excess noise factor (see note 9)		-	$\sqrt{2}$	-

NOTES

1. Measured at a pixel rate of 1 MHz.
2. The typical variation of gain with R∅2HV at different temperatures is shown in Fig. 1.
3. Some increase of R∅2HV may be required throughout life to maintain gain performance. Adjustment of R∅2HV should be limited to the maximum specified under Operating Conditions.
4. When multiplication gain is used, a linear response of output signal with input signal is achieved for output signals up to 400 ke^- typically.
5. These values are inferred by design and not measured.
6. The quoted maximum frequencies assume a 20 pF load and that correlated double sampling is being implemented. If, instead, single sampling is used, the output will be settled to 1% at 15 MHz typically.
7. The quoted dark signal has the usual temperature dependence for inverted mode operation. For operation at high frame rates with short integration times, there will also be a significant component generated during readout through the register. Operating at a temperature of 293 K and 30 Hz frame rate, the readout component contributes 8 e^-/pixel/frame typically, at a gain of 1000 and referenced to the image area, and has a temperature dependence consistent with non-inverted mode operation.

   There exists a further weakly temperature dependent component, the clock induced charge, which is independent of the integration time. The clock induced charge is dependent on the operating biases and timings employed and is typically 0.1 e^-/pixel/frame at T = −55 °C.

   For more information, refer to the technical note "Dark Signal and Clock-Induced Charge in L3Vision™ CCD Sensors".
8. DSNU is defined as the 1σ variation of the dark signal.
9. The excess noise factor is defined as the factor by which the multiplication process increases the shot noise on the image when multiplication gain is used.

DEVICE COSMETIC PERFORMANCE

Grade 1 devices are supplied to the blemish specification shown below.

Note that incorrect biasing of the device may result in spurious dark or white blemishes appearing. These will be eliminated if the biases are adjusted.

Test Conditions

Operating mode	Devices run in 2-phase inverted mode, with an integration time of 30 ms and a readout rate of 11 MHz.
Sensor temperature	-5 ± 3 °C.
Multiplication gain	Set to approximately 1000.
Illumination	Set to give a signal level of approximately 30 e^-/pixel/frame.

BLEMISH SPECIFICATION

Black Columns Black defects are counted when they have a responsivity of less than 80% of the local mean signal at approximately the specified gain and level of illumination. A black column contains at least 9 black defects.

White Columns White defects are pixels having a dark signal generation rate corresponding to an output signal of greater than 5 times the maximum dark signal level. A white column contains at least 9 white defects.

Pin-Head Columns Pin-head columns are manifest as a partial dark column with a bright pixel showing photoresponse at the end of the column nearest to the readout register. Pin-head columns are counted when the black column has a responsivity of less than 80% of the local mean signal at approximately the specified multiplication gain and level of illumination. A pin-head column contains at least 9 black defects.

SPECIFICATION

PARAMETER	GRADE 1 SPECIFICATION	GRADE 2 SPECIFICATION
White Columns	0	0
Black/Pin-head Columns	0	2

ORDERING INFORMATION

PART NUMBER	OPERATING MODE	COATING	WINDOW
CCD97-00-*-444	2-phase IMO	Midband	Permanent

* denotes grade of device.

Figure 1: TYPICAL VARIATION OF MULTIPLICATION GAIN WITH R∅2HV AT DIFFERENT TEMPERATURES

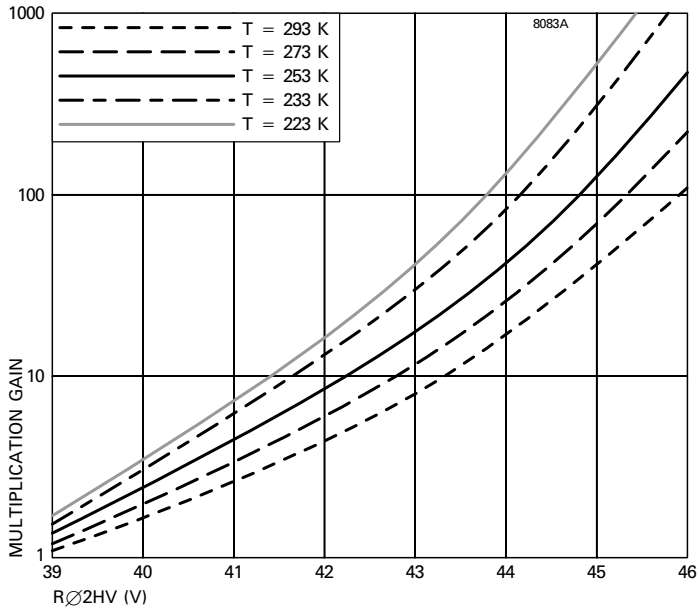


Figure 2: TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE

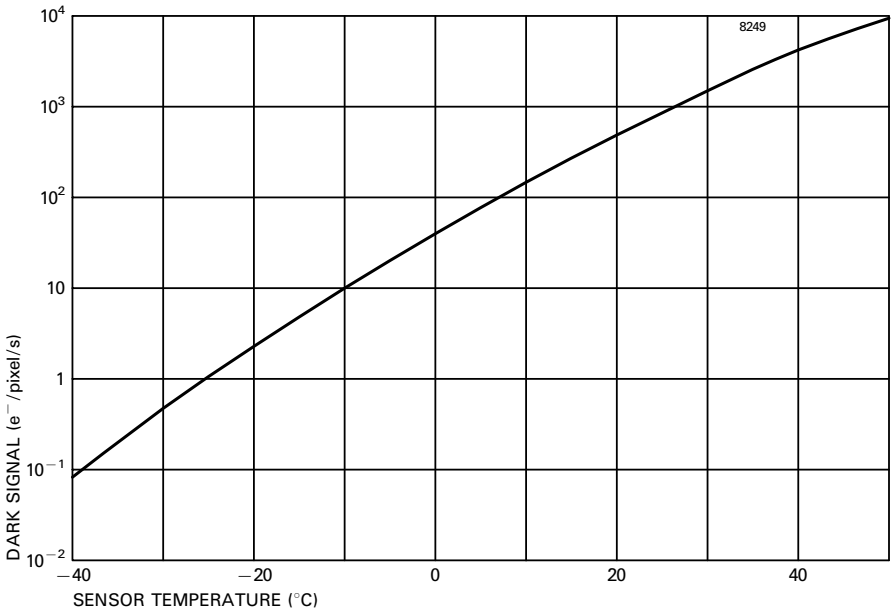
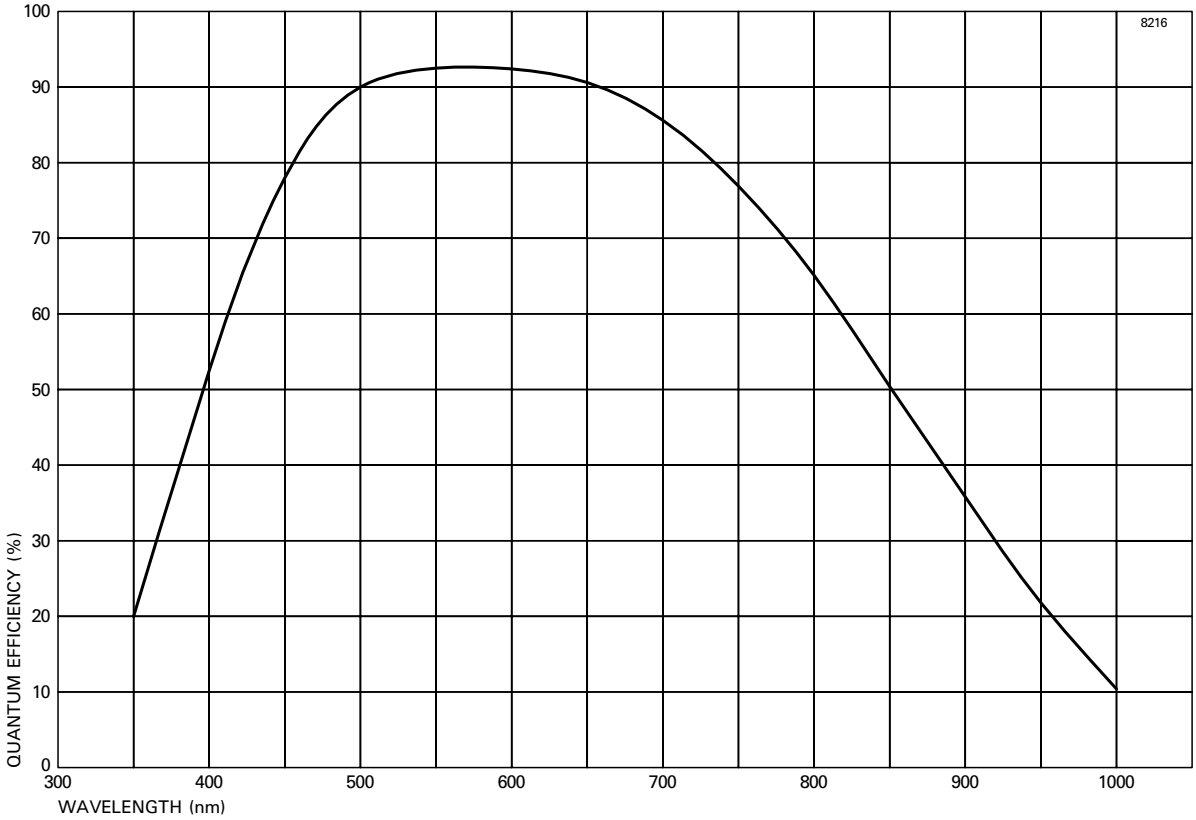


Figure 3: TYPICAL SPECTRAL RESPONSE (Mid-band coated, no window, T = −20 °C)



ABSOLUTE MAXIMUM RATINGS

Maximum ratings are with respect to SS.

PIN	CONNECTION	MIN (V)	MAX (V)
1	Thermistor		
2	ABD	−0.3	+25
3	IØ3	−20	+20
4	IØ1	−20	+20
5	IØ2	−20	+20
6	IØ4	−20	+20
7	OG	−20	+20
8*	OSH	−0.3	+25
9	DD	−0.3	+25
10	RØ2	−20	+20
11	RØ1	−20	+20
12	RØ3	−20	+20
13	ØRL	−20	+20
14	SS	0	
15*	OSL	−0.3	+25
16	ODL	−0.3	+32
17	RØ2HV	−20	+50
18	RØDC	−20	+20
19	SS	0	
20	n.c.		
21	RDL	−0.3	+25
22	DG	−20	+20
23	ØRH	−20	+20
24	RDH	−0.3	+25
25	n.c.		
26	ODH	−0.3	+32
27	SØ4	−20	+20
28	SØ2	−20	+20
29	SØ1	−20	+20
30	SØ3	−20	+20
31	IG	−20	+20
32	Thermistor		

n.c. not connected.

* Permanent damage may result if, in operation, OSL or OSH experience short-circuit conditions.

Maximum voltages between pairs of pins:

PIN	CONNECTION	PIN	CONNECTION	MIN (V)	MAX (V)
8	OSH	26	ODH	−15	+15
15	OSL	16	ODL	−15	+15
17	RØ2HV	18	RØDC	−20	+50
17	RØ2HV	12	RØ3	−20	+50
Output transistor current (mA)					20

OPERATION OF PELTIER COOLER

Operating the device at 15 MHz pixel rate, with the heat extracted from the base of the package using a 1 °C/W heatsink to an ambient temperature of 30 °C, cooling the sensor to −10 °C will typically require a Peltier supply current of approximately 3 A and a potential of approximately 1 V.

THERMISTOR

The package includes a Fenwal thermistor for temperature sensing, part number 196-302LAD-002.

ESD HANDLING PROCEDURES

CCD sensors, in common with most high performance IC devices, are static sensitive. In certain cases a static electricity discharge may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench.
- Operator wearing a grounded wrist strap.
- All receiving socket pins to be positively grounded.
- Unattended CCDs should not be left out of their conducting foam or socket.

All devices are provided with internal protection circuits to most gate electrodes but not to the other pins.

Evidence of incorrect handling will terminate the warranty.

EXPOSURE TO RADIATION

Exposure to radiation may irreversibly damage the device and result in degradation of performance. Users wishing to operate the device in a radiation environment are advised to consult e2v technologies.

OPERATING CONDITIONS

Typical operating voltages are as given in the table below. Some adjustment within the minimum-maximum range specified may be required to optimise performance.

CONNECTION	PULSE AMPLITUDE OR DC LEVEL (V)		
	Min	**Typical**	**Max**
I∅1,2,3,4 high	+5 (see note 10)	+7	+9 (see note 10)
I∅1,2,3,4 low	−6	−5	−4
S∅1,2,3,4 high	+5 (see note 10)	+7	+9 (see note 10)
S∅1,2,3,4 low	−6	−5	−4
R∅1,2,3 high	+8	+12	+13
R∅1,2,3 low	-	0	-
R∅2HV high	+20	+40	+50 (see note 3
R∅2HV low	0	+4	+5
∅RL, ∅RH high	see note 11	+10	see note 11
∅RL, ∅RH low	-	0	-
R∅DC	+2	+3	+5
OG	+1	+3	+5
IG	-	−5	-
SS	0	+4.5	+7
ODL, ODH	+25	+28	+32
RDL, RDH	+15	+17	+20
ABD	+10	+18	+20
DG low	-	0	-
DG high	+10	+12	+13
DD	+20	+24	+25

NOTES

10. I∅ and S∅ adjustment may be common.
11. ∅RL and ∅RH high level may be adjusted in common with R∅1,2,3.
12. Other than the output gates (OG), there are no common connections made between the two amplifiers, and either can be powered down by connecting the appropriate output drain (OD) connection to substrate (SS). The reset drains (RD) should remain biased, with the reset gate (∅R) clocked normally or held at clock low level.

An external load is required for each output amplifier. For the HR amplifier, this can be a resistor of about 5 kΩ or a constant current type of about 5 mA. For the LS amplifier, the load should be either 5 kΩ or 5 mA. The on-chip amplifier power dissipation is approximately 30 mW for the HR amplifier and 40 mW for the LS amplifier.

DRIVE PULSE WAVEFORM SPECIFICATION

The device is of a 4-phase construction, designed to operate in 2-phase inverted mode. This is achieved by applying common timings to phases ∅1 and ∅2, and phases ∅3 and ∅4 of the image and store sections. Suggested timing diagrams are shown in Figs. 4 - 11. The following are suggested pulse rise and fall times.

CLOCK PULSE	TYPICAL RISE TIME τ (ns)	TYPICAL FALL TIME τ (ns)	TYPICAL PULSE OVERLAP
I∅	120 < τ < 200	120 < τ < 200	@90% points
S∅	120 < τ < 200	120 < τ < 200	@90% points
R∅1	10	10	@70% points
R∅2	10	10	@70% points
R∅3	10	10	@70% points
R∅2HV	25	25	see note 14
R∅2HV	Sine	Sine	Sinusoid- high on falling edge of R∅1

NOTES

13. Register clock pulses are as shown in Figs. 5 and 6.
14. An example clocking scheme is shown in Fig. 5. R∅2HV can also be operated with a normal clock pulse, as shown in Fig. 6. The requirement for successful clocking is that R∅2HV reaches its maximum amplitude before R∅1 goes low.

ELECTRICAL INTERFACE CHARACTERISTICS

ELECTRODE CAPACITANCES AT MID CLOCK LEVELS				
Connection	**Capacitance to SS**	**Inter-phase Capacitances**	**Total Capacitance**	**Units**
I∅1	3.7	1.6	5.3	nF
I∅2	1.6	1.6	3.2	nF
I∅3	3.7	1.6	5.3	nF
I∅4	1.6	1.6	3.2	nF
S∅1	3.7	1.6	5.3	nF
S∅2	1.6	1.6	3.2	nF
S∅3	3.7	1.6	5.3	nF
S∅4	1.6	1.6	3.2	nF
R∅1	50	65	115	pF
R∅2	32	43	75	pF
R∅3	62	63	125	pF
R∅2HV	28	37	65	pF
SERIES RESISTANCES				
Connection	**Approximate Total Series Resistance**			
I∅1	17			Ω
I∅2	17			Ω
I∅3	17			Ω
I∅4	17			Ω
S∅1	17			Ω
S∅2	17			Ω
S∅3	17			Ω
S∅4	17			Ω
R∅1	6			Ω
R∅2	6			Ω
R∅3	6			Ω
R∅2HV	2			Ω
APPROXIMATE OUTPUT IMPEDANCE				
Large Signal Amplifier	350			Ω
High Responsivity Amplifier	250			Ω

Figure 4: CLOCKING SCHEME FOR 2-PHASE INVERTED MODE OPERATION

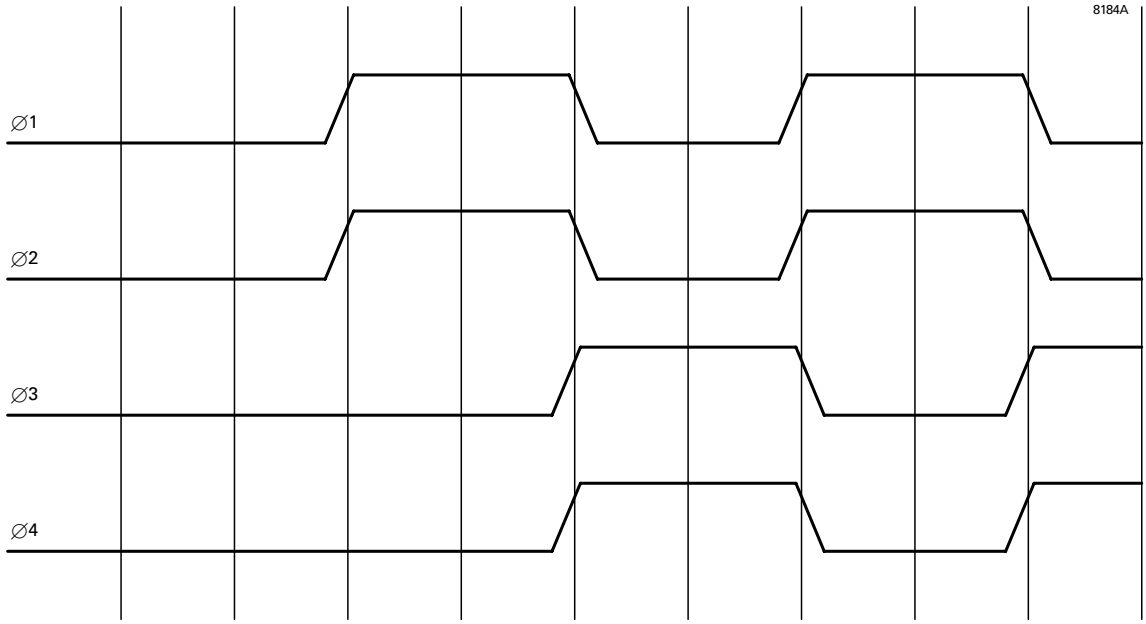


Figure 5: CLOCKING SCHEME FOR MULTIPLICATION GAIN
(Sine wave clocking scheme) (see note 15)

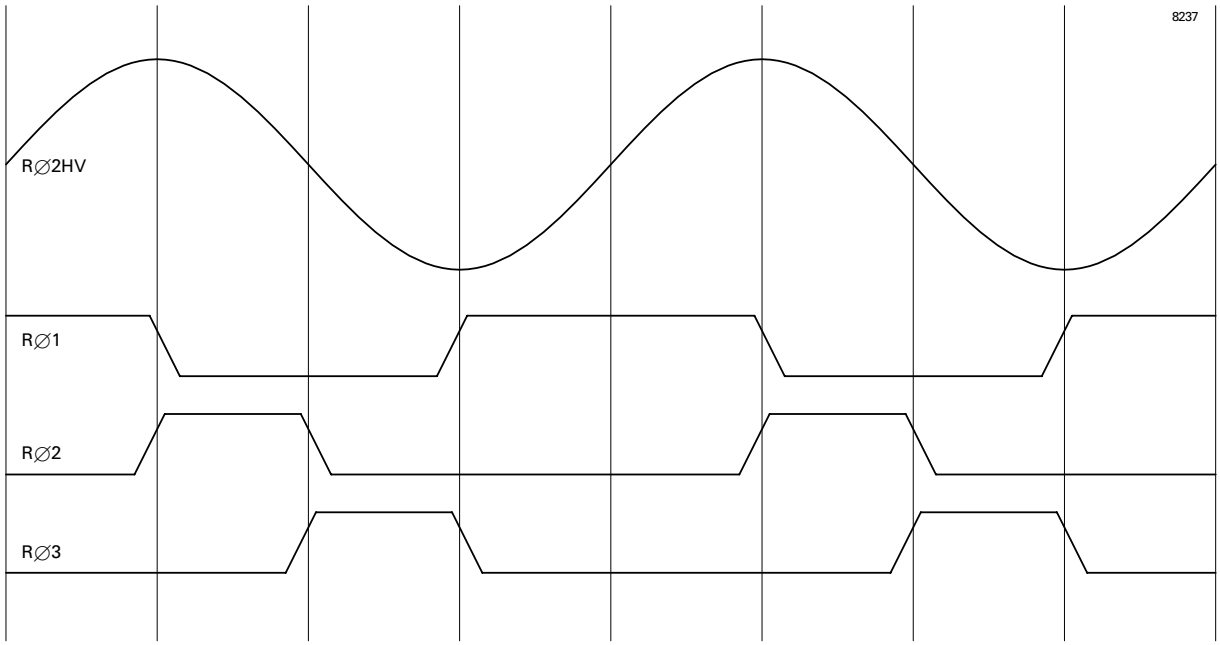
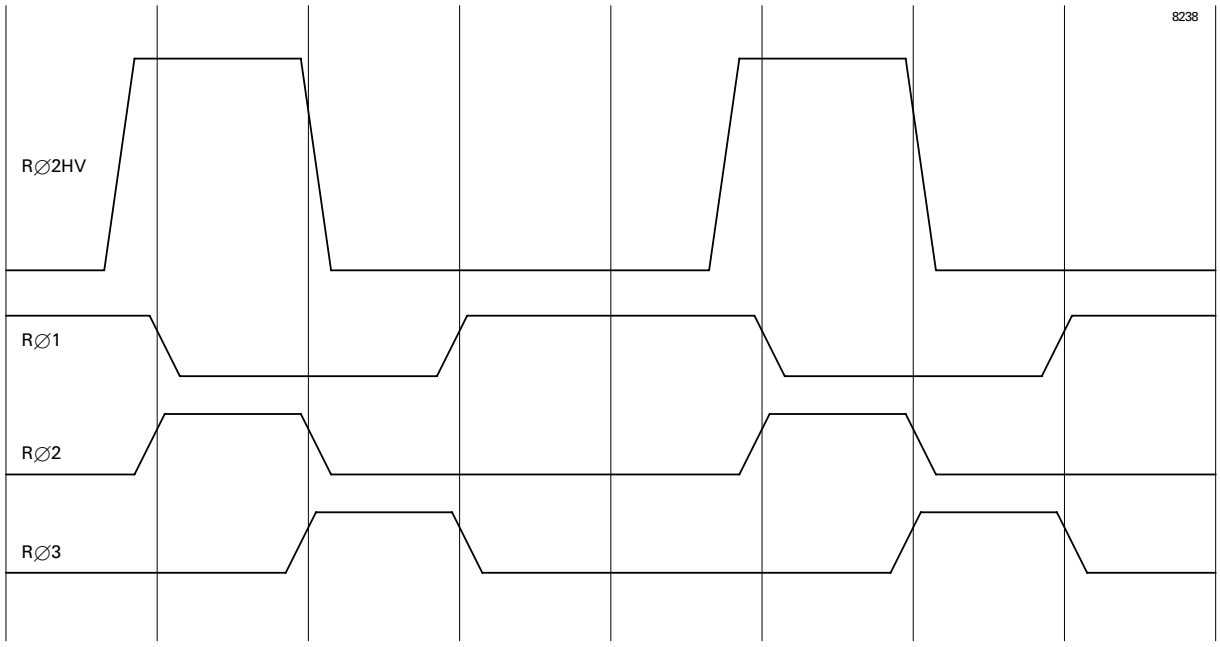


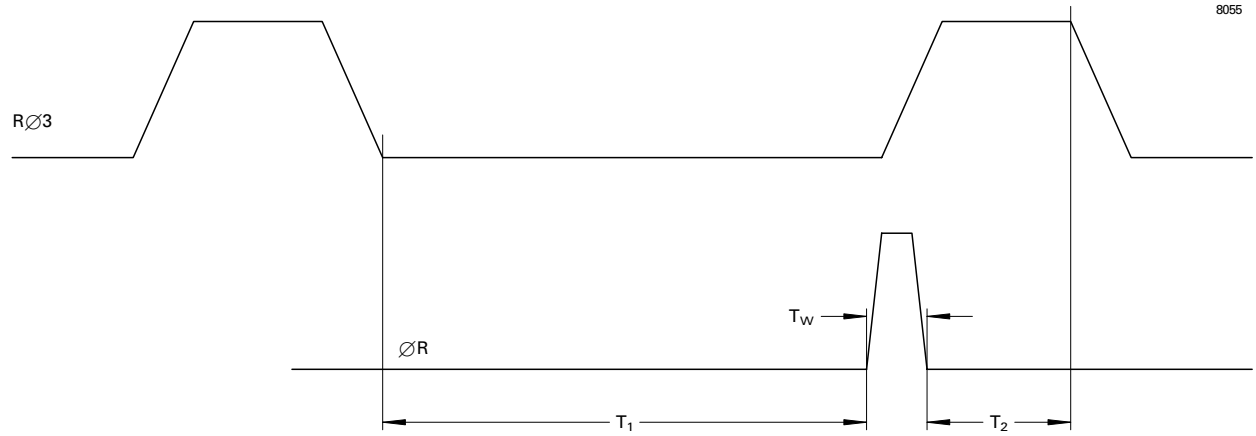
Figure 6: CLOCKING SCHEME FOR MULTIPLICATION GAIN
(Conventional clocking scheme) (see note 15)



NOTE
15. To operate through the OSH output amplifier, the RØ1 and RØ2 waveforms should be interchanged.

PULSE TIMINGS AND OVERLAPS

Figure 7: RESET PULSE



T_W = 10 ns typical
T_1 = output valid
T_2 > 0 ns

Figure 8: PULSE AND OUTPUT TIMING

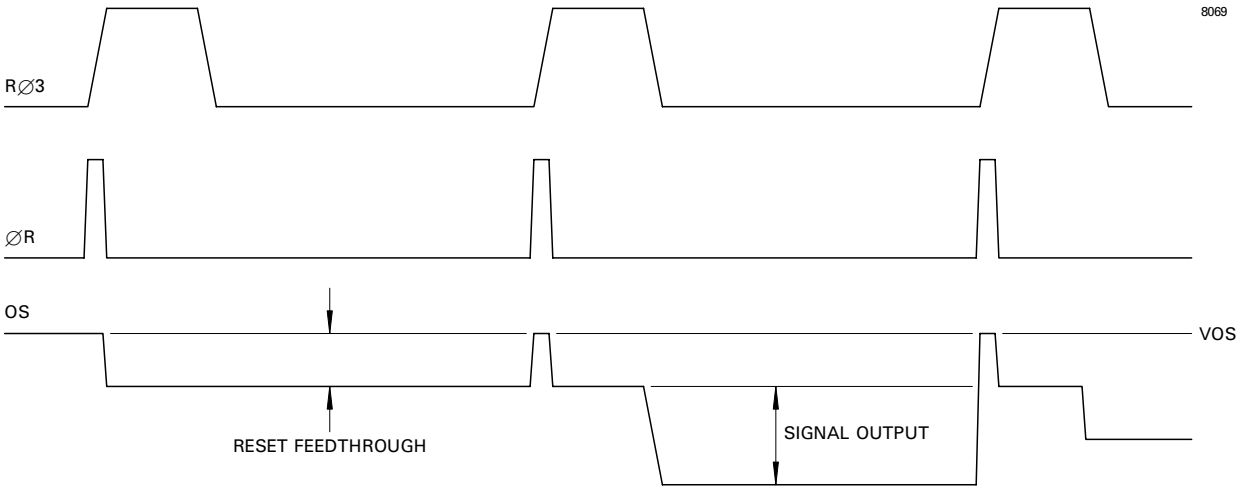


Figure 9: EXAMPLE FRAME TIMING DIAGRAM

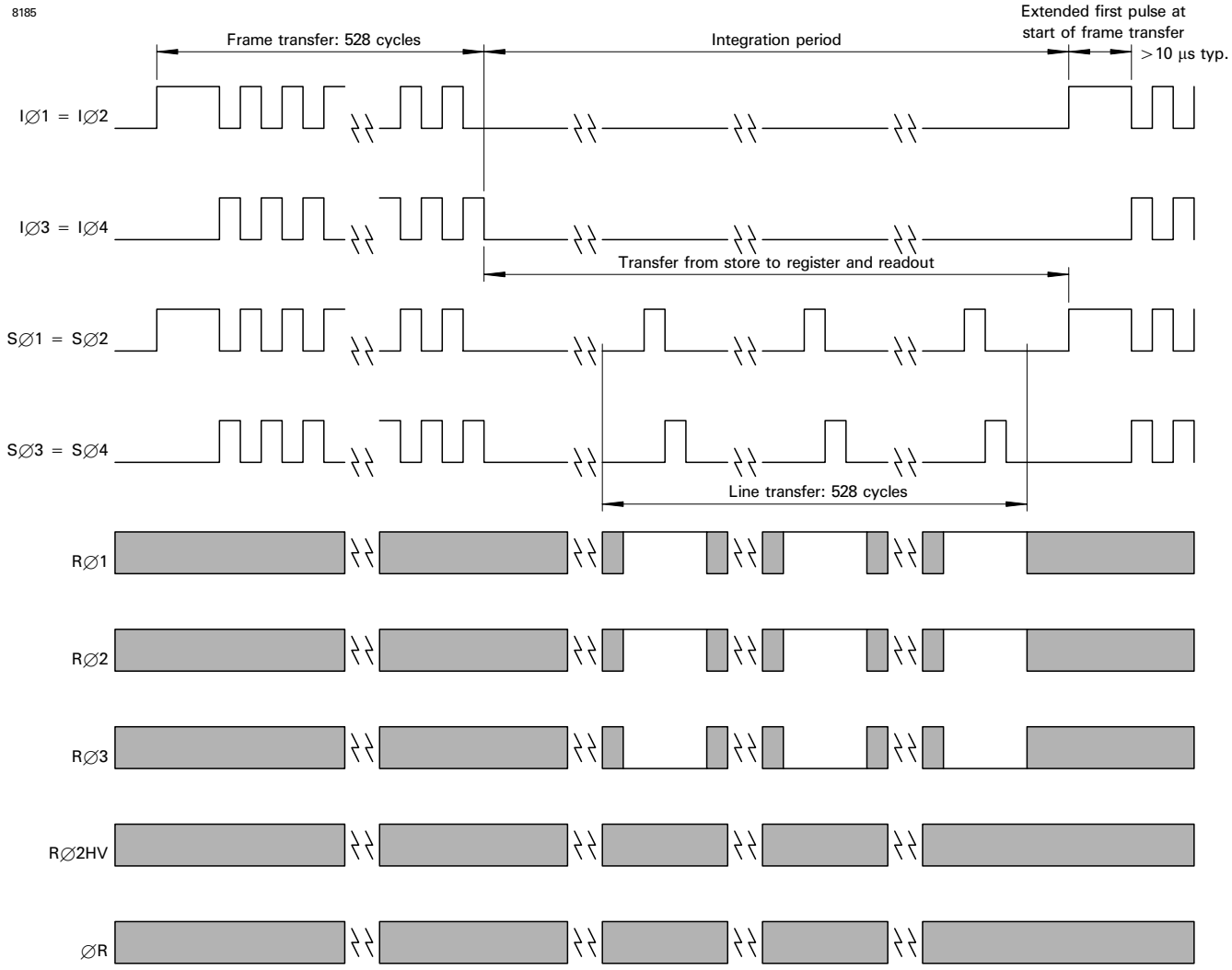


Figure 10: EXAMPLE LINE TIMING DIAGRAM (Operation through OSL, see notes 15 and 18)

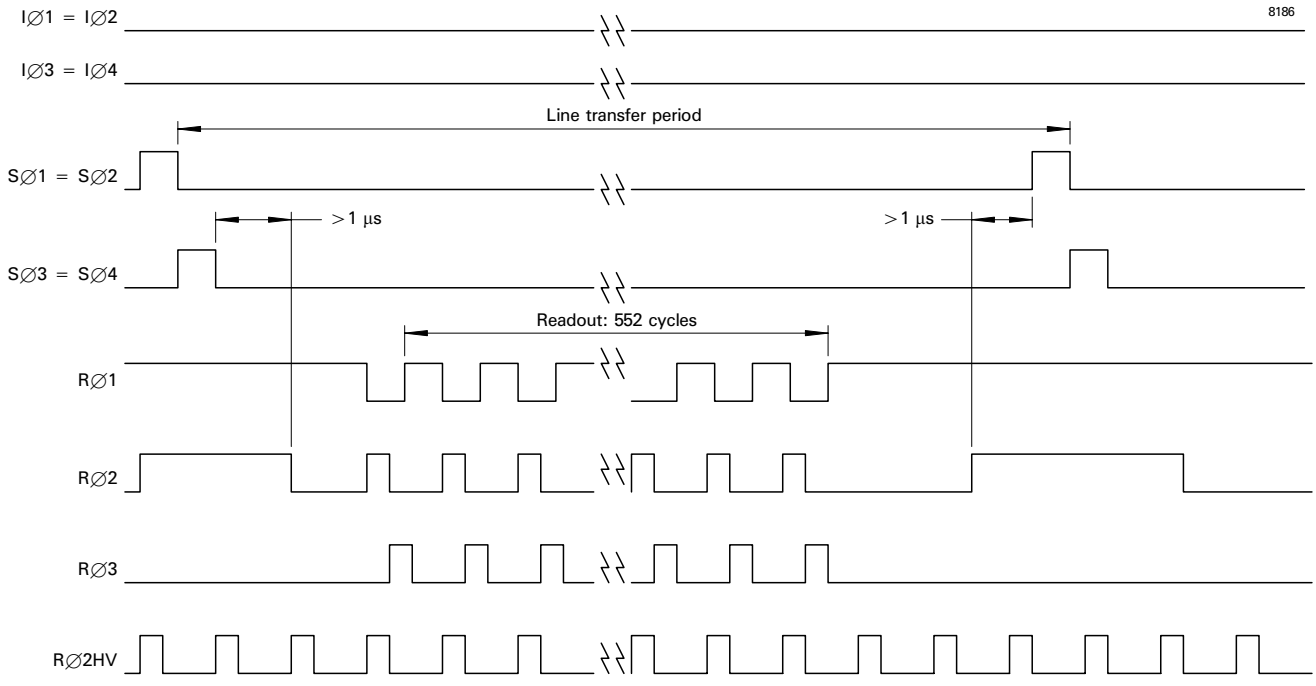
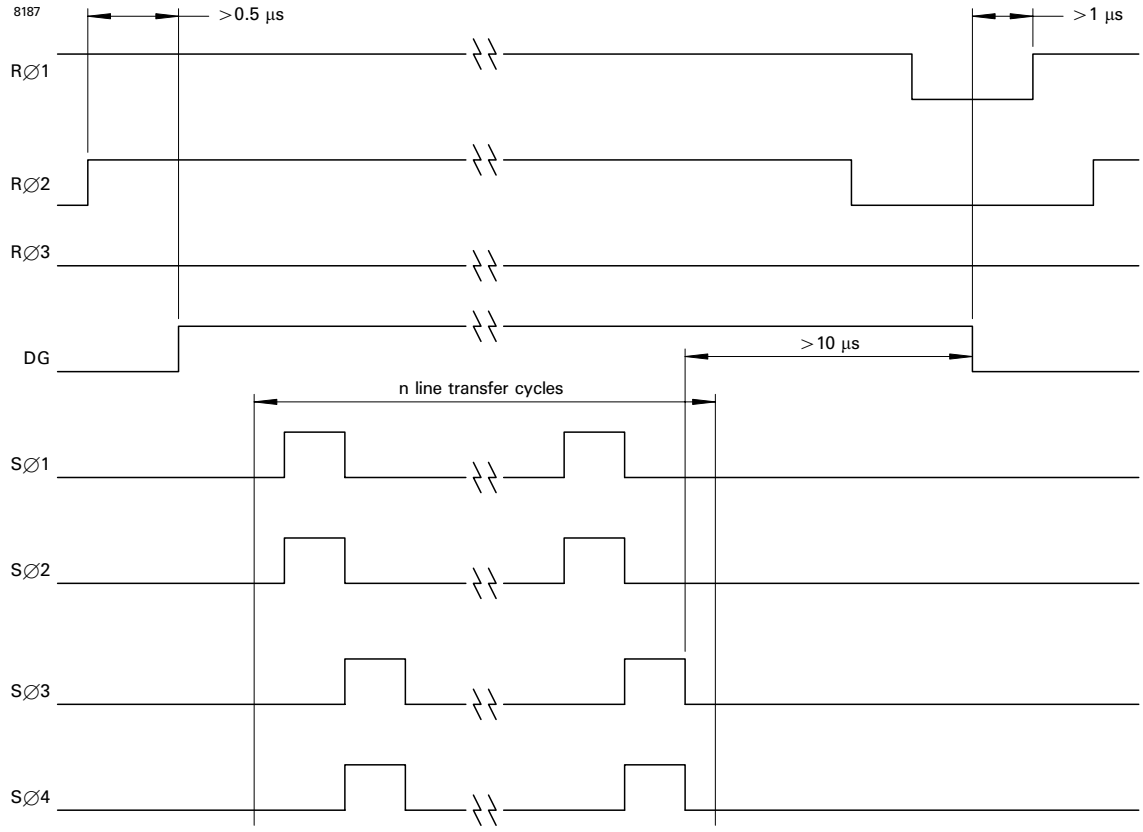


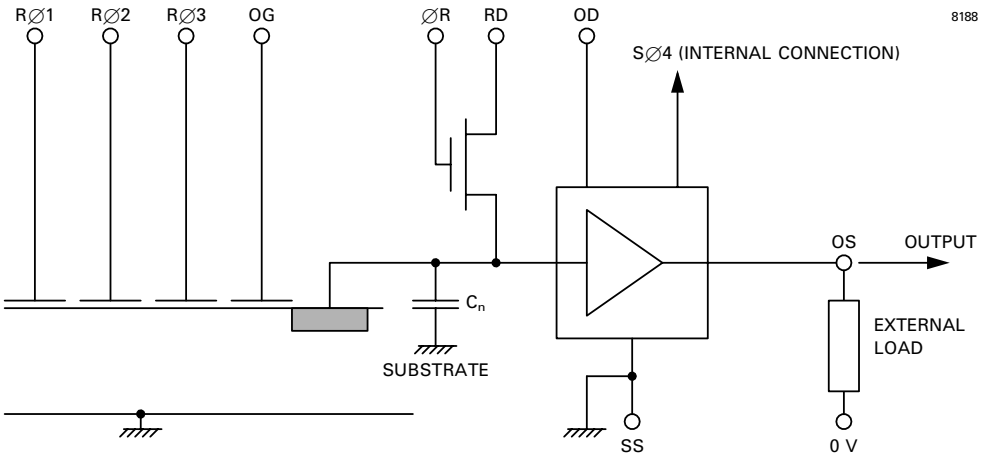
Figure 11: OPERATION OF THE DUMP GATE TO DUMP n LINES OF UNWANTED DATA FROM THE STANDARD REGISTER



NOTE

16. Wanted lines of data must be completely read out before dumping unwanted data.

Figure 12: OUTPUT CIRCUIT SCHEMATIC (OSL and OSH Amplifiers)



NOTE

17. The amplifiers have a DC restoration circuit that is internally activated whenever SØ4 is high.

Figure 13: SCHEMATIC CHIP DIAGRAM

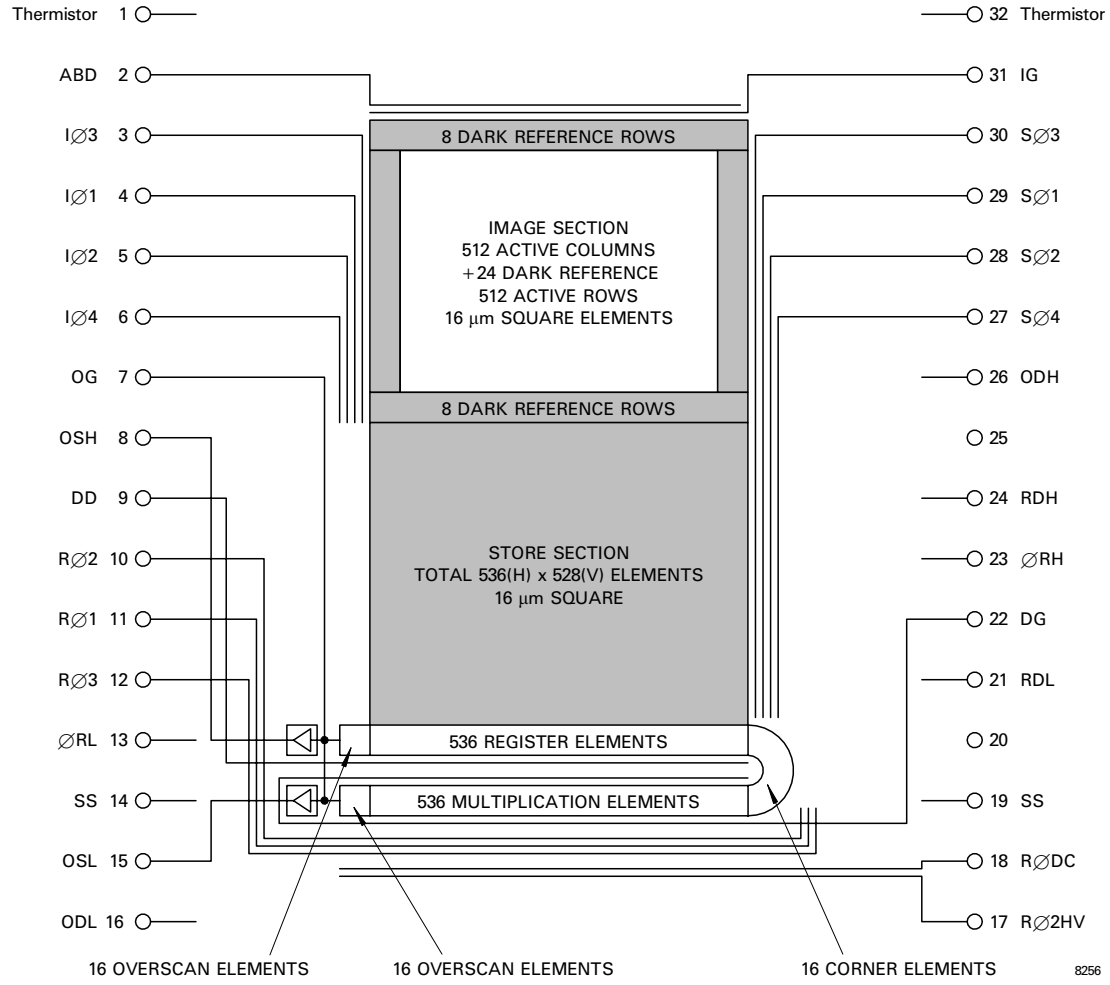
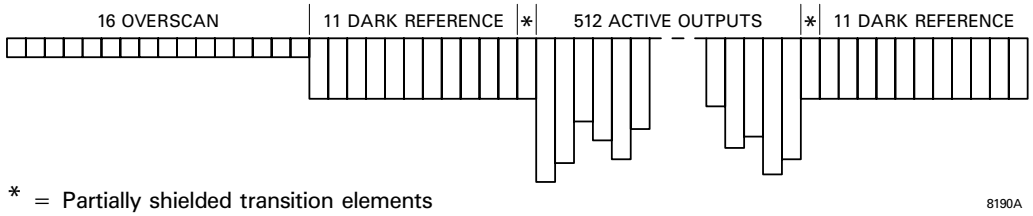


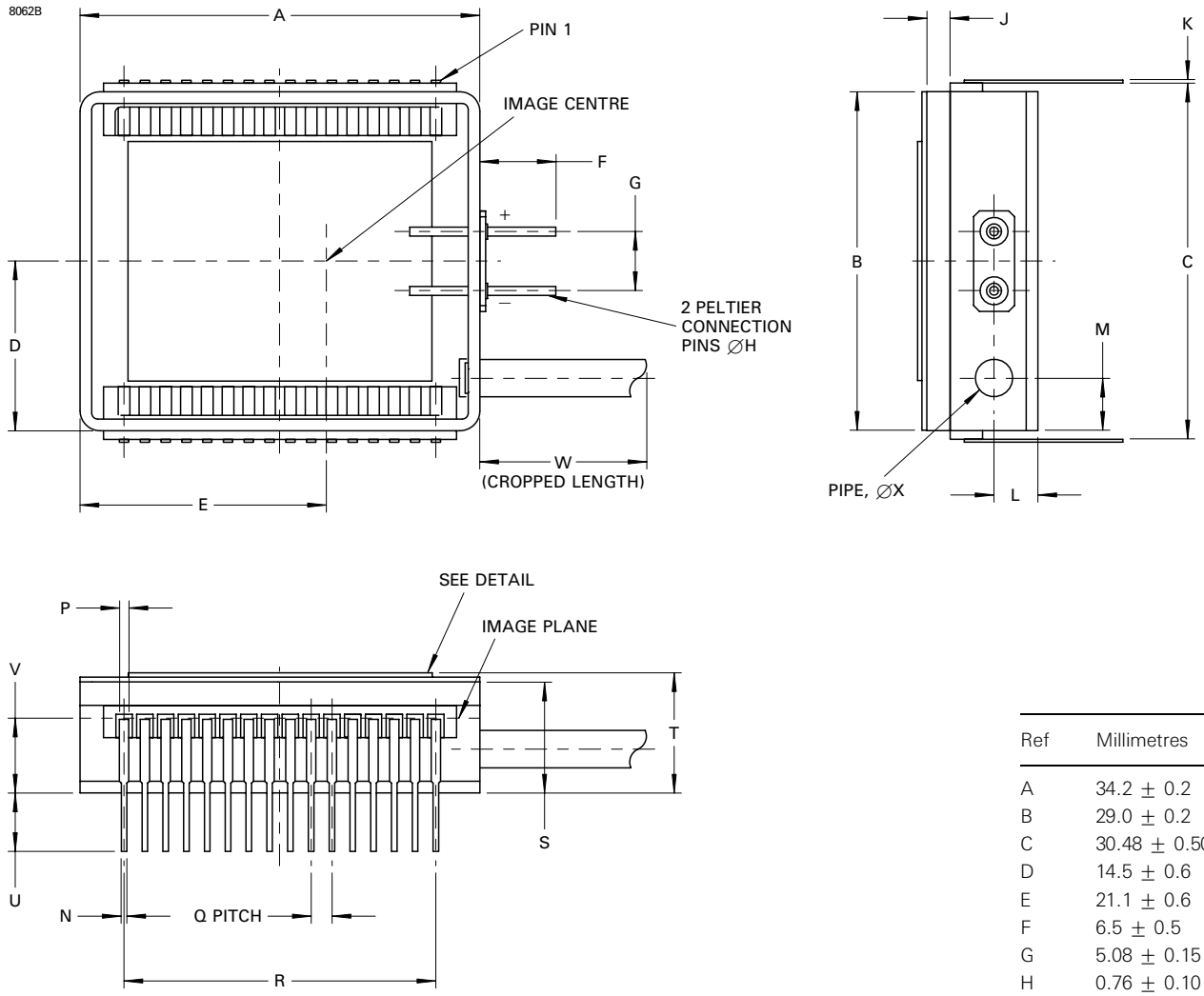
Figure 14: LINE OUTPUT FORMAT (for Example Line Timing Figure 10)



NOTE

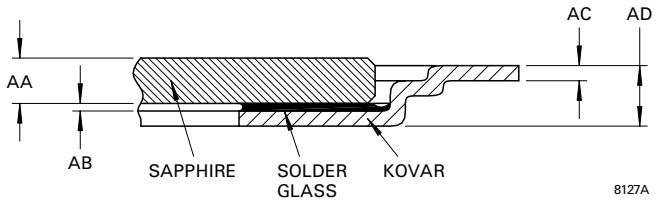
18. There is a 1-line propagation delay between transferring a line from the store section to the standard register and reading it out through the OSL output amplifier.

Figure 15: PACKAGE OUTLINE
(All dimensions without limits are nominal)



Ref	Millimetres
A	34.2 ± 0.2
B	29.0 ± 0.2
C	30.48 ± 0.50
D	14.5 ± 0.6
E	21.1 ± 0.6
F	6.5 ± 0.5
G	5.08 ± 0.15
H	0.76 ± 0.10
J	2.0 ± 0.2
K	0.25 ± 0.05
L	3.75 ± 0.25
M	4.5 ± 0.2
N	0.475 ± 0.075
P	0.8 ± 0.1
Q	1.778 ± 0.130
R	26.67
S	9.5 ± 0.2
T	9.9 ± 0.4
U	4.5 min
V	6.5 ± 0.4
W	13.0 max
X	3.200 ± 0.075
AA	0.9 ± 0.1
AB	0.10 ± 0.10
AC	0.25 ± 0.03
AD	1.25 ± 0.03

Detail of Window Bonding



Outline Notes

1. Package material Fe-Ni-Co alloy.
2. The device image area is parallel to the package back surface to within 100 μm typically.
3. The sapphire window is AR coated to give a total transmission that is typically >97% between 450 and 1000 nm.