Synchronous Buck PWM Controller

Features

- **Single 12V Power Supply Required**
- **0.6V Reference with 1% Accuracy**
- **Shutdown and Soft-Start Function**
- **Programmable Frequency Range from 50 kHz to 1000kHz**
- **Voltage Mode PWM Control Design**
- **Up to 100% Duty Cycle**
- **Over-Current Protection (OCP)**
- **SOP-14 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

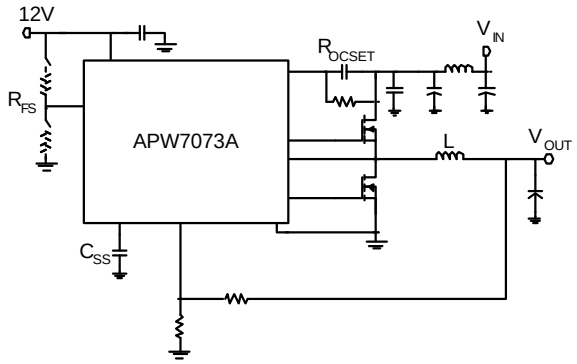
General Description

The APW7073A is a voltage mode and synchronous PWM controller which drives dual N-channel MOSFETs. The device integrates all of the controlling, monitoring, and protecting functions into a single package, and provides one controlled power output with over-current protection.

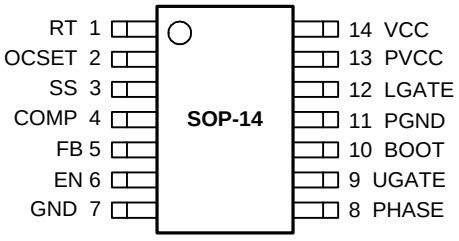
The APW7073A provides excellent regulation for output load variation. The internal 0.6V temperature-compensated reference voltage is designed to meet the requirement of low output voltage applications. The device includes a 200kHz free-running triangle-wave oscillator that is adjustable from 50kHz to 1000kHz.

The APW7073A has been equipped with excellent protection functions: Power-On-Reset (POR) and Over-Current Protection (OCP). The POR circuit can monitor the VCC, EN, and OCSET voltages to make sure the supply voltages exceed their threshold voltage while the controller is running. The OCP monitors the output current by using the voltage drop across the upper MOSFET's $R_{DS(ON)}$. When the output current reaches the trip point, the IC shuts off the converter and initiates a new soft-start process. After two over-current events are counted, the device turns off both high-side and low-side MOSFETs and the converter output is latched to be floating. It requires a POR of VCC to restart.

Typical Application Circuit



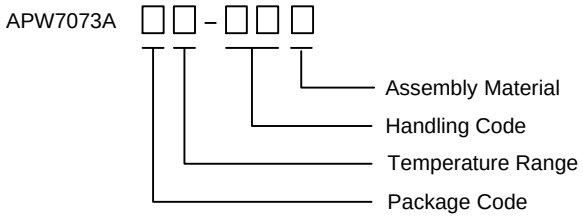
Pin Configuration



Applications

- **DC-DC Power Supply**

Ordering and Marking Information



Package Code
K : SOP - 14
Operating Ambient Temperature Range
E : -20 to 70°C
Handling Code
TR : Tape & Reel
Assembly Material
L : Lead Free Device G : Halogen and Lead Free Device

APW7073A K :

XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC}, V_{PVCC}	VCC, PVCC to GND	-0.3 to +16	V
V_{BOOT}	BOOT to PHASE	-0.3 to +16	V
V_{UGATE}	UGATE to PHASE <400ns pulse width >400ns pulse width	-5 to V_{BOOT} +5 -0.3 to V_{BOOT} +0.3	V
V_{LGATE}	LGATE to PGND <400ns pulse width >400ns pulse width	-5 to V_{PVCC} +5 -0.3 to V_{PVCC} +0.3	V
V_{PHASE}	PHASE to GND <400ns pulse width >400ns pulse width	-10 to +30 -0.3 to 16	V
V_{RT}, V_{OCSET}, V_{EN}	RT, OCSET, EN to GND	-0.3 to V_{CC}+0.3	V
V_{FB}, V_{COMP}, V_{SS}	FB, COMP, SS to GND	-0.3 to 7	V
V_{PGND}	PGND to GND	-0.3 to +0.3	V
T_J	Junction Temperature Range	-20 to 150	°C
T_{STG}	Storage Temperature	-65 to 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note 2)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance in Free Air SOP-14	160	°C/W

Note2: θ_{JA} is measured with the component mounted on a high effective the thermal conductivity test board in free air. The exposed pad of package is soldered directly on the PCB.

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{CC}, V_{PVCC}	IC Supply Voltage	10.8 to 13.2	V
V_{IN}	Converter Input Voltage	2.2 to 13.2	V
V_{OUT}	Converter Output Voltage	0.6 to 5	V
I_{OUT}	Converter Output Current	0 to 30	A
T_A	Ambient Temperature Range	-20 to 70	°C
T_J	Junction Temperature Range	-20 to 125	°C

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CC}=12V, and T_A=-20~70°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7073A			Unit
			Min.	Typ.	Max.	
INPUT SUPPLY CURRENT						
I_{CC}	VCC Supply Current (Shutdown Mode)	UGATE, LGATE and EN = GND	-	0.5	1	mA
	VCC Supply Current	UGATE and LGATE Open	-	5	10	mA
POWER-ON-RESET						
	Rising VCC Threshold		9	9.5	10.0	V
	Falling VCC Threshold		7.5	8	8.5	V
	Rising V_{OCSET} Threshold		-	1.3	-	V
	VOCSET Hysteresis Voltage		-	0.1	-	V
	Rising EN threshold Voltage		-	1.3	-	V
	EN Hysteresis Voltage		-	0.1	-	V
OSCILLATOR						
	Accuracy		-15	-	+15	%
F_{OSC}	Free Running Frequency	RT = open	-	200	-	kHz
	Adjustment Range	RT pin: resistor to GND; resistor to VCC	50	-	1000	kHz
V_{OSC}	Ramp Amplitude	(nominal 1.35V to 2.95V)	-	1.6	-	V
Duty	Duty Cycle Range		0	-	100	%
REFERENCE						
V_{REF}	Reference Voltage		-	0.60	-	V
	Reference Voltage Tolerance		-1	-	+1	%
PWM ERROR AMPLIFIER						
Gain	Open Loop Gain	R_L = 10k, C_L = 10pF (Note3)	-	88	-	dB
GBWP	Open Loop Bandwidth	R_L = 10k, C_L = 10pF (Note3)	-	15	-	MHz
SR	Slew Rate	R_L = 10k, C_L = 10pF (Note3)	-	6	-	V/µs
	FB Input Current	V_{FB} = 0.6V	-	0.1	1	µA
V_{COMP}	COMP High Voltage		-	5.5	-	V
V_{COMP}	COMP Low Voltage		-	0	-	V
I_{COMP}	COMP Source Current	V_{COMP} = 2V	-	5	-	mA
I_{COMP}	COMP Sink Current	V_{COMP} = 2V	-	5	-	mA

Electrical Characteristics (Cont.)

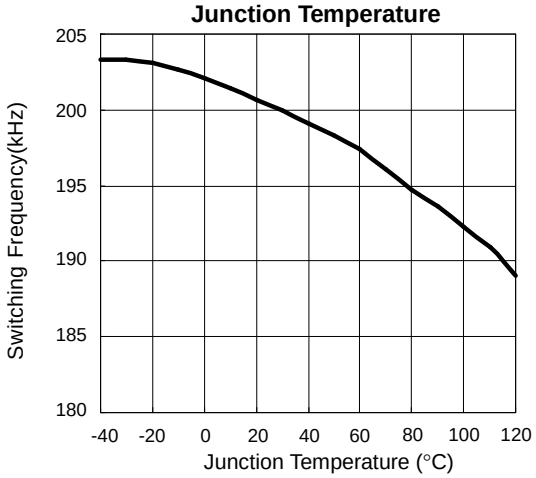
Unless otherwise specified, these specifications apply over V_{CC}=12V, and T_A=-20~70°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7073A			Unit
			Min.	Typ.	Max.	
GATE DRIVERS						
I_{UGATE}	Upper Gate Source Current	V_{BOOT} = 12V, V_{UGATE} -V_{PHASE} = 2V	-	2.6	-	A
R_{UGATE}	Upper Gate Sink Impedance	V_{BOOT} = 12V, I_{UGATE} = 0.1A	-	1.6	2.4	Ω
I_{LGATE}	Lower Gate Source Current	V_{PVCC} = 12V, V_{LGATE} = 2V	-	3.0	-	A
R_{LGATE}	Lower Gate Sink Impedance	V_{PVCC} = 12V, I_{LGATE} = 0.1A	-	1.25	1.88	Ω
T_D	Dead Time		-	50	-	ns
PROTECTION						
I_{OCSET}	OCSET Source Current	V_{OCSET} = 11.5V	170	200	250	µA
ENABLE/SOFT-START						
I_{SS}	Soft-Start Charge Current		24	30	36	µA

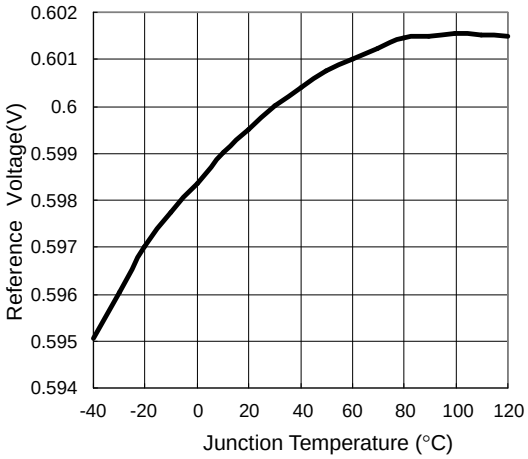
Note 3 : Guaranteed by design

Typical Operating Characteristics

Switching Frequency vs. Junction Temperature

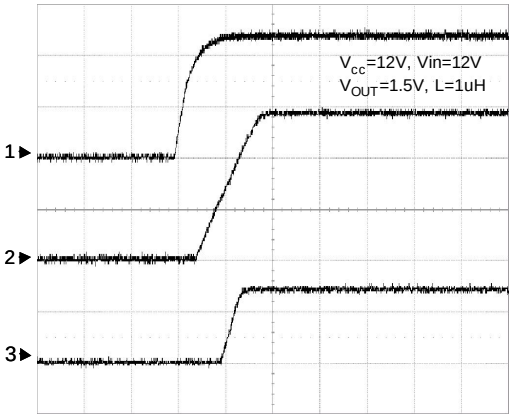


Reference Voltage vs. Junction Temperature



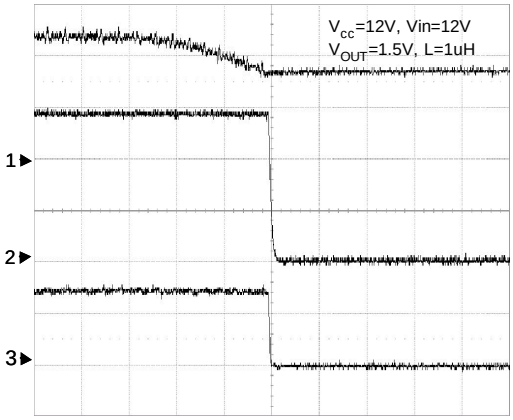
Operating Waveforms

Power On



CH1: V_{CC} (5V/div)
CH2: V_{SS} (2V/div)
CH3: V_{OUT} (1V/div)
Time: 10ms/div

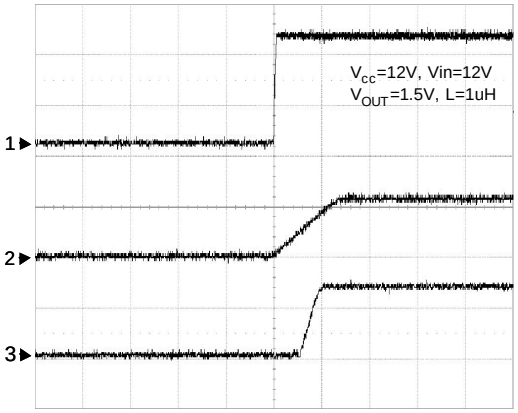
Power Off



CH1: V_{CC} (5V/div)
CH2: V_{SS} (2V/div)
CH3: V_{OUT} (1V/div)
Time: 2ms/div

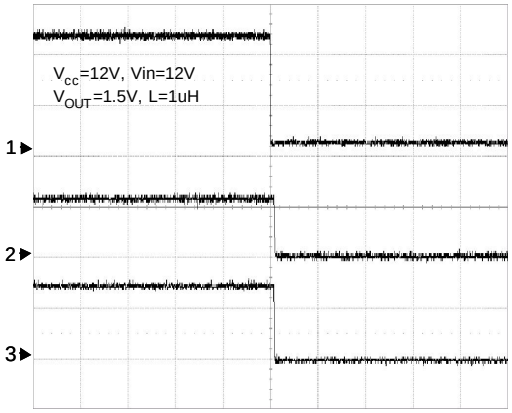
Operating Waveforms (Cont.)

EN (V_{EN}=V_{CC})



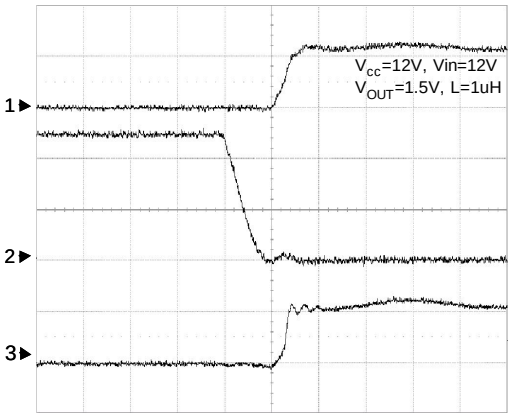
CH1: V_{EN} (5V/div)
CH2: V_{SS} (5V/div)
CH3: V_{OUT} (1V/div)
Time: 10ms/div

Shutdown (V_{EN}=V_{GND})



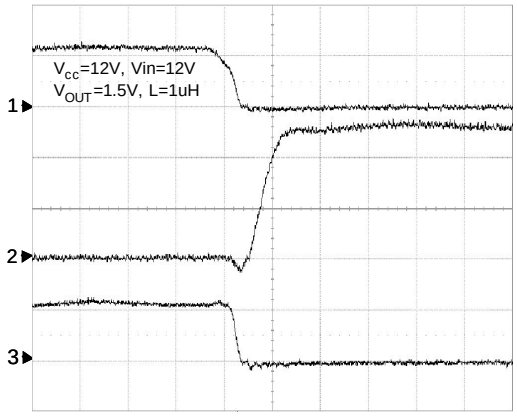
CH1: V_{EN} (5V/div)
CH2: V_{SS} (5V/div)
CH3: V_{OUT} (1V/div)
Time: 10ms/div

UGATE Rising



CH1: V_{UGATE} (20V/div)
CH2: V_{LGATE} (5V/div)
CH3: V_{PHASE} (10V/div)
Time: 50ns/div

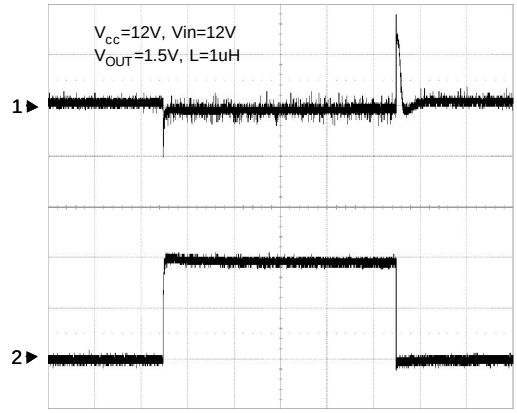
UGATE Falling



CH1: V_{UGATE} (20V/div)
CH2: V_{LGATE} (5V/div)
CH3: V_{PHASE} (10V/div)
Time: 50ns/div

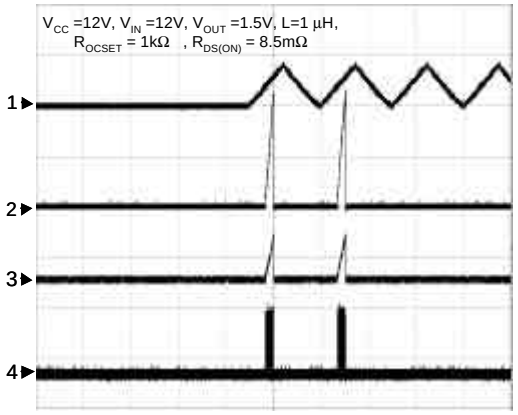
Operating Waveforms (Cont.)

Load Transient Response



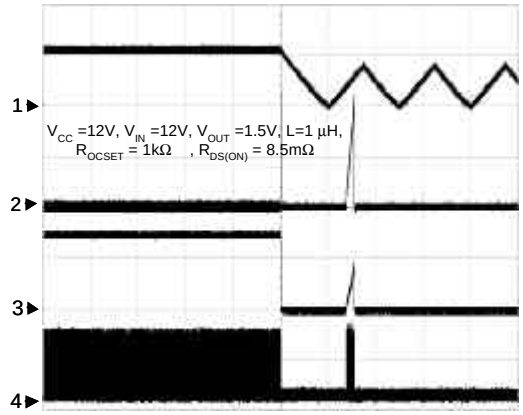
CH1: V_{OUT} (500mV/div)
CH4: I_{OUT} (5A/div)
Time: 200µs/div

Short Test before Power On



CH1: V_{SS} (5V/div)
CH2: I_L (10A/div)
CH3: V_{OUT} (1V/div)
CH4: V_{UGATE} (20V/div)
Time: 20ms/div

Short Test after Power On



CH1: V_{SS} (5V/div)
CH2: I_L (10A/div)
CH3: V_{OUT} (1V/div)
CH4: V_{UGATE} (20V/div)
Time: 20ms/div

Function Pin Description

VCC

Power supply input pin. Connect a nominal 12V power supply to this pin. The power-on-reset function monitors the input voltage by this pin. It is recommended that a decoupling capacitor (1 to 10μF) be connected to the GND for noise decoupling.

PVCC

This pin provides a supply voltage for the lower gate drive. Connect this pin to VCC pin in normal use.

BOOT

This pin provides the bootstrap voltage to the upper gate driver for driving the N-channel MOSFET.

PHASE

This pin is the return path for the upper gate driver. Connect this pin to the upper MOSFET source. This pin is also used to monitor the voltage drop across the MOSFET for over-current protection.

GND

This pin is the signal ground pin. Connect the GND to a good ground plane.

PGND

This pin is the power ground pin for the lower gate driver. It should be tied to the GND on the board.

COMP

This pin is the output of PWM error amplifier. It is used to set the compensation components.

FB

This pin is the inverting input of the PWM error amplifier. It is used to set the output voltage and the compensation components.

UGATE

This pin is the gate driver for the upper MOSFET of PWM output.

LGATE

This pin is the gate driver for the lower MOSFET of PWM output.

SS

Connect a capacitor to the GND and a 30μA current source charges this capacitor to set the soft-start time.

OCSET

This pin serves two functions: a shutdown control and the setting of over current limit threshold. Pulling this pin below 1.3V will shutdown the controller, forcing the UGATE and LGATE signals to be low.

A resistor (Rocset) connected between this pin and the drain of the high side MOSFET will determine the over current limit. An internal 200μA current source will flow through this resistor, creating a voltage drop, which will be compared with the voltage across the high side MOSFET. The threshold of the over current limit is therefore given by:

$$I_{PEAK} = \frac{I_{OCSET}(200uA) \times R_{OCSET}}{R_{DS(ON)}}$$

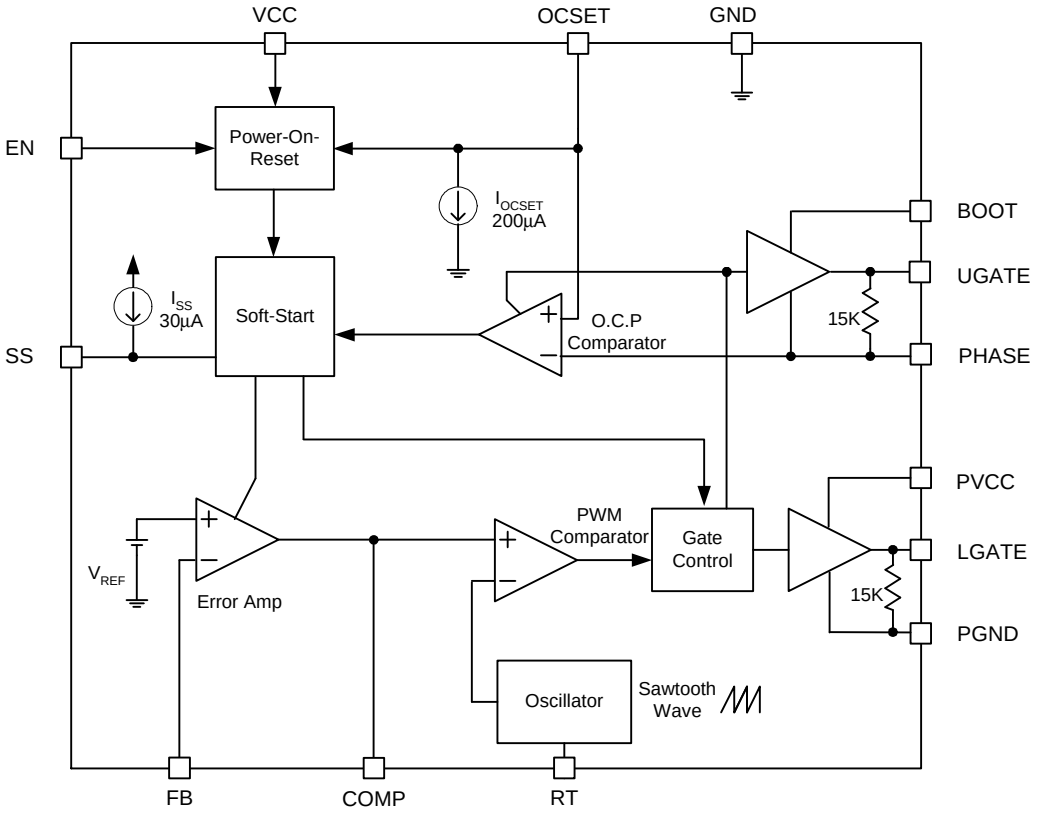
EN

Pull this pin above 1.3V to enable the device and pull this pin below 1.2V to disable the device. In shutdown, the SS is discharged and the UGATE and LGATE pins are held low. Note that don't leave this pin open.

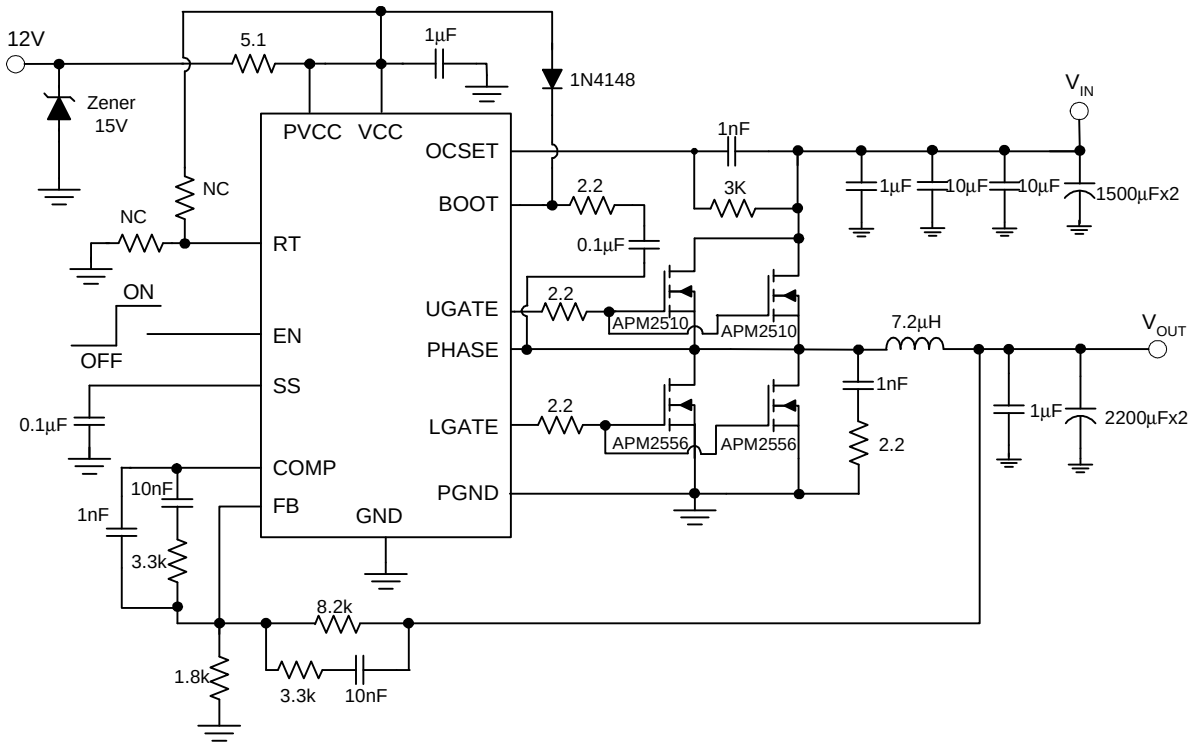
RT

This pin allows adjusting the switching frequency. Connect a resistor from RT pin to the ground to increase the switching frequency. Conversely, connect a resistor from RT to the VCC to decrease the switching frequency.

Block Diagram



Typical Application Circuit



Function Description

Power-On-Reset (POR)

The Power-On-Reset (POR) function of APW7073A continually monitors the input supply voltage (V_{CC}), the enable (EN) pin, and the OCSET pin. The supply voltage (V_{CC}) must exceed its rising POR threshold voltage. The voltage at OCSET pin is equal to V_{IN} less a fixed voltage drop (V_{OCSET} = V_{IN}- V_{ROCSET}). The EN pin can be pulled high with connecting a resistor to the VCC. The POR function initiates soft-start operation after VCC, EN, and OCSET voltages exceed their POR thresholds. For operation with a single +12V power source, V_{IN} and V_{cc} are equivalent and the +12V power source must exceed the rising VCC threshold. The POR function inhibits operation at disabled status (EN pin low). With both input supplies above their POR thresholds, the device initiates a soft-start interval.

Soft-Start/EN

The SS/EN pins control the soft-start and enable or disable the controller. Connect a soft-start capacitor from SS pin to GND to set the soft-start interval. Figure1. shows the soft-start interval. When V_{CC} reaches its Power-On-Reset threshold (9.5V), internal 30µA current source starts to charge the capacitor. When the V_{SS} reaches the enabled threshold about 1.8V, the internal 0.6V reference starts to rise and follows the V_{SS}; the error amplifier output (V_{COMP}) suddenly raises to 1.35V, which is the valley of the triangle wave of the oscillator, leads the V_{OUT} to start-up. Until the V_{SS} reaches about 4.2V, the internal reference completes the soft-start interval and reaches to 0.6V, and then V_{OUT} is in regulation. The SS still rises to 5.5V and then stops.

$$T_{Soft-Start} = t_2 - t_1 = \frac{C_{SS}}{I_{SS}} \cdot 2.4V$$

Where:

C_{SS} = external Soft-Start capacitor

I_{SS} = Soft-Start current=30µA

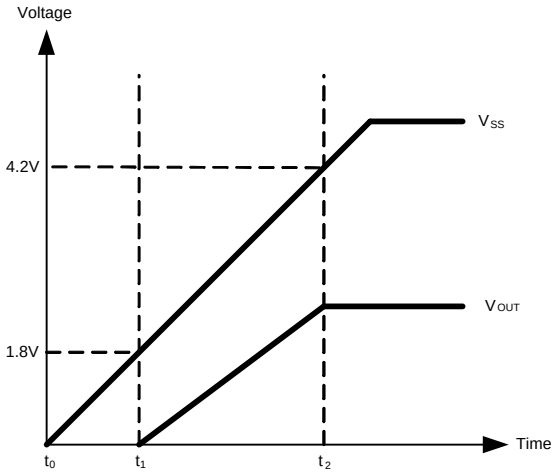


Figure 1. Soft-Start Internal

Over-Current Protection (monitor upper MOSFET)

The APW7073A monitors the voltage across the upper MOSFET and uses the OCSET pin to set the over-current trip point.

A resistor (R_{OCSET}) connected between OCSET pin and the drain of the upper MOSFET will determine the over current limit. An internal 200µA current source will flow through this resistor, creating a voltage drop, which will be compared with the voltage across the upper MOSFET. When the voltage across the upper MOSFET exceeds the voltage drop across the R_{OCSET}, an over-current will be detected. The threshold of the over current limit is therefore given by:

$$I_{LIMIT} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}}$$

For the over-current, it is never occurred in the normal operating load range; the variation of all parameters in the above equation should be determined.

- The MOSFET's $R_{DS(ON)}$ is varied by temperature and gate to source voltage, the user should determine the maximum $R_{DS(ON)}$ in manufacturer's datasheet.

- The minimum I_{OCSET} (170µA) and minimum R_{OCSET} should be used in the above equation.

- Note that the I_{LIMIT} is the current flow through the upper MOSFET; I_{LIMIT} must be greater than maximum output current add the half of inductor ripple current.

Function Description (Cont.)

Over-Current Protection (Cont.)

An over current condition will shut down the device and discharge the C_{SS} with a 30μA sink current and then initiate the soft-start sequence. After two over-current events are counted, the device turns off both high-side and low-side MOSFETs and the converter output is latched to be floating. It requires a POR of VCC to restart.

Switching Frequency

The APW7073A provides the oscillator switching frequency adjustment. The device includes a 200kHz free-running triangle wave oscillator. If operating in higher frequency than 200kHz, connect a resistor from RT pin to the ground to increase the switching frequency. Conversely, if operating in lower frequency than 200kHz, connect a resistor from RT to the VCC to decrease the switching frequency.

Figure 2. shows how to select the resistor for the desired frequency. Figure 3 shows more detail for the higher frequencies and Figure 4 shows the lower frequency detail.

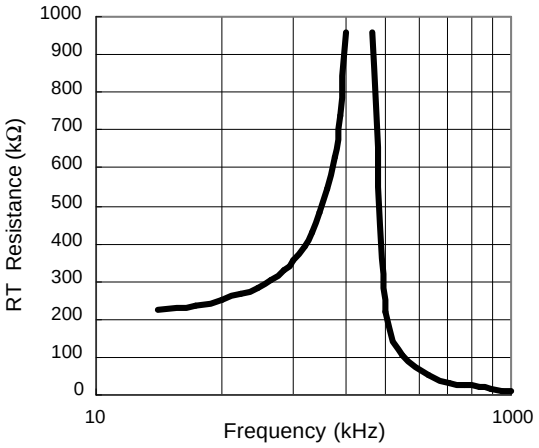


Figure 2. Oscillator Frequency vs. RT Resistance

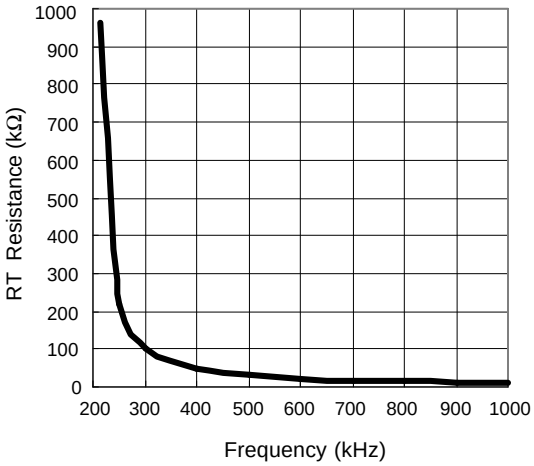


Figure 3. Oscillator Frequency vs. RT Resistance (High Frequency)

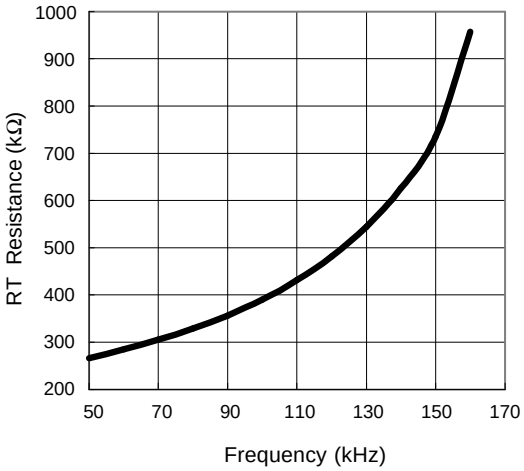


Figure 4. Oscillator Frequency vs. RT Resistance (Low Frequency)

Application Information

Output Voltage Selection

The output voltage can be programmed with a resistive divider. Use 1% or better resistors for the resistive divider is recommended. The FB pin is the inverter input of the error amplifier, and the reference voltage is 0.6V. The output voltage is determined by:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{OUT}}{R_{GND}}\right)$$

Where R_{OUT} is the resistor connected from V_{OUT} to FB, and R_{GND} is the resistor connected from FB to GND.

Output Inductor Selection

The inductor value determines the inductor ripple current and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

$$\Delta V_{OUT} = I_{RIPPLE} \times ESR$$

where Fs is the switching frequency of the regulator.

Although increase of the inductor value and frequency reduces the ripple current and voltage, a tradeoff will exist between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_S) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFET and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

Output Capacitor Selection

Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In some applications, multiple capacitors have to be parallelled to achieve the desired ESR value. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors also must be considered. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer. For high frequency decoupling, a ceramic capacitor 1µF can be connected between the drain of upper MOSFET and the source of lower MOSFET.

MOSFET Selection

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reverse transfer capacitance (C_{RSS}) and maximum output current requirement. There are two components of loss in the MOSFETs: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following equations:

$$P_{UPPER} = I_{OUT}^{\ 2}(1 + TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_S$$

$$P_{LOWER} = I_{OUT}^{\ 2}(1 + TC)(R_{DS(ON)})(1-D)$$

Where I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_S is the switching frequency

t_{SW} is the switching interval

D is the duty cycle

Application Information (Cont.)

MOSFET Selection (Cont.)

Note that both MOSFETs have conduction loss while the upper MOSFET includes an additional transition loss. The switching internal, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is to factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

PWM Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network among COMP, FB, and V_{OUT} should be added. The compensation network is shown in Figure 8. The output LC filter consists of the output inductor and output capacitors. The transfer function of the LC filter is given by:

$$F_{ESR} = \frac{1}{2\times\pi\times ESR\times C_{OUT}}$$

The F_{LC} is the double poles of the LC filter, and F_{ESR} is the zero introduced by the ESR of the output capacitor.

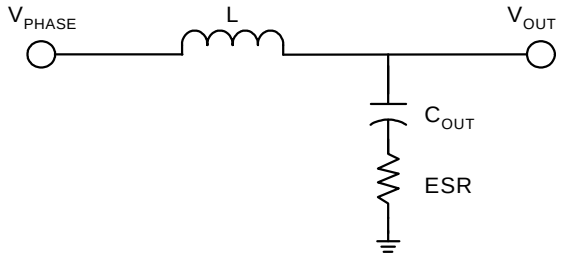


Figure 5. The Output LC Filter

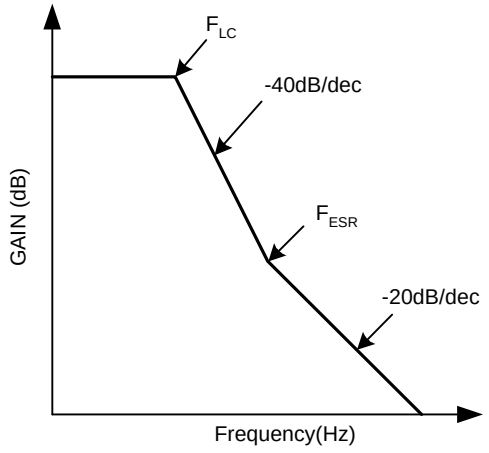


Figure 6. The LC Filter GAIN and Frequency

The PWM modulator is shown in Figure 7. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

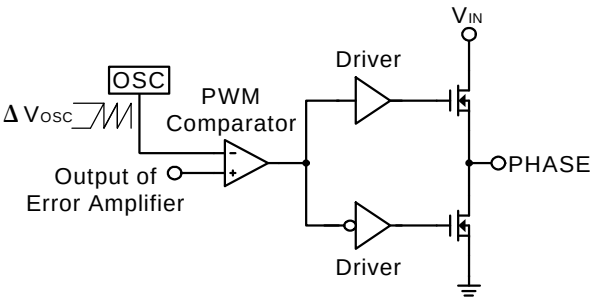


Figure 7. The PWM Modulator

The compensation network is shown in Figure 8. It provides a close loop transfer function with the highest zero crossover frequency and sufficient phase margin. The transfer function of error amplifier is given by:

$$GAIN_{AMP} = \frac{V_{COMP}}{V_{OUT}} = \frac{\frac{1}{sC1}//\left(R2+\frac{1}{sC2}\right)}{R1//\left(R3+\frac{1}{sC3}\right)}$$

$$= \frac{R1+R3}{R1\times R3\times C1}\times\frac{\left(s+\frac{1}{R2\times C2}\right)\times\left(s+\frac{1}{(R1+R3)\times C3}\right)}{s\left(s+\frac{C1+C2}{R2\times C1\times C2}\right)\times\left(s+\frac{1}{R3\times C3}\right)}$$

The poles and zeros of the transfer function are:

$$F_{Z1} = \frac{1}{2\times\pi\times R2\times C2}$$

$$F_{Z2} = \frac{1}{2\times\pi\times(R1+R3)\times C3}$$

$$F_{P1} = \frac{1}{2\times\pi\times R2\times\left(\frac{C1\times C2}{C1+C2}\right)}$$

$$F_{P2} = \frac{1}{2\times\pi\times R3\times C3}$$

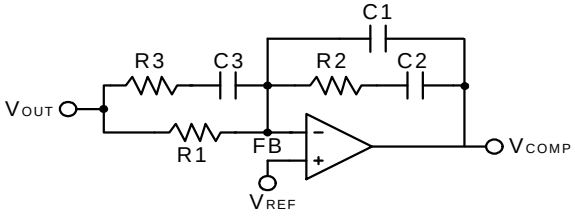


Figure 8. Compensation Network

Application Information (Cont.)

PWM Compensation (Cont.)

The closed loop gain of the converter can be written as:

$$GAIN_{LC} X\, GAIN_{PWM} X\, GAIN_{AMP}$$

Figure 9. shows the asymptotic plot of the closed loop converter gain, and the following guidelines will help to design the compensation network. Using the below guidelines should give a compensation similar to the curve plotted. A stable closed loop has a -20dB/ decade slope and a phase margin greater than 45 degree.

1. Choose a value for R1, usually between 1K and 5K.

2. Select the desired zero crossover frequency

$$F_O: (1/5 \sim 1/10)\ X\ F_S > F_O > F_{ESR}$$

Use the following equation to calculate R2:

$$R2 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_O}{F_{LC}} \times R1$$

3. Place the first zero F_{Z1} before the output LC filter double pole frequency F_{LC}.

$$F_{Z1} = 0.75\ X\ F_{LC}$$

Calculate the C2 by the equation:

$$C2 = \frac{1}{2 \times \pi \times R2 \times F_{LC} \times 0.75}$$

4. Set the pole at the ESR zero frequency F_{ESR}:

$$F_{P1} = F_{ESR}$$

Calculate the C1 by the equation:

$$C1 = \frac{C2}{2 \times \pi \times R2 \times C2 \times F_{ESR} - 1}$$

5. Set the second pole F_{P2} at the half of the switching frequency and also set the second zero F_{Z2} at the output LC filter double pole F_{LC}. The compensation gain should not exceed the error amplifier open loop gain, check the compensation gain at F_{P2} with the capabilities of the error amplifier.

$$F_{P2} = 0.5\ X\ F_S$$

$$F_{Z2} = F_{LC}$$

Combine the two equations will get the following component calculations:

$$GAIN_{LC} = \frac{1 + s \times ESR \times C_{OUT}}{s^2 \times L \times C_{OUT} + s \times ESR \times C_{OUT} + 1}$$

The poles and zero of this transfer functions are:

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

$$R3 = \frac{R1}{\frac{F_S}{2 \times F_{LC}} - 1}$$

$$C3 = \frac{1}{\pi \times R3 \times F_S}$$

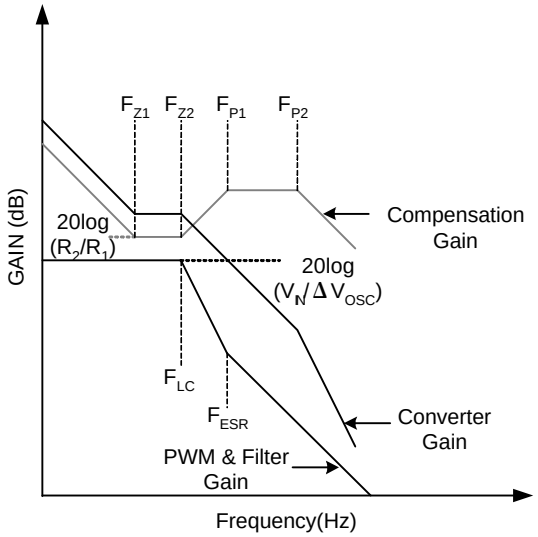


Figure 9. Converter Gain and Frequency

Layout Consideration

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at 300kHz, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is free-wheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short, wide, and printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separating till combined using ground plane construction or single point grounding. Figure 10 illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed lose together. Below is a checklist for your layout:

- Keep the switching nodes (UGATE, LGATE, and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible.

- The traces from the gate drivers to the MOSFETs (UGATE, LGATE) should be short and wide.

- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.

- Decoupling capacitor, compensation component, the resistor dividers, boot capacitors, and SS capacitors should be close their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placed near the drain).

- The input capacitor should be near the drain of the upper MOSFET; the output capacitor should be near the loads. The input capacitor GND should be close to the output capacitor GND and the lower MOSFET GND.

- The drain of the MOSFETs (V_{IN} and PHASE nodes) should be a large plane for heat sinking.

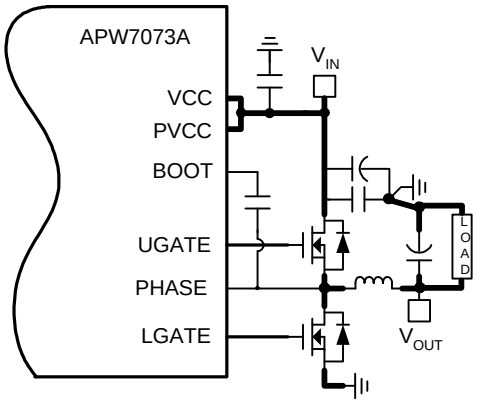
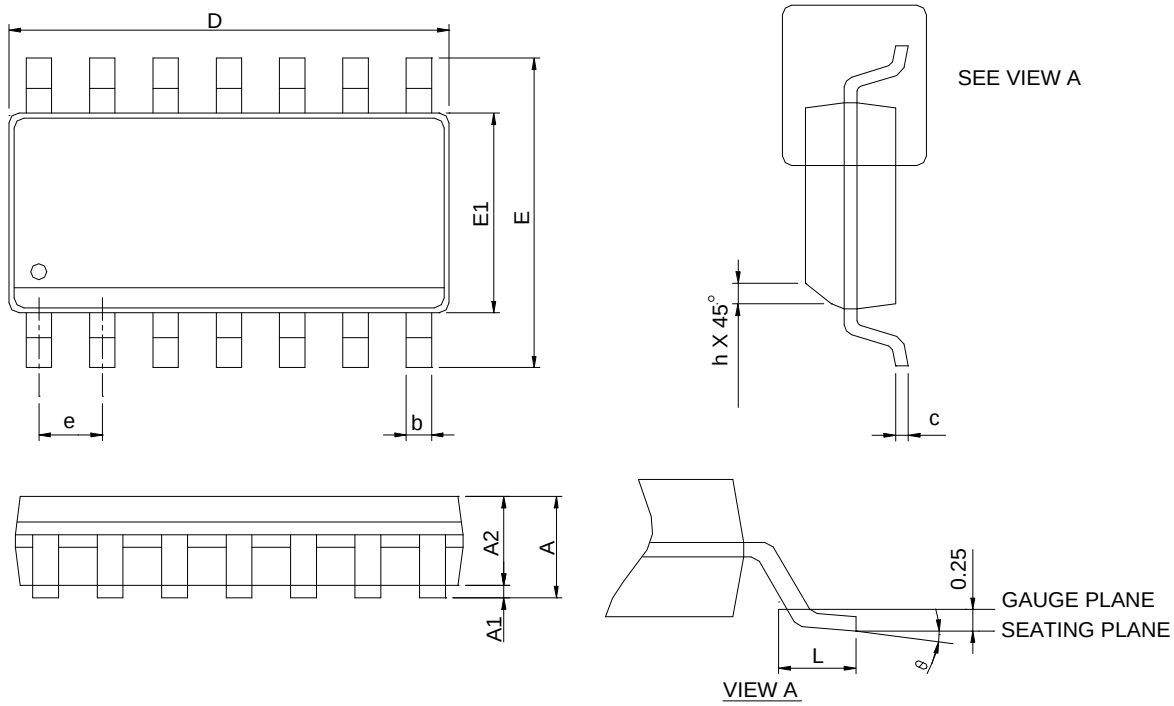


Figure 10. Layout Guidelines

Package Information

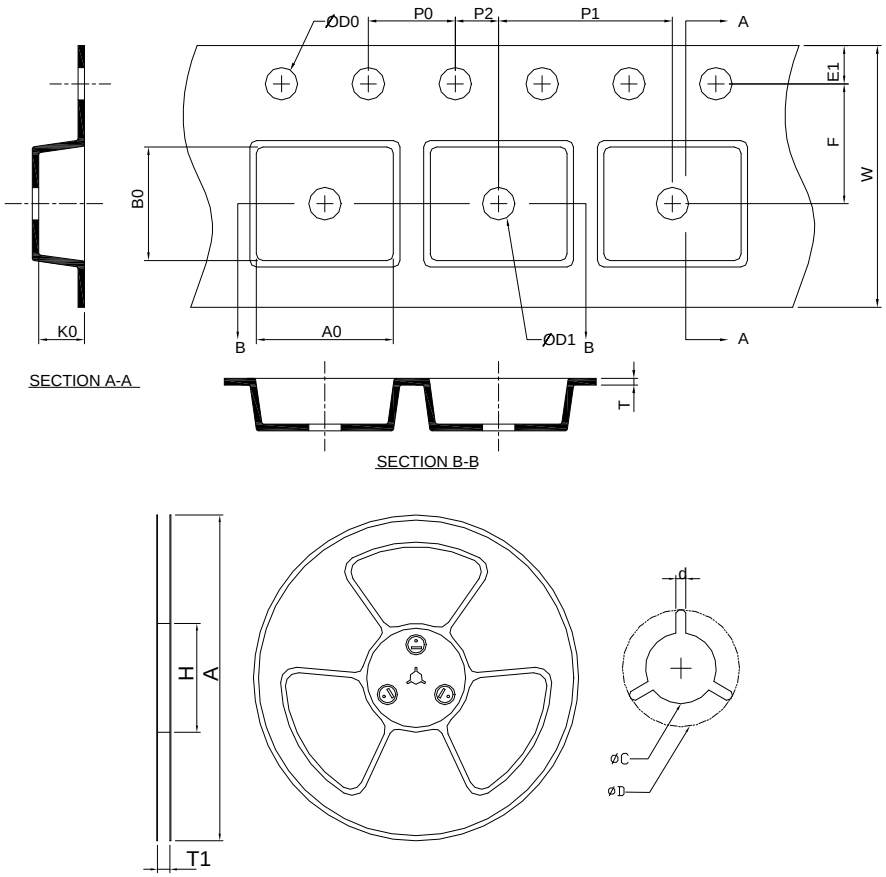
SOP–14



SYMBOL	SOP-14			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	8.55	8.75	0.337	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AB.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-14	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.50±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	9.00±0.20	2.10±0.20

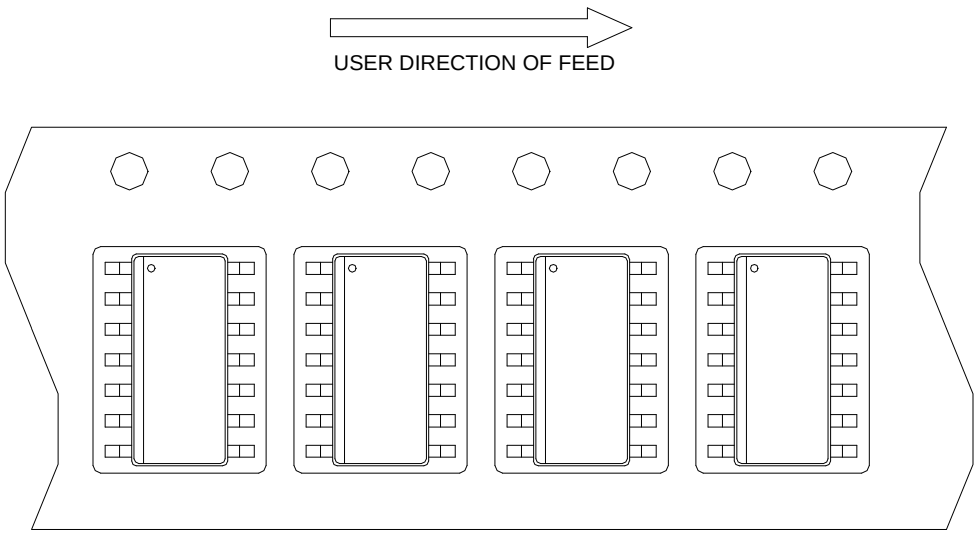
(mm)

Devices Per Unit

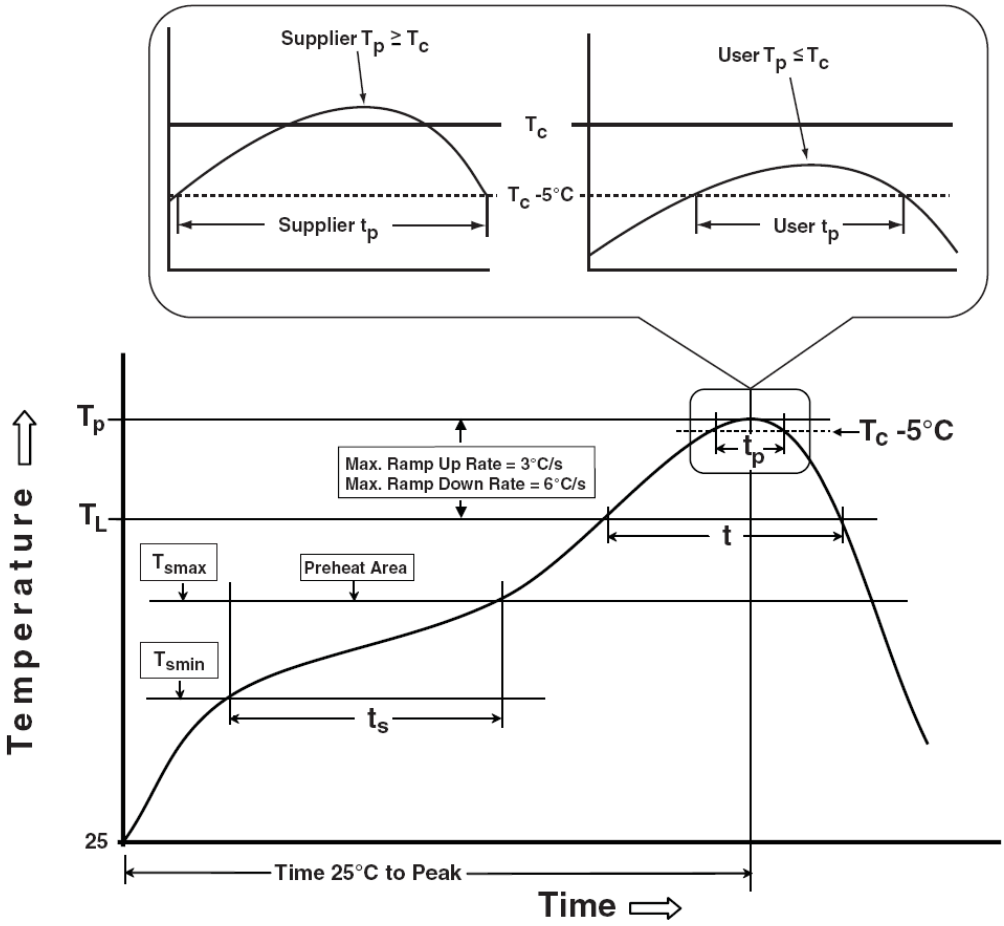
Package Type	Unit	Quantity
SOP- 14	Tape & Reel	2500

Taping Direction Information

SOP–14



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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