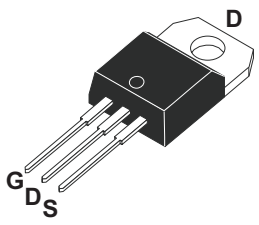
N-Channel Power MOSFET
(63A, 55Volts)

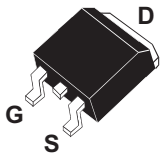
DESCRIPTION

The Nell **65N06** is a three-terminal silicon device with current conduction capability of 63A, fast switching speed, low on-state resistance, breakdown voltage rating of 55V, and max. threshold voltage of 4 volts.

They are designed as an extremely efficient and reliable device and has integral zener giving diodes ESD protection up to 2KV. They are intended for use in DC to DC convertors and general purpose switching applications.



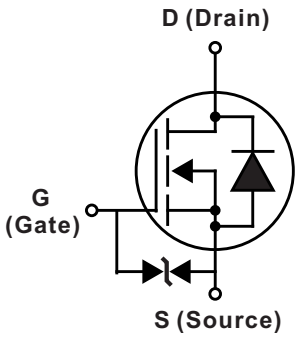
TO-220AB
(65N06A)



TO-263 (D^2PAK)
(65N06H)

FEATURES

- $R_{DS(ON)}$ = 18mΩ@V_{GS} = 10V
- Ultra low gate charge(40nC typical)
- Low reverse transfer capacitance (C_{RSS} = 170pF typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 175°C operation temperature



PRODUCT SUMMARY	
I_D (A)	63
V_{DSS} (V)	60
$R_{DS(ON)}$ (Ω)	0.018 @ V_{GS} = 10V
Q_G(nC) typ.	40

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT
V_{DSS}	Drain to Source voltag	T_J=25°C to 150°C	55	V
V_{DGR}	Drain to Gate voltage	R_{GS}=20KΩ	55	
V_{GS}	Gate to Source voltage		±20	
I_D	Continous Drain Current	V_{GS}=10V , T_C=25°C	63	A
		V_{GS}=10V , T_C=100°C	44	
I_{DM}	Pulsed Drain current(Note 1)		240	
dv/dt	Peak diode recovery dv/dt(Note 2)		7.0	V /ns
P_D	Total power dissipation	T_C=25°C	150	W
	Derating factor above 25°C		1.0	W/°C
V_C	Electro-static Discharge capacitor voltage, all pins	Human body model (100 pF, 1.5KΩ)	2	KV
T_J	Operation junction temperature		-55 to 175	°C
T_{STG}	Storage temperature		-55 to 175	
T_L	Maximum soldering temperature, for 10 seconds	1.6mm from case	300	
	Mounting torque, #6-32 or M3 screw		10 (1.1)	lbf·in (N·m)

Note: 1.Repetitive rating: pulse width limited by junction temperature.
2.I_{SD} ≤ 50A, di/dt ≤ 300A/us, V_{DD} ≤ $V_{(BR)DSS}$, starting T_J=25°C.

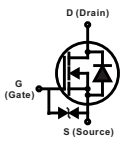
THERMAL RESISTANCE

SYMBOL	PARAMETER	Min.	Typ.	Max.	UNIT
$R_{th(j-c)}$	Thermal resistance, junction to case			1.05	
$R_{th(c-s)}$	Thermal resistance, case to heatsink		0.50		°C/W
$R_{th(j-a)}$	Thermal resistance, junction to ambient			62.5	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS		Min.	Typ.	Max.	UNIT
$V_{(BR)DSS}$	Drain to source breakdown voltage	V_{GS}=0V, I_D=250μA		55			V
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown voltage temperature coefficient	I_D = 250μA, referenced to 25°C			0.07		V/°C
I_{DSS}	Drain to source leakage current	V_{DS}=60V, V_{GS}=0V	T_C = 25°C			5	μA
			T_C=150°C			250	
I_{GSS}	Gate to source forward leakage current	V_{GS} = -20V, V_{DS} = 0V				100	nA
	Gate to source reverse leakage current	V_{GS} = 20V, V_{DS} = 0V				-100	
$R_{DS(ON)}$	Static drain to source on-state resistance	V_{GS}=10V, I_D=25A (Note 1)			15	18	mΩ
$V_{GS(TH)}$	Gate threshold voltage	V_{GS}=V_{DS}, I_D=1000μA		2		4	V
g_{fs}	Forward transconductance	V_{DS}=25V, I_D=25A		6	30		
C_{ISS}	Input capacitance	V_{DS} = 25V, V_{GS} = 0V, f =1MHz			1500	2000	pF
C_{OSS}	Output capacitance				370	470	
C_{RSS}	Reverse transfer capacitance				170	250	
$t_{d(ON)}$	Turn-on delay time	V_{DD} = 30V, I_D = 25A, R_G=10Ω V_{GS}=10V (Note 1)			15	25	ns
t_r	Rise time				30	60	
$t_{d(OFF)}$	Turn-off delay time				35	50	
t_f	Fall time				25	40	
L_D	Internal drain inductance	Between lead, 6mm form package and center of die			4.5		nH
L_S	Internal source inductance				7.5		
Q_G	Total gate charge	V_{DS} = 44V, V_{GS} = 10V I_D = 50A			40		nC
Q_{GS}	Gate to source charge				10		
Q_{GD}	Gate to drain charge (Miller charge)				15		
W_{DSS}	Drain to source non-repetitivw unclamped inductive turn-off energy	I_D = 50A, V_{DD}≤25V, V_{GS}=10V, R_{GD}=50Ω				125	mJ

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
V_{SD}	Diode forward voltage	I_{SD} = 25A, V_{GS} = 0V		0.95	1.20	V
		I_{SD} = 50A, V_{GS} = 0V		1.0	1.35	
$I_S(I_{SD})$	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET			63	A
I_{SM}	Pulsed source current				240	
t_{rr}	Reverse recovery time	I_{SD} = 50A, V_{GS} = -10V, V_R=30V, dI_F/dt = -100A/μs		50		ns
Q_{rr}	Reverse recovery charge			0.1		μC
t_{ON}	Forward turn-on time	Intrinsic turn-on time is negligible (turn-on is domonated by L_S+L_D)				

Note: 1. Pulse test: Pulse width ≤ 300μs, duty cycle ≤ 2%

ORDERING INFORMATION SCHEME

65 N 06 A

Current rating, I_D
65 = 65A

MOSFET series
N = N-Channel

Voltage rating, V_{DS}
06 = 60V

Package type
A = TO-220AB
H = TO-263(D^2-PAK)

■ TEST CIRCUITS AND WAVEFORMS

Fig.1A Peak diode recovery dv/dt test circuit

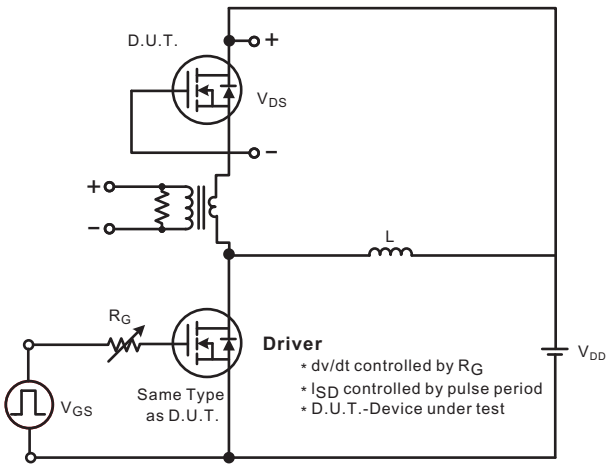


Fig.1B Peak diode recovery dv/dt waverforms

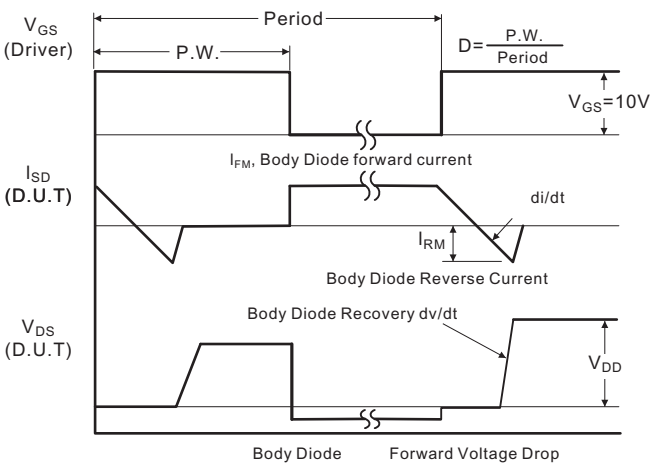


Fig.2A Switching test circuit

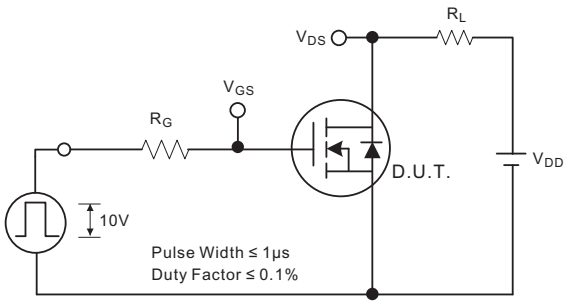


Fig.2B Switching Waveforms

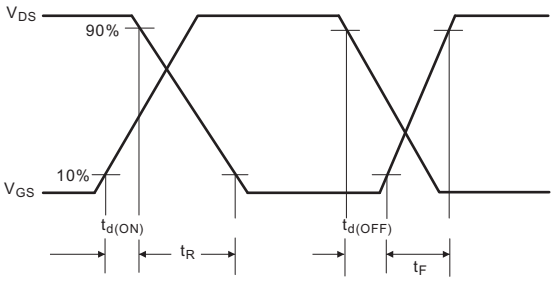


Fig.3A Gate charge test circuit

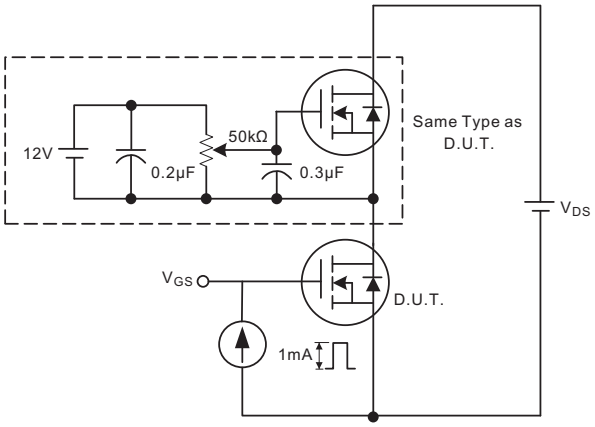
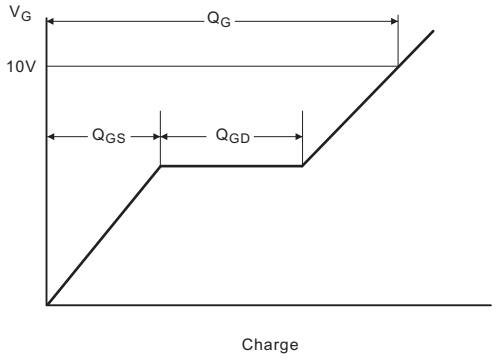


Fig.3B Gate charge waveform



■ TEST CIRCUITS AND WAVEFORMS (Cont.)

Fig.4A Unclamped Inductive switching test circuit

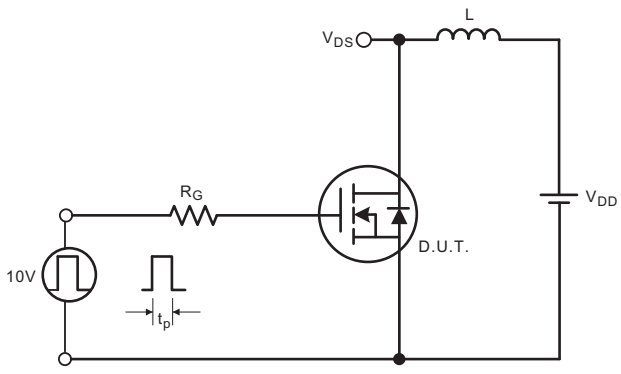
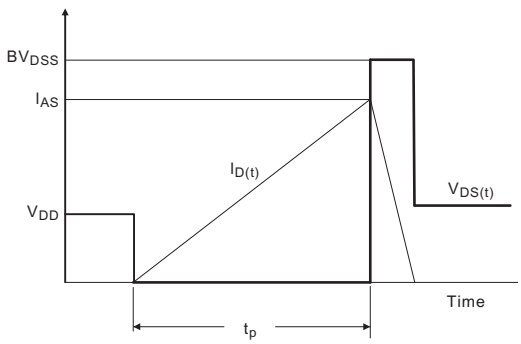


Fig.4B Unclamped Inductive switching waveforms



■ TYPICAL CHARACTERISTICS

Fig.1 Normalised power dissipation

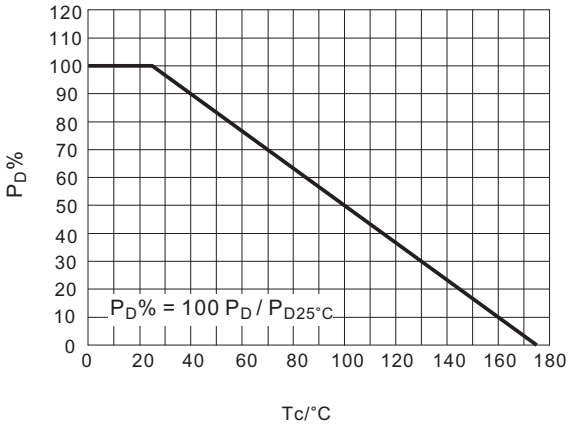


Fig.2 Transient thermal impedance

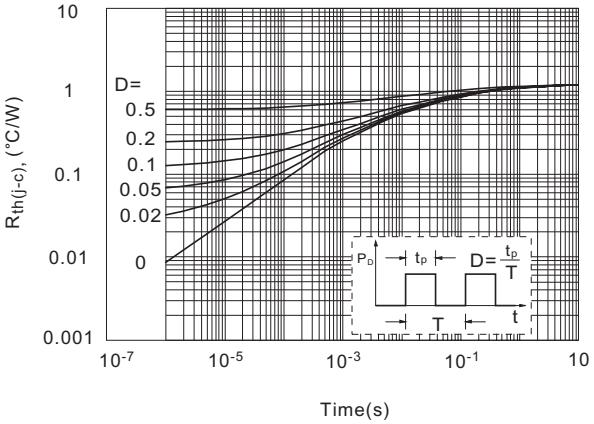


Fig.3 Normalised continuous drain current

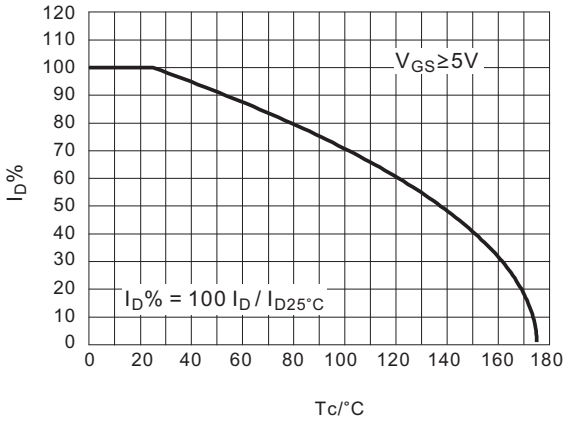


Fig.4 Typical output characteristics, T_j=25°C

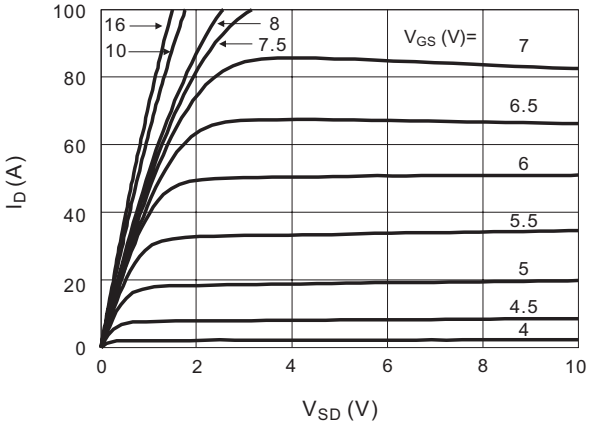


Fig.5 Safe operating area. T_{mb}=25°C

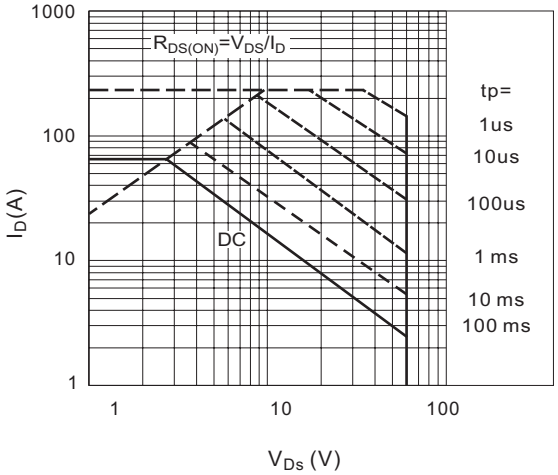


Fig.6 Typical on-state resistance, T_j=25°C

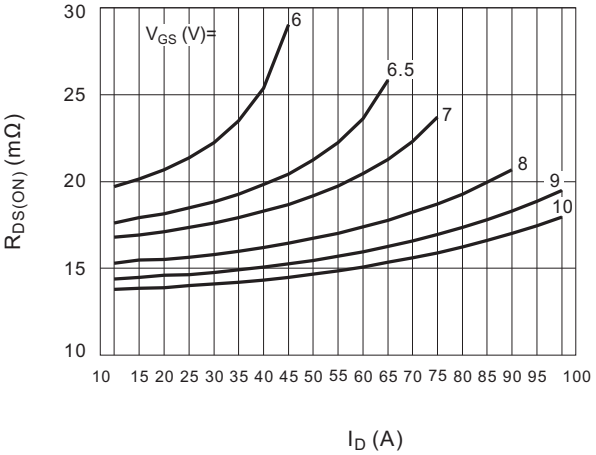


Fig.7 Typical transfer characteristics

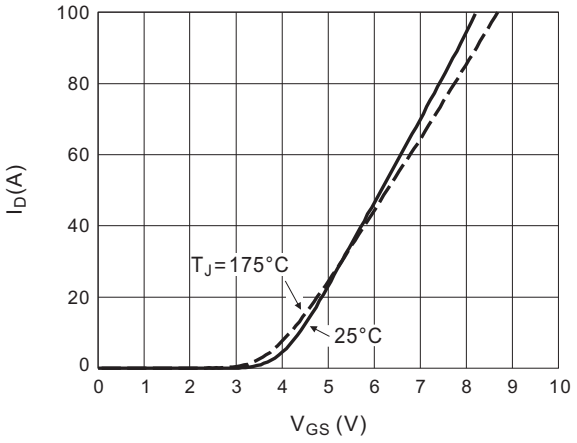


Fig.8 Gate threshold voltage

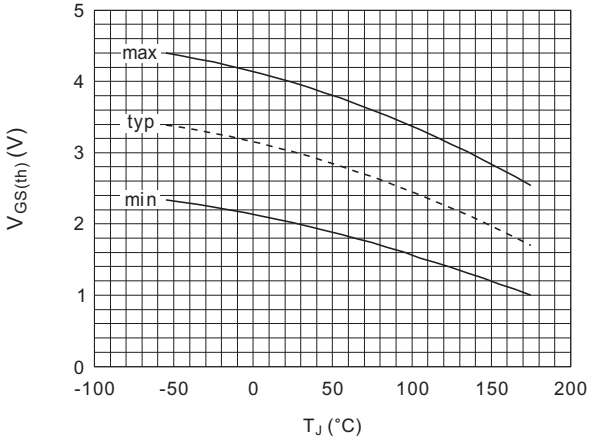


Fig.9 Typical transconductance, T_J=25°C

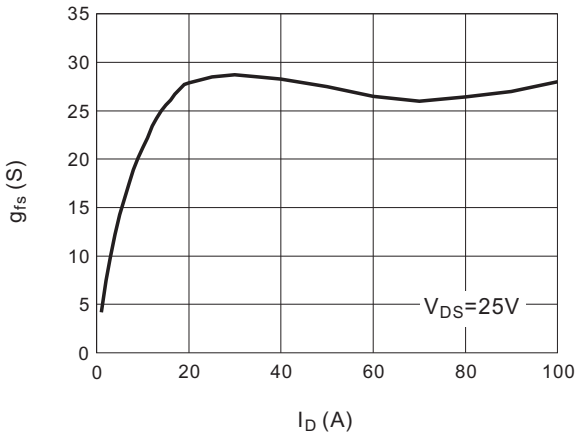


Fig.10 Sub-threshold drain current

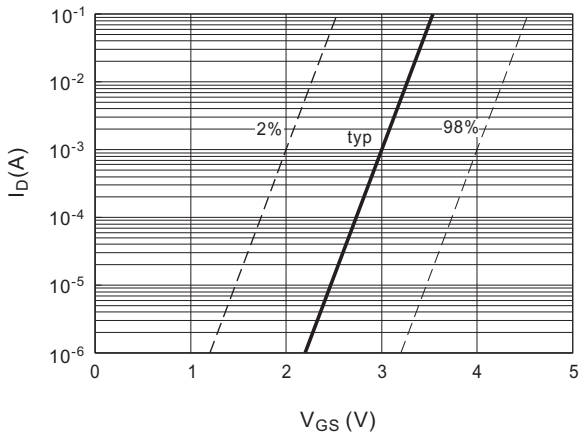


Fig.11 Normalized drain-source on-state resistance

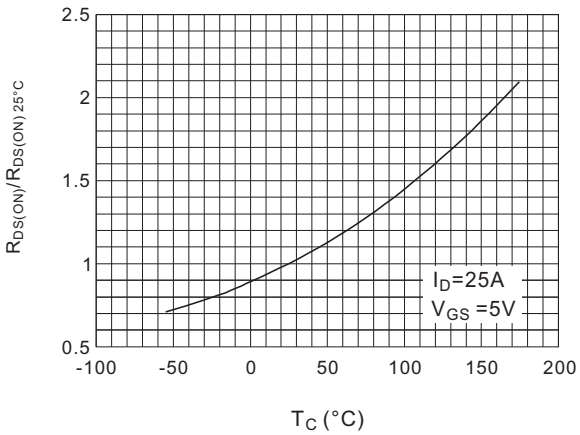


Fig.12 Typical capacitances, C_{iss}, C_{oss}, C_{rss}

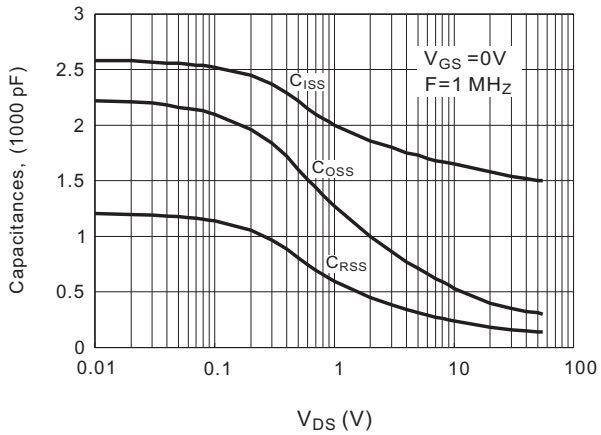


Fig.13 Typical turn-on gate-charge characteristics

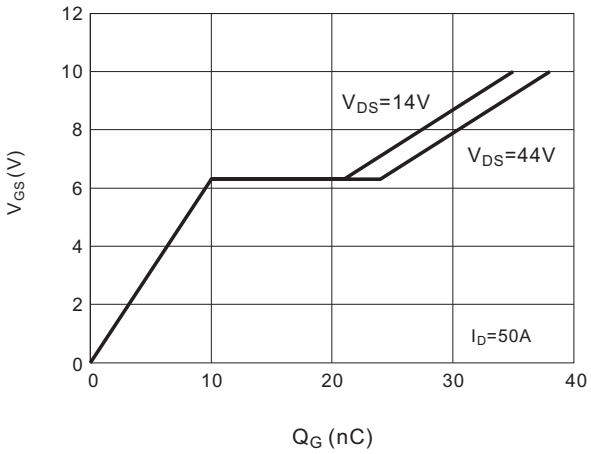


Fig.14 Normalised avalanche energy rating

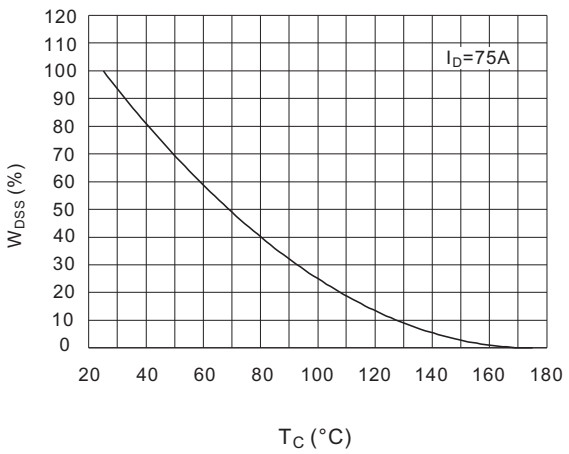


Fig.15 Typical diode forward voltage

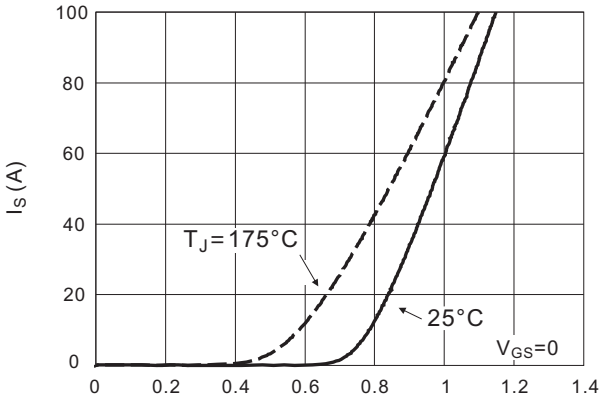
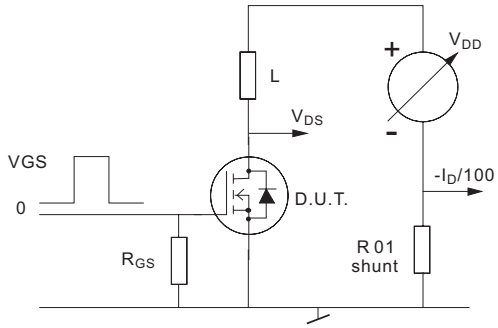


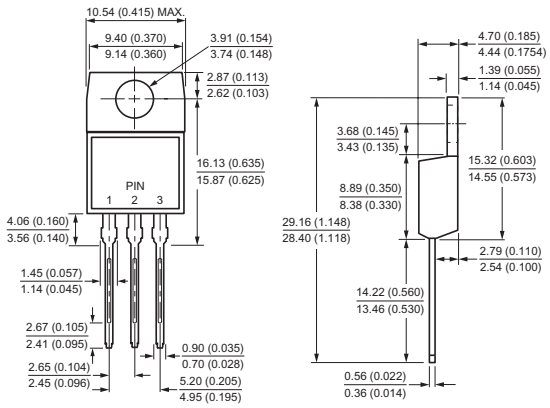
Fig.16 Avalanche energy test circuit



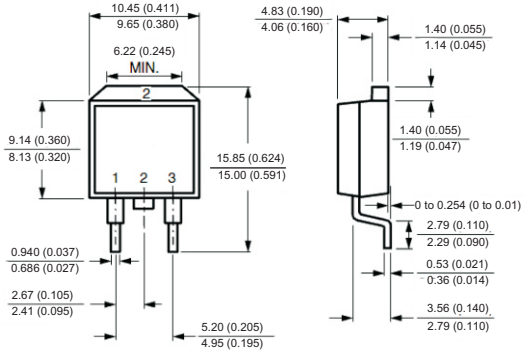
$W_{DSS}=0.5 \cdot L \cdot (I_D)^2 \cdot V_{(BR)DSS}/(V_{(BR)DSS}-V_{DD})$

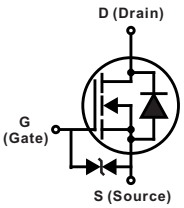
Case Style

TO-220AB



TO-263(D^2PAK)





All dimensions in millimeters(inches)