128MB (16M ´ 64) DDR SDRAM DIMM

1. GENERAL DESCRIPTION

The Winbond W9412FADA series are 16M x 64 Double Data Rate Synchronous Dynamic RAM (DDR SDRAM) memory modules. These modules consists of four pieces of W942516AH (64M x 16 bits) DDR SDRAMs and assembled on a JEDEC standard 184-pin DIMM PCB.

To provide high data bandwidth, W9412FADA uses a double data rate architecture to transfer two data words per clock cycle and delivers a data bandwidth of up to 2.1G (DDR266) bytes per second. It is ideal for high performance systems that require fast data transfer memory modules.

By reading the Serial Presence-Detect (SPD), the system can identify the module type, DDR SDRAM timing parameters and other necessary information to optimize system setting and maximize its performance.

2. FEATURES

- JEDEC standard 184-pin dual In-Line memory module (DIMM)
- Comply to DDR266 and DDR200 specification
- Differential clock inputs (CLK and $\overline{\text{CLK}}$)
- Double Data Rate architecture, two data transfers per clock cycle
- CAS Latency: 2 and 2.5
- Burst Lengths: 2, 4, 8
- Auto Refresh and Self Refresh
- 8K refresh cycles / 64 ms
- Serial Presence Detect with EEPROM
- Interface: SSTL-2
- Power supply: 2.5V ±0.2V
- PCB height: 1.25 inches

3. AVAILABLE PART NUMBERS

MODULE PART NUMBER	SPEED
W9412FADA-7	DDR266/CL2
W9412FADA-75	DDR266/CL2.5

4. PIN ASSIGNMENT

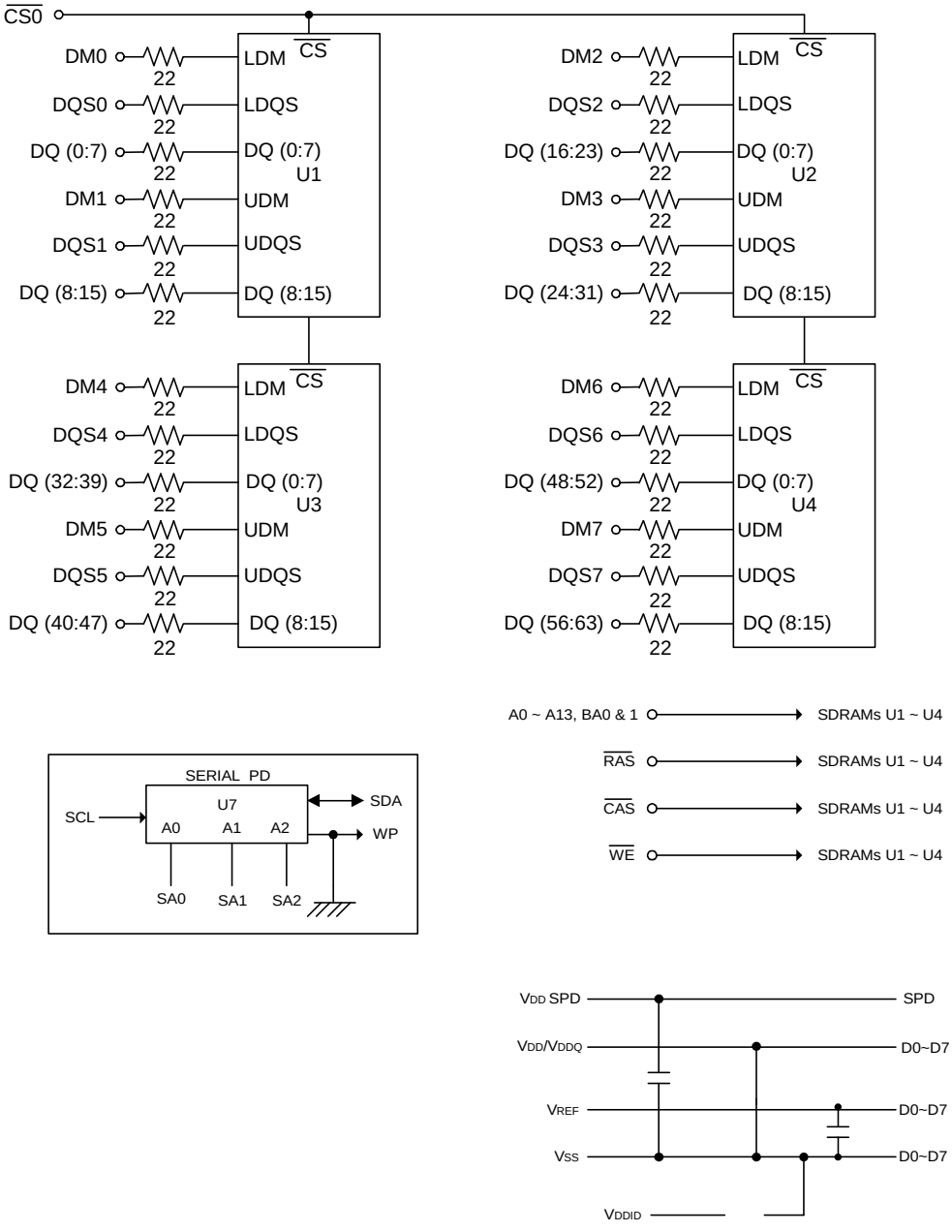
PIN	FONT	PIN	FONT	PIN	FONT	PIN	BACK	PIN	BACK	PIN	BACK
1	VREF	32	A5	62	$V_{DD}Q$	93	V_{SS}	124	V_{SS}	154	$\overline{RAS}$
2	DQ0	33	DQ24	63	$\overline{WE}$	94	DQ4	125	A6	155	DQ45
3	V_{SS}	34	V_{SS}	64	DQ41	95	DQ5	126	DQ28	156	$V_{DD}Q$
4	DQ1	35	DQ25	65	$\overline{CAS}$	96	$V_{DD}Q$	127	DQ29	157	$\overline{CS0}$
5	DQS0	36	DQS3	66	V_{SS}	97	DQS9	128	$V_{DD}Q$	158	$\overline{CS1}$
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DQS12	159	DQS14
7	V_{DD}	38	V_{DD}	68	DQ42	99	DQ7	130	A3	160	V_{SS}
8	DQ3	39	DQ26	69	DQ43	100	V_{SS}	131	DQ30	161	DQ46
9	NC	40	DQ27	70	V_{DD}	101	NC	132	V_{SS}	162	DQ47
10	NC	41	A2	71	*S2	102	NC	133	DQ31	163	*S3
11	V_{SS}	42	V_{SS}	72	DQ48	103	*A13	134	*CB4	164	$V_{DD}Q$
12	DQ8	43	A1	73	DQ49	104	$V_{DD}Q$	135	*CB5	165	DQ52
13	DQ9	44	*CB0	74	V_{SS}	105	DQ12	136	$V_{DD}Q$	166	DQ53
14	DQS1	45	*CB1	75	$\overline{CLK2}$	106	DQ13	137	CLK0	167	NC
15	$V_{DD}Q$	46	V_{DD}	76	CLK2	107	DQS10	138	$\overline{CLK0}$	168	V_{DD}
16	CKL1	47	*DQS8	77	$V_{DD}Q$	108	V_{DD}	139	V_{SS}	169	DQS15
17	$\overline{CLK1}$	48	A0	78	DQS6	109	DQ14	140	*DQS17	170	DQ54
18	V_{SS}	49	*CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	V_{SS}	80	DQ51	111	CKE1	142	*CB6	172	$V_{DD}Q$
20	DQ11	51	*CB3	81	V_{SS}	112	$V_{DD}Q$	143	$V_{DD}Q$	173	NC
21	CKE0	52	BA1	82	$V_{DD}ID$	113	*BA2	144	*CB7	174	DQ60
22	$V_{DD}Q$	**KEY**		83	DQ56	114	DQ20	**KEY**		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	V_{SS}	176	VSS
24	DQ17	54	$V_{DD}Q$	85	V_{DD}	116	V_{SS}	146	DQ36	177	DQS16
25	DQS	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	V_{SS}	56	DQS4	87	DQ58	118	A11	148	V_{DD}	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DQS11	149	DQS13	180	$V_{DD}Q$
28	DQ18	58	V_{SS}	89	V_{SS}	120	V_{DD}	150	DQ38	181	SA0
29	A7	59	BA0	90	WP	121	DQ22	151	DQ39	182	SA1
30	V_{DD}	60	DQ35	91	SDA	122	A8	152	V_{SS}	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	$V_{DD}SPD$

*These pins are not used in this module.

5. PIN DESCRIPTIONS

PIN	NAME	FUNCTION DESCRIPTION
CLKn, $\overline{\text{CLKn}}$	Clock Input	CLKn and $\overline{\text{CLKn}}$ are differential clock inputs. All input command signals are sampled at the positive edge of CLK (except for DQ, DM and CKE).
$\overline{\text{CSn}}$	Chip select	Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
CKEn	Clock Enable	CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self-Refresh mode is entered.
A0 – A12	Address	Multiplexed pins for row and column address. Row address: A0 – A12. Column address: A0 – A8.
BA0 – BA1	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	Row Address Strobe	Command input. When sampled at the rising edge of the clock, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ define the operation to be executed.
$\overline{\text{CAS}}$	Column Address Strobe	Referred to $\overline{\text{RAS}}$
$\overline{\text{WE}}$	Write Enable	Referred to $\overline{\text{RAS}}$
DM0 – DM7	Input/Output Mask	The output buffer is placed at Hi-Z when DM is sampled high in read cycle. In write cycle, sampling DM high will block the write data.
DQ0 – DQ63	Data Input/Output	Multiplexed pins for data output and input
DQS0 – DQS7	Data Strobe Input/Output	Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data.
V_{DD}	Power (+2.5V)	Power supply (2.5V).
V_{SS}	Ground	Ground
V_{REF}	Reference Voltage	SSTL-2 Reference voltage
V_{DD}SPD	SPD Power	Separated power supply for SPD EEPROM (2.3V – 3.6V)
SCL	Serial Clock	Clock for serial presence detection
SDA	Serial Data I/O	Data line for serial presence detection
SAn	SPD Address Line	System assigned address (SA0 – SA2) to identify different memory module in a system board.
NC	No Connection	No connection

6. BLOCK DIAGRAM



7. ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{IN}	Input Voltage	-0.3 to V_{DD} +0.3	V
V_{OUT}	Output Voltage	-0.3 to V_{DD} +0.3	V
V_{DD}	Power Supply Voltage	-0.3 – 4.6	V
T_{OPR}	Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 125	°C
PD	Power Dissipation	4	W
I_{OUT}	Short Circuit Output Current	50	mA

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8. RECOMMENDED DC OPERATING CONDITIONS

°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Power Supply Voltage	V_{DD}	2.3	2.5	2.7	V	2
Power Supply Voltage (for I/O Buffer)	$V_{DD}Q$	2.3	2.5	V_{DD}	V	2
Input Reference Voltage	V_{REF}	0.49 x $V_{DD}Q$	0.50 x $V_{DD}Q$	0.51 x $V_{DD}Q$	V	2,3
Termination Voltage (System)	V_{TT}	V_{REF} -0.04	V_{REF}	V_{REF} +0.04	V	2,8
Input High Voltage (DC)	$V_{IH\ (DC)}$	V_{REF} +0.15	-	$V_{DD}Q$ +0.3	V	2
Input Low Voltage (DC)	$V_{IL\ (DC)}$	-0.3	-	V_{REF} -0.15	V	2
Differential Clock DC Input Voltage	$V_{ICK\ (DC)}$	-0.3	-	$V_{DD}Q$ +0.3	V	15
Input Differential Voltage. CLK and $\overline{CLK}$ inputs (DC)	$V_{ID\ (DC)}$	0.36	-	$V_{DD}Q$ +0.6	V	13,15
Input High Voltage (AC)	$V_{IH\ (AC)}$	V_{REF} +0.31	-	-	V	2
Input Low Voltage (AC)	$V_{IL\ (AC)}$	-	-	V_{REF} -0.31	V	2
Input Differential Voltage. CLK and $\overline{CLK}$ inputs (AC)	$V_{ID\ (AC)}$	0.7	-	$V_{DD}Q$ +0.6	V	13,15
Differential AC input Cross Point Voltage	$V_{X\ (AC)}$	$V_{DD}Q/2$ -0.2	-	$V_{DD}Q/2$ +0.2	V	12, 15
Differential Clock AC Middle Point	$V_{ISO\ (AC)}$	$V_{DD}Q/2$ -0.2	-	$V_{DD}Q/2$ +0.2	V	14, 15

Note: Undershoot limit: V_{IL} (min) = -0.9V with a pulse width $\leq$ 5 nS

Overshoot limit: V_{IH} (max) = $V_{DD}Q$ +0.9V with a pulse width $\leq$ 5 nS

$V_{IH\ (DC)}$ and $V_{IL\ (DC)}$ are levels to maintain the current logic state, $V_{IH\ (AC)}$ and $V_{IL\ (AC)}$ are levels to change to the new logic state.

9. CAPACITANCE

(V_{DD} = $V_{DD}Q$ = 2.5V±0.2V, f = 1 MHz, T_A = 25°C, V_{OUT} (DC) = $V_{DD}Q$/2, V_{OUT} (Peak to Peak) = 0.2V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Address Input Capacitance (A0 – A12, BA0, BA1)	C_{add-IN}		12	pF
Command Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{CMD-IN}		12	pF
$\overline{CS}$ signals Input Capacitance ($\overline{CS0}$)	C_{CS-IN}		12	pF
CKE signal Input Capacitance (CKE0)	C_{CKE-IN}		12	pF
CLK signals Input Capacitance (CLKn, $\overline{CLKn}$)	C_{CLK-IN}		6	pF
DM/DQS/DQ Input capacitance (DM0 – DM7, DQS0 – 7, DQ0 – 63)	$C_{I/O}$		5	pF

10. DC CHARACTERISTICS

PARAMETER	SYM.	MAX.		UNIT	NOTES
		-7	-75		
OPERATING CURRENT: One Bank Active-Precharge; t_{RC} = t_{RC} min; t_{CK} = t_{CK} min; DQ, DM and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle	I_{DD0}	440	440	mA	7
OPERATING CURRENT: One Bank Active-Read-Precharge; Burst = 2; t_{RC} = t_{RC} min; CL=2.5; t_{CK} = t_{CK} min; I_{OUT} = 0mA; Address and control inputs changing once per clock cycle.	I_{DD1}	440	440		7, 9
PRECHARGE-POWER-DOWN STANDBY CURRENT: All Banks Idle; Power down mode; CKE ≤ V_{IL} max; t_{CK} = t_{CK} min; Vin = V_{REF} for DQ, DQS and DM	I_{DD2P}	8	8		
IDLE FLOATING STANDBY CURRENT: $\overline{CS}$ ≥ V_{IH} min; All Banks Idle; CKE ≥ V_{IH} min; Address and other control inputs changing once per clock cycle; Vin = Vref for DQ, DQS and DM	I_{DD2F}	180	160		7
IDLE STANDBY CURRENT: $\overline{CS}$ ≥ V_{IH} min; All Banks Idle; CKE ≥ V_{IH} min; t_{CK} = t_{CK} min; Address and other control inputs changing once per clock cycle; Vin ≥ V_{IH} min or Vin ≤ V_{IL} max for DQ, DQS and DM	I_{DD2N}	180	160		7
IDLE QUIET STANDBY CURRENT: $\overline{CS}$ ≥ V_{IH} min; All Banks Idle; CKE ≥ V_{IH} min; t_{CK} = t_{CK} min; Address and other control inputs stable; Vin ≥ V_{REF} for DQ, DQS and DM	I_{DD2Q}	160	140		7
ACTIVE POWER-DOWN STANDBY CURRENT: One Bank Active; Power down mode; CKE ≤ V_{IL} max; t_{CK} = t_{CK} min	I_{DD3P}	80	80		
ACTIVE STANDBY CURRENT: $\overline{CS}$ ≥ V_{IH} min; CKE ≥ V_{IH} min; One Bank Active-Precharge; t_{RC} = t_{RAS} max; t_{CK} = t_{CK} min; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I_{DD3N}	280	260		7
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One Bank Active; Address and control inputs changing once per clock cycle; CL=2.5; t_{CK} = t_{CK} min; I_{OUT} = 0mA	I_{DD4R}	660	620		7, 9
OPERATING CURRENT: Burst = 2; Write; Continuous burst; One Bank Active; Address and control inputs changing once per clock cycle; CL = 2.5; t_{CK} = t_{CK} min; DQ, DM and DQS inputs changing twice per clock cycle	I_{DD4W}	660	620		7
AUTO REFRESH CURRENT: t_{RC} = t_{RFC} min	I_{DD5}	760	760		7
SELF REFRESH CURRENT: CKE ≤ 0.2V	I_{DD6}	12	12		
RANDOM READ CURRENT: 4 Banks Active Read with activate every 20ns, Auto-Precharge Read every 20ns; Burst = 4; T_{rcd} = 3; I_{OUT} = 0mA; DQ, DM and DQS inputs changing twice per clock cycle; Address changing once per clock cycle	I_{DD7}	1080	1080		

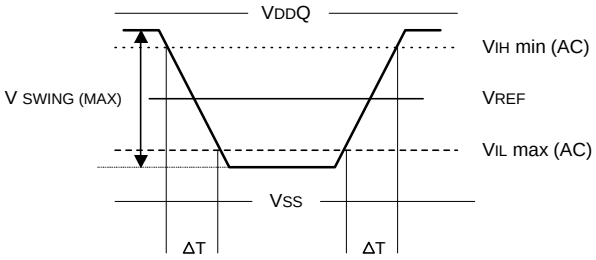
11. AC CHARACTERISTICS OF SDRAM COMPONENTS

(Notes: 10, 12)

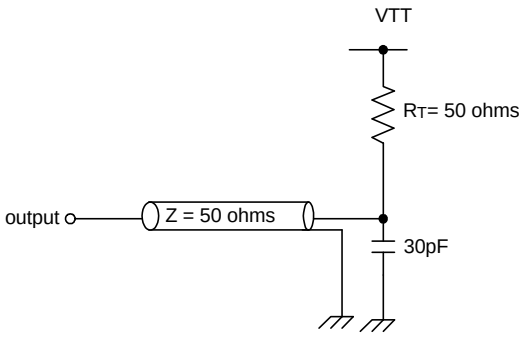
SYMBOL	PARAMETER		-7		-75		UNITS	NOTES
			MIN.	MAX.	MIN.	MAX.		
t_{RC}	Active to Ref/Active Command Period		65		65		nS	
t_{RFC}	Ref to Ref/Active Command Period		75		75			
t_{RAS}	Active to Precharge Command Period		45	100000	45	100000		
t_{RCD}	Active to Read/Write Command Delay Time		15		15			
t_{RAP}	Active to Read with Auto Precharge Enable		15		15			
t_{CCD}	Read/Write(a) to Read/Write(b) Command Period		1		1		t_{CK}	
t_{RP}	Precharge to Active Command Period		20		20		nS	
t_{RRD}	Active(a) to Active(b) Command Period		15		15			
t_{WR}	Write Recovery Time		15		15			
t_{DAL}	Auto Precharge Write Recovery + Precharge Time		30		30			
t_{CK}	CLK Cycle Time	CL=2	7.5	15	8	15		
		CL=2.5	7	15	7.5	15		
t_{AC}	Data Access Time from CLK, $\overline{CLK}$		-0.75	0.75	-0.75	0.75		16
t_{DQSCK}	DQS Output Access Time from CLK, $\overline{CLK}$		-0.75	0.75	-0.75	0.75		
t_{DQSQ}	Data Strobe Edge to Output Data Edge Skew			0.5		0.5		
t_{CH}	CLk High Level Width		0.45	0.55	0.45	0.55	t_{CK}	11
t_{CL}	CLK Low Level Width		0.45	0.55	0.45	0.55		
t_{HP}	CLK Half Period (minimum of actual t_{CH}, t_{CL})		Min. (t_{CL},t_{CH})		Min. (t_{CL},t_{CH})		nS	
t_{QH}	DQ Output Data Hold Time from DQS		t_{HP} -0.75		t_{HP} -0.75			
t_{RPRE}	DQS Read Preamble Time		0.9	1.1	0.9	1.1	t_{CK}	11
t_{RPST}	DQS Read Postamble Time		0.4	0.6	0.4	0.6		
t_{DS}	DQ and DM Setup Time		0.5		0.5		nS	
t_{DH}	DQ and DM Hold Time		0.5		0.5			
t_{DIPW}	DQ and DM Input Pulse Width (for each input)		1.75		1.75			
t_{DQSH}	DQS Input High Pulse Width		0.35		0.35		t_{CK}	11
t_{DQSL}	DQS Input Low Pulse Width		0.35		0.35			
t_{DSS}	DQS Falling Edge to CLK Setup Time		0.2		0.2			
t_{DSH}	DQS Falling Edge Hold Time from CLK		0.2		0.2			
t_{WPRES}	Clock to DQS Write Preamble Set-up Time		0		0		nS	
t_{WPRE}	DQS Write Preamble Time		0.25		0.25		t_{CK}	11
t_{WPST}	DQS Write Postamble Time		0.4		0.4			
t_{DQSS}	Write Command to First DQS Latching Transition		0.75	1.25	0.75	1.25		
t_{DSSK}	UDQS – LDQS Skew (x 16)		-0.25	0.25	-0.25	0.25		
t_{IS}	Input Setup Time		0.9		0.9		nS	
t_{IH}	Input Hold Time		0.9		0.9			
t_{IPW}	Control & Address Input Pulse Width (for each input)		2.2		2.2			
t_{HZ}	Data-out High-impedance Time from CLK, $\overline{CLK}$		-0.75	0.75	-0.75	0.75		
t_{LZ}	Data-out Low-impedance Time from CLK, $\overline{CLK}$		-0.75	0.75	-0.75	0.75		
$t_{T(SS)}$	SSTL Input Transition		0.5	1.5	0.5	1.5		
t_{WTR}	Internal Write to Read Command Delay		1		1		t_{CK}	
t_{XSNR}	Exit Self Refresh to non-Read Command		75		75		nS	
t_{XSRD}	Exit Self Refresh to Read Command		10		10		t_{CK}	
t_{REF}	Refresh Time (8K)			64		64	mS	
t_{MRD}	Mode Register Set Cycle Time		15		15		nS	

12. AC TEST CONDITION OF SDRAM COMPONENTS

SYMBOL	PARAMETER	VALUE	UNIT	NOTE
V_{IH}	Input High Voltage (AC)	V_{REF} +0.31	V	
V_{IL}	Input Low Voltage (AC)	V_{REF} -0.31	V	
V_{REF}	Input Reference Voltage	0.5 x V_{DDQ}	V	
V_{TT}	Termination Voltage	0.5 x V_{DDQ}	V	
V_{SWING}	Input Signal Peak to Peak Swing	1.0	V	
V_R	Differential Clock Input Reference Voltage	V_x (AC)	V	
V_{ID} (AC)	Input Difference Voltage. CLK and $\overline{CLK}$ Inputs (AC)	1.5	V	
SLEW	Input Signal Minimum Slew Rate	1.0	V/nS	
V_{OTR}	Output Timing Measurement Reference Voltage	0.5 x V_{DDQ}	V	



SLEW = (V_{IH} min (AC) - V_{IL}max (AC)) / ΔT



A.C. TEST LOAD (A)

Notes:

(1) Conditions outside the limits listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device.

(2) All voltages are referenced to V_{SS}, $V_{SS}Q$.

(3) Peak to peak AC noise on V_{REF} may not exceed ±2%of $V_{REF(DC)}$.

(4) V_{OH} = 1.95V,V_{OL} = 0.35V

(5) V_{OH} = 1.9V,V_{OL} = 0.4V

(6) The values of $I_{OH(DC)}$ is based on $V_{DD}Q$ = 2.3V and V_{TT} = 1.19V. The values of $I_{OL(DC)}$ is based on $V_{DD}Q$ = 2.3V and V_{TT} = 1.11V.

(7) These parameters depend on the cycle rate and these values are measured at a cycle rate with the minimum values of t_{CK} and t_{RC}.

(8) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.

(9) These parameters depend on the output loading. Specified values are obtained with the output open.

(10) Transition times are measured between $V_{IH\ min(AC)}$ and $V_{IL\ max(AC)}$.Transition (rise and fall) of input signals have a fixed slope.

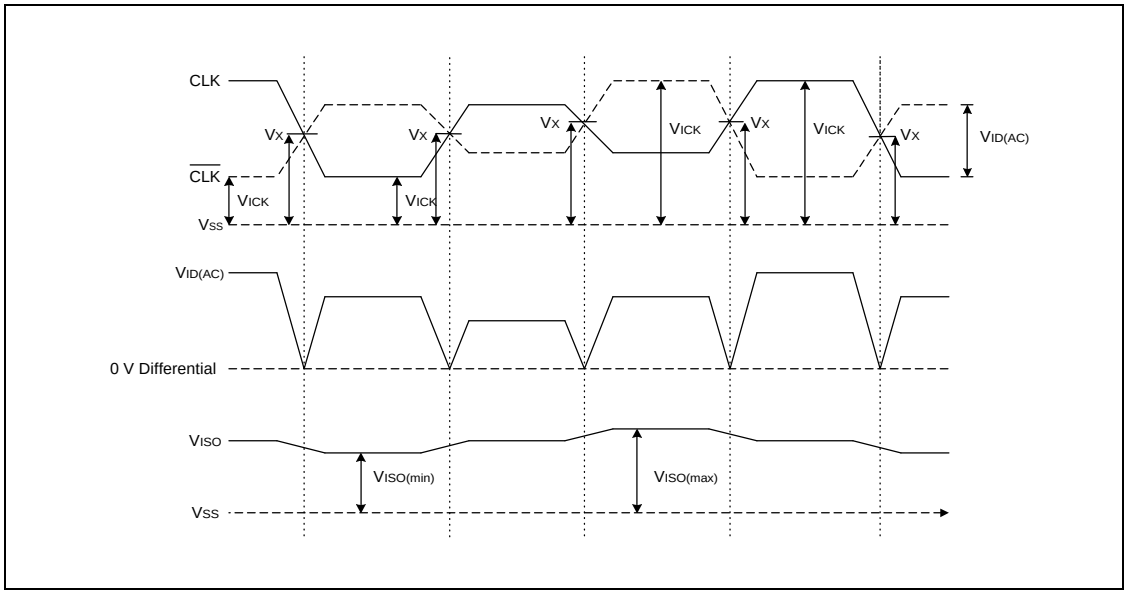
(11) If the result of nominal calculation with regard to t_{CK} contains more than one decimal place, the result is rounded up to the nearest decimal place. i.e., t_{DQSS}=0.75×t_{CK}, t_{CK}=7.5ns, 0.75 × 7.5ns = 5.625ns is rounded up to 5.6ns.

(12) V_X is the differential clock cross point voltage where input timing measurement is referenced.

(13) V_{ID} is magnitude of the difference between CLK input level and $\overline{CLK}$ input level.

(14) V_{ISO} means {V_{ICK}(CLK) + V_{ICK}($\overline{CLK}$)}/2.

(15) Refer to the figure below.



(16) t_{AC} and t_{DQSCK} depend on the clock jitter. These timing are measured at stable clock.

13. OPERATION MODES

The following Simplified Truth Table illustrates the operation modes of DDR SDRAM. For more detailed information please refer to the DDR SDRAM datasheet.

Table 1: Simplified Truth Table

COMMAND	DEVICE STATE	CKE_{N-1}	CKE_N	DM_N	BS0, BS1	A10	A12, A11, A9-A0	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
Bank Active	Idle	H	X	X	V	V	V	L	L	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L
Write	Active(3)	H	X	X	V	L	V	L	H	L	L
Write with Autoprecharge	Active(3)	H	X	X	V	H	V	L	H	L	L
Read	Active(3)	H	X	X	V	L	V	L	H	L	H
Read with Autoprecharge	Active(3)	H	X	X	V	H	V	L	H	L	H
Mode Register Set	Idle	H	X	X	L, L	C	C	L	L	L	L
Extended Mode Register Set	Idle	H	X	X	H, L	V	V	L	L	L	L
No Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Read Stop	Active	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H
Self Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
Self Refresh Exit	Idle (Self Refresh)	L	H	X	X	X	X	H	X	X	X
								L	H	H	X
Power Down Mode Entry	Idle/ Active(5)	H	L	X	X	X	X	H	X	X	X
								L	H	H	X
Power Down Mode Exit	Any (Power Down)	L	H	X	X	X	X	H	X	X	X
								L	H	H	X
Data Write Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Write Disable	Active	H	X	H	X	X	X	X	X	X	X

Notes:

1. V = Valid X = Don't Care L = Low level H = High level
2. CKE_n signal is input level when commands are issued.
3. CKE_{n-1} signal is input level one clock cycle before the commands are issued.
4. These are state designated by the BS0,BS1 signals.
5. Power Down Mode can not entry in the burst cycle.

14. SERIAL PRESENCE DETECT EEPROM

The Serial Presence Detect (SPD) function is implemented by using a 2,408-bit EEPROM component. This nonvolatile storage device contains those data for identifying the module type and various SDRAM organizations and timing parameters. System read operations to the EEPROM device occur using the DIMM SCL(clock) and SDA (data) signals, together with SA(2:0) which provide the EEPROM Device Address.

SPD EEPROM DC Operating Conditions

(V_{CC}=2.3V ~ 3.6V)

PARAMETER/CONDITION	SYMBOL	MIN.	MAX.	UNIT	NOTES
Supply Voltage	V_{CC}	2.3	3.6	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	V_{CC} x 0.7	V_{CC} +0.5	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-0.3	V_{CC} x 0.3	V	
Output Low Voltage, Iout = 3 mA	V_{OL}		0.4	V	I_{OL} = 3 mA
Input Leakage Current, V_{IN} = GND to V_{CC}	I_{LI}		2	µA	
Output Leakage Current, V_{OUT} = GND to V_{CC}	I_{LO}		2	µA	
Power Supply Current SCL clock frequency =100 KHz	I_{CC}		1	mA	

SPD AC Operating Conditions

(V_{CC} = 2.3V ~ 3.6V)

PARAMETER	SYM.	MIN.	MAX.	UNIT
SCL Clock Frequency	f_{SCL}		100	KHz
Noise Suppression Time Constant at SCL, SDA Inputs	t_I		100	nS
SCL Low to SDA Data Out Valid	t_{AA}	0.2	3.5	µS
Time the bus must be free before a new transition can start	t_{BUF}	4.7		µS
Start Condition Hold Time	$t_{HD:STA}$	4.0		µS
Clock Low Period	t_{LOW}	4.7		µS
Clock High Period	t_{HIGH}	4.0		µS
Start Condition Setup Time	$t_{SU:STA}$	4.7		µS
Data in Hold Time	$t_{HD:DAT}$	0		µS
Data in Setup Time	$t_{SU:DAT}$	250		nS
SDA and SCL Rise time	t_R		1	µS
SDA and SCL Fall Time	t_F		300	nS
Stop Condition Setup Time	$t_{SU:STO}$	4		µS
Data Out Hold Time	t_{DH}	200		nS
Write Cycle Time	t_{WR}		10	mS

Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle the EEPROM bus interface circuits are disabled, SDA is allowed to remain high the bus level pull-up resistor, and the device does not respond to its slave address.

15. SPD DATA

Byte No.	FUNCTION DESCRIBED	FUNCTION SUPPORTED		HEX VALUE	
		-7	-75	-7	-75
0	Defines # bytes written into serial memory at module manufacturer	128 bytes		80h	
1	Total # bytes of SPD memory device	256 bytes (2K-bit)		08h	
2	Fundamental memory type (FPM, EDO, DRAM..)	DDR SDRAM		07h	
3	# Row Addresses on this assembly	13		0Dh	
4	# Column Addresses on this assembly	09		09h	
5	# Module Rows on this assembly	1 row		01h	
6	Data Width of this assembly.	64 bits		40h	
7	Data Width continuation	-		00h	
8	Voltage interface standard of this assembly	SSTL 2.5V		04h	
9	SDRAM Cycle time @CAS latency of 2.5	7 nS	7.5 nS	70h	75h
10	SDRAM Access time @CAS latency of 2.5	+/-0.75 nS	+/-0.75 nS	75h	75h
11	DIMM Configuration type (Non-parity, Parity ECC)	Non parity		00h	
12	Refresh Rate/Type	7.8 us, support self refresh		82h	
13	SDRAM width, Primary DRAM	X 16		10h	
14	Error Checking SDRAM data width	None		00h	
15	Minimum Clock Delay, Back Random Column Addresses	TCCD = 1 CLK		01h	
16	Burst Lengths supported	2, 4, 8		0Eh	
17	#Bank on Each SDRAM device	4 banks		04h	
18	CAS# Latencies Supported	2 & 2.5		0Ch	
19	CS# Latency	0 CLK		01h	
20	Write Latency	1 CLK		02h	
21	SDRAM Module Attributes	Differential Clock, Non-buffered Non–registered & redundant addressing		20h	
22	SDRAM Device Attributes: General	2.5V+/-10% voltage tolerance, Burst Read, Write, precharge all, auto precharge		00h	
23	SDRAM cycle time @ CAS latency of 2	7.5 nS	10 nS	75h	A0h
24	SDRAM access time @CAS latency of 2	+/-0.75 nS	+/-0.75 nS	75h	75h
25	SDRAM cycle time @ CAS latency of 1.5	-	-	00h	00h
26	SDRAM access time @CAS latency of 1.5	-	-	00h	00h
27	Precharge to active command period (t_{RP})	20 nS	20 nS	50h	50h
28	Active to Active command period (t_{RRD})	15 nS	15 nS	3Ch	3Ch
29	Active to Read/Write command delay time (t_{RCD})	20 nS	20 nS	50h	50h
30	Minimum Active to precharge period (t_{RAS})	45 nS	45 nS	2Dh	2Dh
31	Density of each Row on Module	Each row of 128 MB		20h	
32	Command and Address signal input setup time	0.9 nS	0.9 nS	90h	90h
33	Command and Address signal input hold time	0.9 nS	0.9 nS	90h	90h
34	Data signal input setup time	0.5 nS	0.5 nS	50h	50h
35	Data signal input hold time	0.5 nS	0.5 nS	50h	50h
36 – 61	Superset Information (may be used in future)	-		00h	
62	SPD data specification revision	Initial release revision		00h	
63	Checksum for Bytes 0-62	-	-	76h	A6h
64 – 128	Unused storage locations	-		00h	

16. LABELING INFORMATION

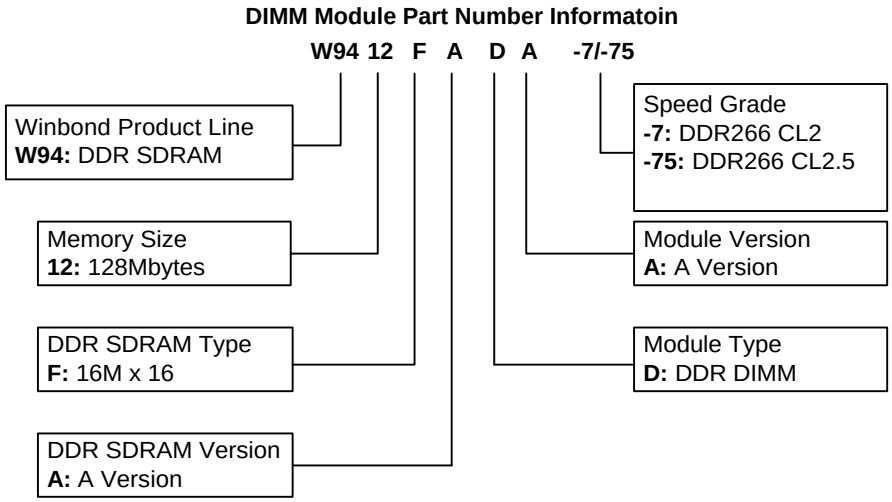
There is a product description sticker stuck on each module to fully describe the information of the module. The following are examples of the product description sticker.

Examples:

MODULE P/N	EXAMPLE OF STICKER
W9412FADA-7 (DDR266/CL2 DIMM)	W9412FADA-7 128MB DDR266/CL2 DIMM TAIWAN 126K264896
W9412FADA-75 (DDR266/CL2.5 DIMM)	W9412FADA-75 128MB DDR266/CL2.5 DIMM TAIWAN 126K264896

The content of this product description sticker is described as below:

1. MODULE PART NUMBER **W9412FADA-7/-75**

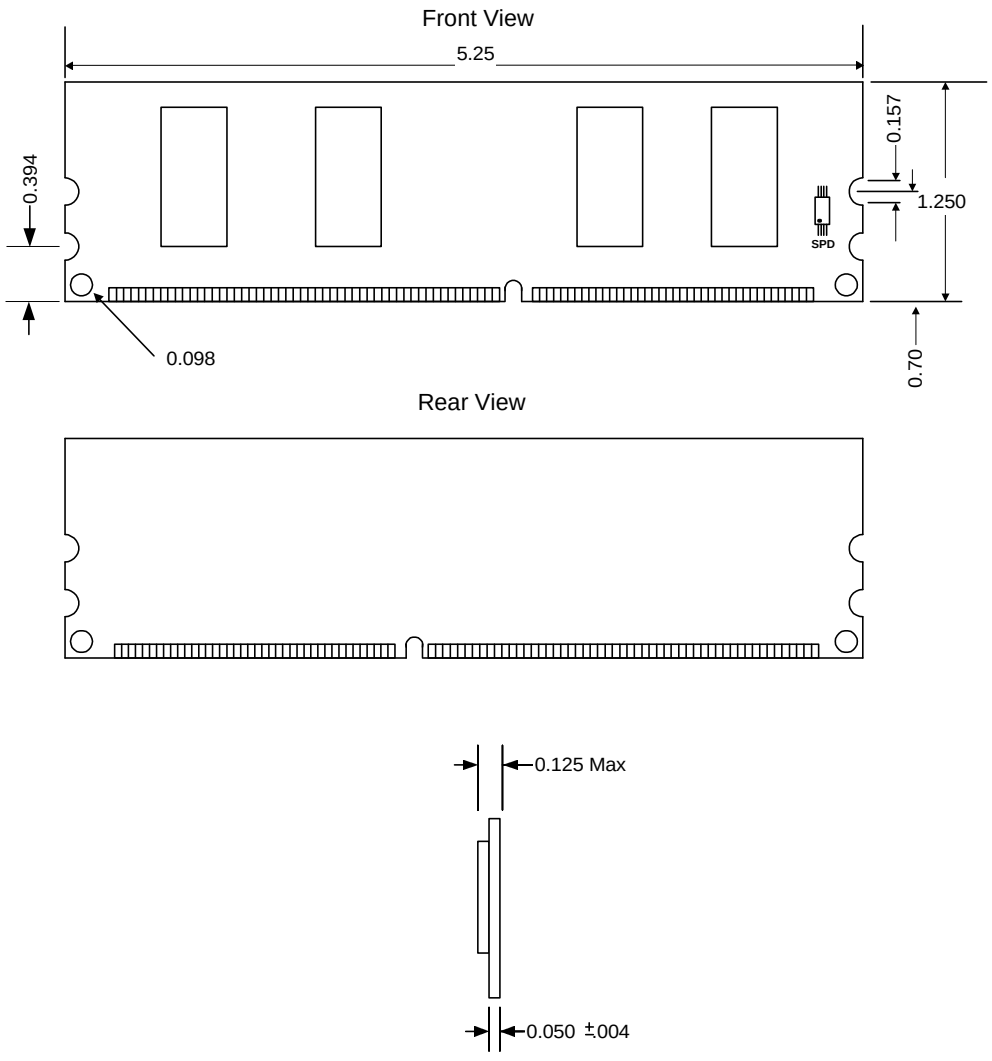


2. Total Memory Size: **128Mbytes**
3. Compliant Industry Spec: **DDR266/CL2, DDR266/CL2.5**
4. Module Type: **DIMM**
5. Manufacturing Location: **TAIWAN**
6. Tracking Number: **126K264896**

   (The number "126K264896" is for reference only. It is changed according to assembly date, assembly site, and serial lot number.)

17. PACKAGE DIMENSIONS

Units:Inches



Tolerances: .005 unless othrerwise specified
Component P/N: W942516AH-7/-75 (16M X 16 DDR-SDRAM,TSOP-66)

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