S1C33L26

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CMOS 32-bit Application Specific Controller

- 32-bit RISC CPU core (Epson S1C33 PE core) (Max. 60 MHz operation)
- 34KB RAM (including cache and VRAM)
- Programmable operating clock using PLL
  (Division ratio: 1/1～1/10, Multiplication ratio: x1～x16)
- DSP function (Multiplier/ Divider)
- 1KB Instruction Cache and 1KB Data Cache
- Graphics Engine (GE)
  - Drawing objects, Image data block transfer, Drawing effects
  - Word boundary commands (variable length) are provided for drawing control and commands list.
- LCD controller
  - Supports 1/2/4/8/12/16 and 24 bpp (16M-color) TFT color panel
  - Supports 1/2/4/8/12 bpp CSTN,1/2/4 bpp mono-STN panel
  - IVRAM (QVGA: 320 x 240 2bpp)
  - Supports up to 16M-color LCD controller with external SDRAM/SRAM as VRAM.
  - Two-image overlay display via the Picture-in-Picture Plus function
  - Brightness/gray scale control via the mono display LUT (Look Up Table with 16 × 4 bits), or palette control via the color display LUT (Look Up Table RAM with 256 × 16 bits)
- 8-ch. DMA controller
- Burst control SDRAM controller
- 1-ch. x 16-bit audio PWM timer
- 2-ch. x 16-bit PWM timer, 8-ch. x 8-bit timer
- 1-ch. Universal Serial I/F (UART/SPI/I2C)
- 1-ch. Universal Serial I/F with Serial or Parallel LCD interface
- 2-ch. SIO with FIFO
- I^2S bus interface (16-bit format)
- Remote Controller Circuit (REMC)
- 6-ch. 10-bit ADC for-analog input
- USB－FS(12Mbps) function controller (FIFO 1KB)
- RTC and 16-Byte battery backup RAM with separated $RTCV_{DD}$

■ DESCRIPTIONS

The S1C33L26 is a 32-bit application specific RISC controller that features extensive peripheral circuits such as an enhanced drawing graphics module, GPIO ports, serial interface modules, a USB module, PWM generators, and an A/D converter. It is suitable for applications that require a high-resolution LCD display, e.g. control panels on OA/FA equipment and intelligent remote controllers.

The S1C33L26 incorporates an LCD controller and VRAM supporting four-level gray scale QVGA display in single-chip. Adding an external SDRAM expands this capability into a higher resolution and with more displayable colors (e.g., 64K-color VGA display). An LCD driver interface with DMA function is also implemented allowing efficient data transfer to LCD modules that include a built-in VRAM LCD driver. In addition, the embedded Graphics Engine (GE) provides rich graphic features, such as drawing functions for dots, straight lines, triangles, rectangles, and circles, resizing, and rotation that can be used simply by calling commands.

The GE also supports drawing of lossless compressed image data; this makes it possible to reduce CPU load and image data ROM size.

As for DSP functions, a 32-bit × 32-bit multiplier (MUL) and a 16-bit ÷ 16-bit divider (DIV) are implemented. These functions help reduce CPU load for ADPCM audio data playback processing. Also the embedded I2S interface module is used to connect an external audio DAC.
The S1C33L26 has adopted the EPSON SoC (System on Chip) design technology using 0.18 μm low power CMOS process to install these features.

■ FEATURES

- Technology
  - 0.18 µm AL-4-layers mixed analog low power CMOS process technology
- CPU
  - EPSON original C33 PE 32-bit RISC CPU-Core
  - Maximum operating frequency: 60 MHz (36 MHz in SDRAM double frequency mode)
  - Internal two-stage pipeline
  - Instruction set: 125 instructions (16-bit fixed length)
  - Dual AMBA bus system for CPU and GE
- DSP
  - Multiplier (MUL)
    - 32 × 32 bits (seven cycles) or 16 × 16 bits (five cycles)
  - Divider (DIV)
    - 16 ÷ 16 bits (18 cycles)
- Internal Memories
  - IRAM (Internal RAM)
    - 12K bytes
  - IVRAM (Internal VRAM)
    - 20K bytes
    - Configurable as a 32K-byte general-purpose RAM sequentially addressed with IRAM
  - Cache RAM
    - 1K bytes (instruction cache RAM)
    - 1K bytes (data cache RAM)
    - Usable as a general-purpose RAM when not used as cache RAM
  - DSTRAM (DMA descriptor RAM)/LUTRAM (look-up table RAM)
    - 512 bytes (can exclusively be used as either DSTRAM or LUTRAM.)
    - DMA descriptor RAM for storing DMA control table (128 × 32 bits)
    - Color look-up table RAM for LCDC (256 × 16 bits)
      16 bits = (R: 5 bits, G: 6 bits, B: 5 bits)
    - The DMA control table can be located in the IVRAM or an external RAM when this RAM is used for LCDC color look-up table.
  - BBRAM (Battery backup RAM)
    - 16 bytes
    - The RAM contents can be maintained while the system power is off using the separated power supply for RTC.
- Input clock
  - High-speed clock (OSC3)
    - Maximum input clock frequency: 48 MHz
    - Internal oscillator circuit (crystal or ceramic resonator) or external clock input
  - Low-speed clock (OSC1)
    - 32.768 kHz (typ.) clock for RTC and low-power operations
    - Internal oscillator circuit (crystal resonator) or external clock input
- Cache Controller (CCU)
  - 1K-byte instruction cache and 1K-byte data cache with a four-way associative frame structure (four frames/way, four lines/frame, four words/line)
  - LRU replacement algorithm
  - Automatic lock function during debug mode and the interrupt process of specified priority
  - The instruction cache RAM and data cache RAM can be used as a general-purpose RAM when the cache function is disabled.
- DMA Controller (DMAC)
  - Eight channels of table DMA
  - Supports table reloading and low-priority channel pausing functions.
  - Trigger sources
    - USI (SPI/UART)
    - USIL (SPI/UART/Built-in RAM LCD interface)
    - FSIO (Asynchronous/Synchronous)
    - I2S
    - 16-bit audio PWM timer (T16P)
    - A/D converter (ADC10)
    - I/O ports (GPIO)
    - USB function controller (USB)
    - 16-bit PWM timer (T16A5)
    - Software
- Graphics Engine (GE)
  - Object drawing
    - Shapes with width: straight lines (vertical, horizontal, and sloped lines), rectangle frames, and circle rings

- Solid Shapes: points, triangles, rectangles, quadrilaterals, circles
- Texts with a font specified
- Compressed image (original run-length encoding)

• Image data block transfer
- Rectangle area copy within VRAM
- Data copy between VRAM and other memory

• Drawing effects
- Clip drawing
- Line width setting
- Drawing color setting with transparency-effect
- Fill/Mesh/Rewrite/XOR
- Color conversion with palette/color depth conversion
- Resize/repeat/rotation (texts/compressed image)

• Word boundary commands (variable length) for drawing control and commands list.

- SRAM Controller (SRAMC)
  • Allows direct connection of SRAM, ROM, and Flash memories.
  • 26-bit address bus and 8/16-bit selectable data bus
  • Up to six chip enable signals are available to connect external devices.
  • Up to 64M-byte (A[25:0]) address space is accessible with each chip enable signal.
  • Programmable bus access wait cycle (0 to 15 cycles)
  • Supports little endian access.
  • Memory mapped I/O
  • Supports both A0 and BS (Bus Strobe) type devices.
  • Supports external wait request via the #WAIT pin.
- SDRAM Controller (SDRAMC)
  • Supports SDRAM direct interface. (Max. 72 MHz SDRAM clock)
  • Supports only SDRAM devices with 16-bit data bus.
    - Minimum configuration: 16M bits (2MB), 16-bit SDRAM × 1
    - Maximum configuration: 512M bits (64MB), 16-bit SDRAM × 1
  • CAS latency: one, two, or three programmable
  • Supports burst and single read/write operations.
  • Equipped with a two-stage × 32-bit DQB (Data Queue Buffer).
  • Supports up to four SDRAM banks and bank active mode.
  • Built-in 12-bit auto-refresh counter
  • Intelligent self-refresh function for low power operation
  • Arbitrates ownership of the external bus between the CPU, DMAC, LCDC, and GE.
- Clock Management Unit/Oscillators/PLL (CMU)
  • Selects the system clock source (OSC3, PLL, OSC1).
  • Turns the OSC3 and OSC1 oscillator circuits on and off.
  • Controls frequency multiplication rate of the PLL (×1 to ×16).
  • Controls clocks according to the standby mode (SLEEP and HALT).
  • Controls the external clock.
  • Controls clock supply to the core and peripheral modules.
  • OSC3 oscillator circuit
    - Crystal oscillation: 5 MHz min. to 48 MHz max.
    - Ceramic oscillation: 5 MHz min. to 48 MHz max.
    - External clock input: 5 MHz min. to 48 MHz max.

  * A 48 MHz clock source with 0.25% of accuracy should be connected for using the USB function.
  * Before using a ceramic resonator, please be sure to contact Murata Manufacturing Co., Ltd. for further information on conditions of use for ceramic resonators.

  • PLL
    - PLL input frequency: 5 MHz min. to 50 MHz max. (OSC3 ×1, ×1/2, ×1/3, ... ×1/9, ×1/10)
    - PLL output frequency: 20 MHz min. to 72 MHz max.
    - Multiplication rate: ×1, ×2, ×3, ... ×15, ×16
  • OSC1 oscillator circuit
    - Crystal oscillation: 32.768 kHz typ.
    - External clock input: 32.768 kHz typ.
- Interrupt Controller (ITC)
  • Five non-maskable interrupts
  • 31 maskable interrupts (including four software interrupts)
- 16-bit Audio PWM Timer (T16P)
  • One channel of 16-bit timer/counter with PWM output function
  • Three bit division modes are provided. (10 bits + 6 bits, 9 bits + 7 bits, 8 bits + 8 bits)
  • Supports 8, 16, 22.05, 32, 44.1, and 48 kHz sampling rates.
  • Audio PWM function supporting 8-bit and 16-bit PCM data (mono)
  • Can output monophonic sound without using an external DAC (external resistors and capacitors are required).
  • Supports fine mode to control pulse widths with high accuracy.
  • Supports a digital volume control function.
  • Can generate two types of compare-match interrupts.

  - Supports DMA transfer.
- 8-bit Timers (T8, T8F)
  - T8F: four channels of 8-bit timer with fine mode (presettable down counter)
    T8: four channels of 8-bit timer without fine mode
  - Clocks generated with the counter underflow can be output to internal devices.
    - The T8F Ch.0 can be used as the USI clock generator.
    - The T8F Ch.3 can be used as the USIL clock generator.
    - The T8F Ch.2 can be used to trigger the ADC10.
  - Each timer can generate underflow interrupts.
- 16-bit PWM Timer (T16A5)
  - Two channels of 16-bit timer with a counter capture/comparison functions
  - Each channel has built-in two comparison/capture data buffers.
  - Can generate compare/capture interrupts.
  - Supports DMA transfer.
- Watchdog Timer (WDT)
  - 30-bit watchdog timer to generate an NMI or a reset
  - Programmable watchdog timer overflow period (NMI or reset interrupt period)
  - The watchdog timer overflow signal can be output outside the IC.
- Real Time Clock (RTC)
  - Contains time counters (seconds, minutes, and hours) and calendar counters (days, days of the week, months, and years).
  - 24-hour or 12-hour mode can be selected.
  - Operates with an independent power supply (RTCVDD) separated from system power (operable while the system power is off).
  - Provides the WAKEUP output pin and #STBY input pin to control standby mode.
  - Can generate periodic interrupts.
- Universal Serial Interface (USI)
  - Multi-serial I/O that can be used as a UART, SPI, or I2C module
  - Contains 1-byte receive data buffer and 1-byte transmit data buffer.
  - UART mode
    - Character length: 7 or 8 bits
    - Parity mode: even, odd, or no parity
    - Stop bit: 1 or 2 bits (start bit: 1 bit fixed)
    - Supports both MSB first and LSB first modes.
    - Parity error, framing error, and overrun error detectable
    - Can generate receive buffer full, transmit buffer empty, and receive error interrupts.
    - Supports DMA transfer.
  - SPI mode
    - Supports both master and slave modes.
    - Data length: 8 or 9 bits (master mode), 8 bits fixed (slave mode)
    - Supports both MSB first and LSB first modes.
    - Data transfer timing (clock phase and polarity variations) is selectable from among 4 types.
    - Receive data mask function is available.
    - Can generate receive buffer full, transmit buffer empty, and overrun error interrupts.
    - Supports DMA transfer.
  - I2C mode
    - Supports both master (single master only) and slave modes.
    - 7-bit addressing mode (10-bit addressing is possible by software control.)
    - Supports clock stretch/wait functions.
    - Can generate start/stop, data transfer, ACK/NAK transfer, and overrun error interrupts.
- Universal Serial Interface with Built-in RAM LCD interface (USIL)
  - Multi-serial I/O that can be used as a UART, SPI, I2C, or built-in RAM LCD interface module
  - Contains 1-byte receive data buffer and 1-byte transmit data buffer.
  - UART mode
    - Character length: 7 or 8 bits
    - Parity mode: even, odd, or no parity
    - Stop bit: 1 or 2 bits (start bit: 1 bit fixed)
    - Supports both MSB first and LSB first modes.
    - Parity error, framing error, and overrun error detectable
    - Can generate receive buffer full, transmit buffer empty, and receive error interrupts.
    - Supports DMA transfer.
  - SPI mode
    - Supports both master and slave modes.
    - Data length: 8 bits fixed
    - Supports both MSB first and LSB first modes.
    - Data transfer timing (clock phase and polarity variations) is selectable from among 4 types.
    - Receive data mask function is available.
    - Can generate receive buffer full, transmit buffer empty, and overrun error interrupts.
    - Supports DMA transfer.

- I2C mode
  - Supports both master (single master only) and slave modes.
  - 7-bit addressing mode (10-bit addressing is possible by software control.)
  - Supports clock stretch/wait functions.
  - Can generate start/stop, data transfer, ACK/NAK transfer, and overrun error interrupts.
- LCD SPI mode
  - Data length is configurable for 8 bits, 16 bits, 18 bits (4 data format) and 24 bits + CMD bit.
  - CMD bit or A0 is selectable.
  - Data transfer timing (clock phase and polarity variations) is selectable from among 4 types.
  - Can generate transmit buffer empty interrupts.
  - Supports DMA transfer.
- LCD parallel interface mode
  - Provides 8-bit data bus, #CS, #RD, #WR and A0 control signals.
  - Supports byte read/write access mode only.
  - Can generate transmit buffer empty and receive buffer full interrupts.
  - Supports DMA transfer for both data transmission and reception.
  - Access timings can be controlled using T8F. The setup cycle (1 to 4), hold cycle (1 to 4), and wait cycle (1 to 16) are configurable.

● Serial Interface with FIFO (FSIO)
- Two channels of clock synchronous/asynchronous serial interface
- Contains FIFO data buffers (4-byte receive data buffer and 2-byte transmit data buffer are available for each channel).
- Supports IrDA1.0-equivalent communications by software control or using an external IrDA driver.
- Contains a baud-rate generator (12-bit programmable timer).
- Can generate receive buffer full, transmit buffer empty, and receive error interrupts.
- Supports DMA transfer.

● I^2S Bus Interface (I2S)
- Supports universal audio I^2S bus interface.
- Contains a 16-byte transmit FIFO (16 bits × 2 channels × 4)
- I^2S output: one channel
- Resolution: 16 bits (PCM data output format)
- Operates as master that generates the bit clock, word-select signal, data and master clock.
- Clock polarity and data shift direction (MSB first/LSB first) are software configurable.
- Can generate I^2S FIFO empty interrupts.
- Supports DMA transfer.

● Card Interface (CARD)
- Generates 8-bit or 16-bit NAND Flash interface signals.
- The ECC and EDC functions should be implemented in the application program.

● Infrared Remote Controller (REMC)
- Outputs a modulated carrier signal and inputs remote control pulses.
- Embedded carrier signal generator and data length counter
- Can generate counter underflow interrupts for data transmission and input rising/falling edge detection interrupts for data reception.

● LCD Controller (LCDC)
- Supports STN LCD panels with 4/8-bit data lines or TFT LCD panels with up to 24-bit data lines.
- Supports generic panel resolutions up to VGA, such as 640 × 480 pixels (VGA) and 320 × 240 pixels (QVGA) (can be configured according to the panel used).
- Supports up to 16M-color (for color TFT), 4K-color (for color STN), and 16-level gray scale (for monochrome STN) display modes.
- Typical display configuration when the internal VRAM (20KB) is used
  - 320 × 240 pixels, 2 bpp (4-level gray scale display)
- Display configuration when an external memory is used
  - 320 × 240 pixels, 16 bpp (QVGA 64K-colors display)
  - 400 × 240 pixels, 16 bpp (WQVGA 64K-colors display)
  - 640 × 480 pixels, 16 bpp (VGA 64K-colors display)
- Two-image overlay display via the Picture-in-Picture Plus function
- Brightness/gray scale control via the mono display LUT (Look Up Table with 16 × 4 bits), or palette control via the color display LUT (Look Up Table RAM with 256 × 16 bits)
- Virtual display function to handle images with a different resolution from the LCD panel (any area in the virtual screen can be displayed on the LCD.)

● A/D Converter (ADC10)
- 10-bit A/D converter with up to six analog input channels
- Conversion time: 10 µs min. (when 2 MHz input clock is selected)
  1,250 µs max. (when 16 kHz input clock is selected)
- Can generate conversion completion and data overwrite interrupts.

● USB Function Controller (USB)
- Supports USB2.0 full speed (12M bps) mode.
- Supports auto negotiation function.
- Supports control, bulk, isochronous and interrupt transfers.

- Scratchable variable number of bulk end points
- Embedded 1K-byte programmable FIFO
- Can generate USB interrupts.
- Supports DMA transfer.

● General-purpose I/O Ports (GPIO)
- Maximum 71 I/O ports and six input ports are available (144-pin package).
- Can generate maximum 16 input interrupts from 64 I/O ports.
- Supports DMA transfer.

* The GPIO ports are shared with other peripheral function pins (USI, PWM etc.). Therefore, the number of GPIO ports depends on the peripheral functions used.

● Operating Voltage
- HVDD (I/O power voltage)
  2.7 V to 3.6 V (3.3 V typ.)
  or 3.0 V to 3.6 V (3.3 V typ.) when the USB module is used.
- AVDD (analog power voltage)
  2.7 V to 3.6 V (3.3 V typ.) or 3.0 V to 3.6 V (3.3 V typ.)
- LVDD (core/internal logic power voltage)
  1.65 V to 1.95 V (1.8 V typ.)
  or 1.7 V to 1.9 V (1.8 V typ.) when a ceramic resonator is used.
- PLLVDD (PLL power voltage)
  1.65 V to 1.95 V (1.8 V typ.)
  or 1.7 V to 1.9 V (1.8 V typ.) when a ceramic resonator is used.
- RTCVDD (RTC/BBRAM power voltage)
  1.65 V to 1.95 V (1.8 V typ.)
  or 1.7 V to 1.9 V (1.8 V typ.) when a ceramic resonator is used.

* LVDD = PLLVDD = RTCVDD
The S1C33L26 does not support 5 V tolerant I/O.

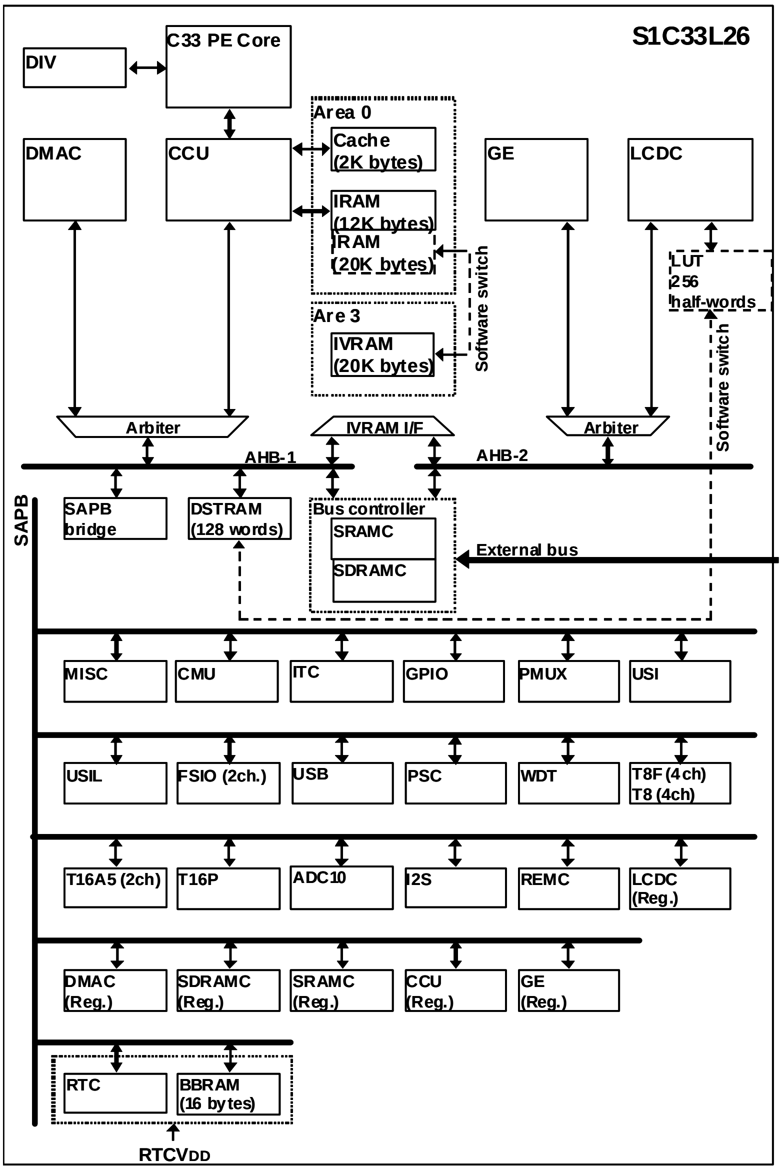
● Operating Temperatures
- -40 to 85°C
- 0 to 70°C when the USB module and a ceramic resonator are used.

● Power Consumption
- During SLEEP: 2.6uA (typ.) RTC: On
  1.6uA (typ.) RTC: Off
- During HALT: 4.2mA (typ.) when 48MHz OSC is used. All peripheral clocks: Off
- During execution: 22mA (typ.) when 48MHz OSC is used with CPU in normal operating state.
  All peripheral clocks: Off
  40mA (typ.) when 48MHz OSC is used with CPU in normal operating state and GE in IDLE state.

*I/O current is not included.
* Power consumption can be reduced by controlling the clocks through the clock management unit (CMU).

● Shipping Form
- Die form
- Plastic package: TQFP15-128pin
  TQFP24-144pin
  PFBGA12U-180

■ BLOCK DIAGRAM



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