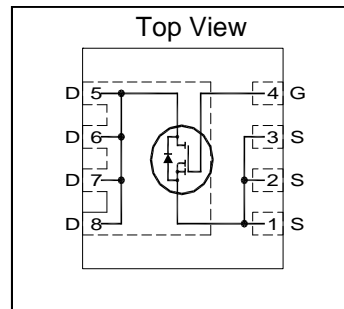


HEXFET® Power MOSFET

$V_{DSS}$	<b>30</b>	<b>V</b>
$R_{DS(on) \max}$ (@ $V_{GS} = 10V$ )	<b>16</b>	<b>mΩ</b>
(@ $V_{GS} = 4.5V$ )	<b>25</b>	
$Qg$ (typical)	<b>5.0</b>	<b>nC</b>
$I_D$ (@ $T_C(Bottom) = 25^\circ C$ )	<b>20</b> Ⓣ	<b>A</b>



**Applications**

- Control MOSFET for synchronous buck converter
- Load Switch

**Features**

Low Charge (typical 5.2 nC)
Low Thermal Resistance to PCB (<6.2°C/W)
Low Profile (<0.9 mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant, Halogen-Free
MSL1, Consumer Qualification

results in  
⇒

**Benefits**

Low Switching Losses
Enable better Thermal Dissipation
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFHM8342PbF	PQFN 3.3mm x 3.3mm	Tape and Reel	4000	IRFHM8342TRPbF

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	10	A
$I_D @ T_C(Bottom) = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	28ⓉⓈ	
$I_D @ T_C(Bottom) = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	18Ⓢ	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Source Bonding Technology Limited)	20Ⓣ	
$I_{DM}$	Pulsed Drain Current ①	112	
$P_D @ T_A = 25^\circ C$	Power Dissipation ⑤	2.6	W
$P_D @ T_C(Bottom) = 25^\circ C$	Power Dissipation	20	
	Linear Derating Factor	0.020	W/°C
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑧ are on page 8

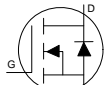
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	20	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DSON</sub>	Static Drain-to-Source On-Resistance	—	13	16	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 17A ③
		—	20	25		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 14A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.35	1.8	2.35	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 25μA
ΔV <sub>GS(th)</sub>	Gate Threshold Voltage Coefficient	—	-5.2	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	1.0	μA	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
g <sub>fs</sub>	Forward Transconductance	19	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 17A
Q <sub>g</sub>	Total Gate Charge	—	10	—	nC	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 15V, I <sub>D</sub> = 17A
Q <sub>gs</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	1.8	—		V <sub>GS</sub> = 4.5V
Q <sub>gd</sub>	Gate-to-Drain Charge	—	1.7	—		I <sub>D</sub> = 17A
Q <sub>godr</sub>	Gate Charge Overdrive	—	1.5	—		
Q <sub>oss</sub>	Output Charge	—	3.3	—		V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V
R <sub>G</sub>	Gate Resistance	—	2.6	—	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	8.1	—	ns	V <sub>DD</sub> = 15V, V <sub>GS</sub> = 4.5V
t <sub>r</sub>	Rise Time	—	30	—		I <sub>D</sub> = 17A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	7.6	—		R <sub>G</sub> = 1.8Ω
t <sub>f</sub>	Fall Time	—	5.6	—		
C <sub>iss</sub>	Input Capacitance	—	560	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	102	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	48	—		f = 1.0MHz

**Avalanche Characteristics**

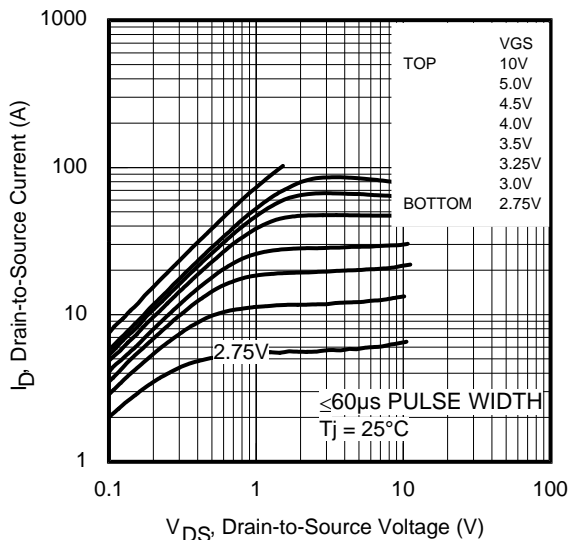
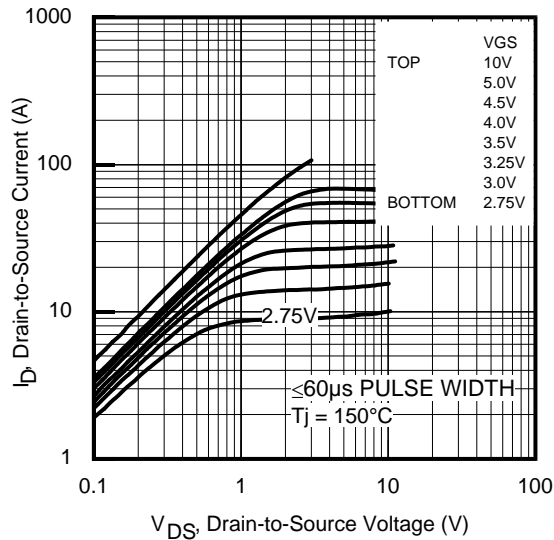
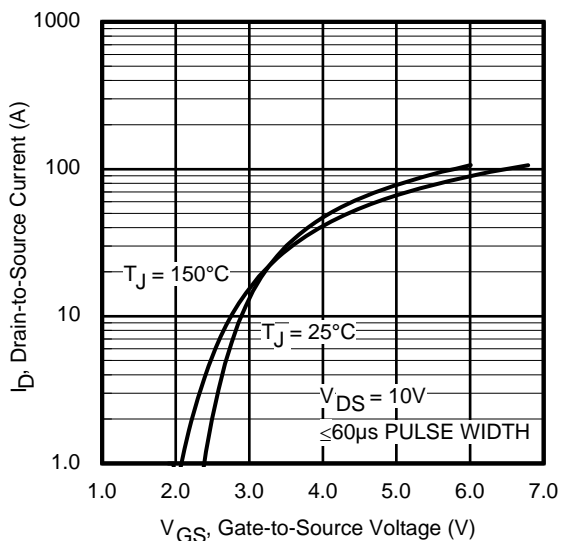
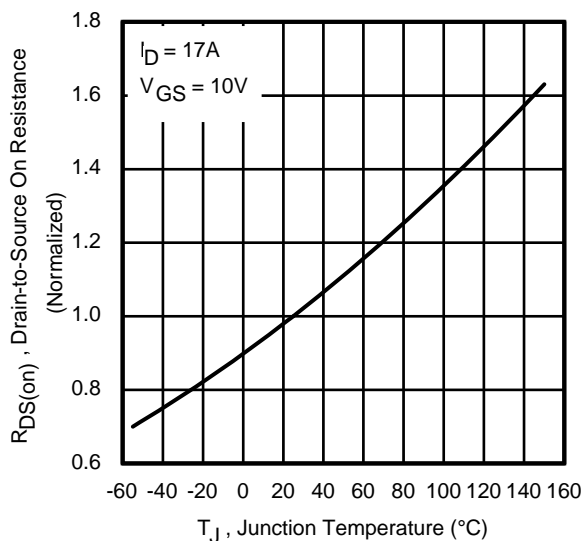
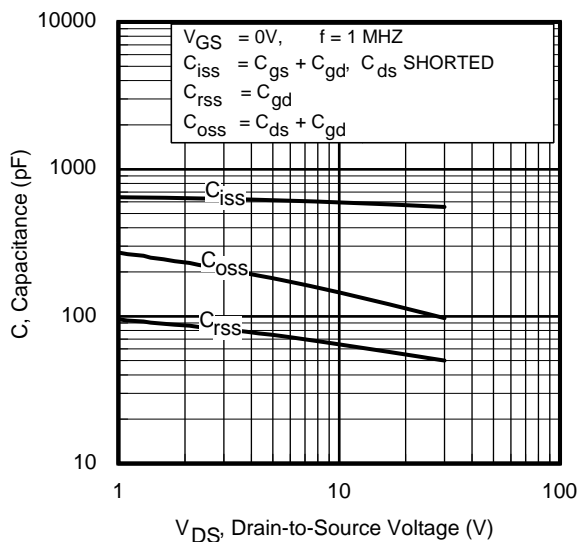
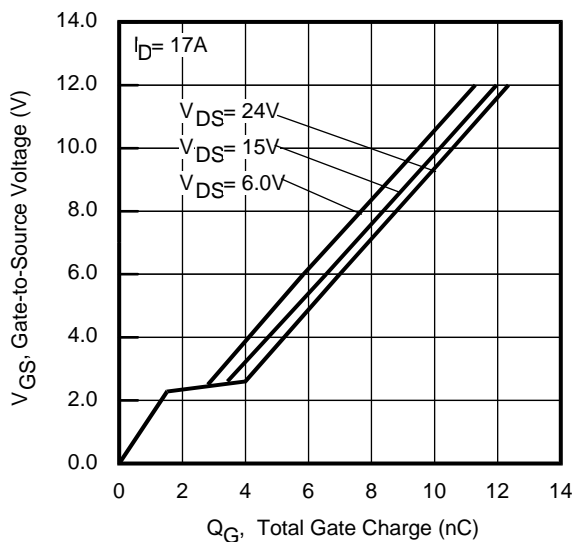
	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	21	mJ

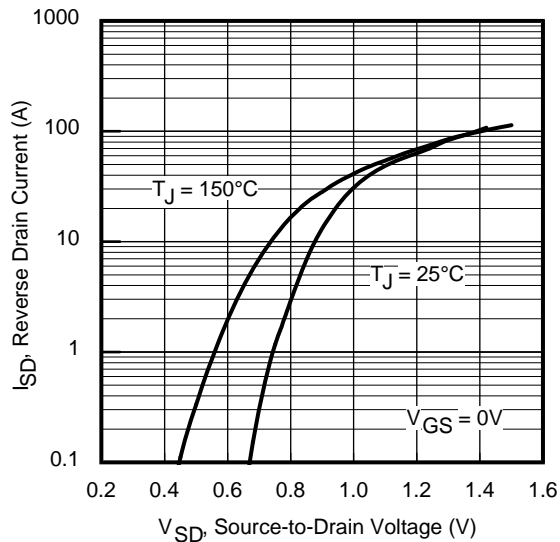
**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	20⑦	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	112		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.0	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 17A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	9.4	14	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 17A, V <sub>DD</sub> = 15V
Q <sub>rr</sub>	Reverse Recovery Charge	—	5.8	8.7	nC	di/dt = 330A/μs ③

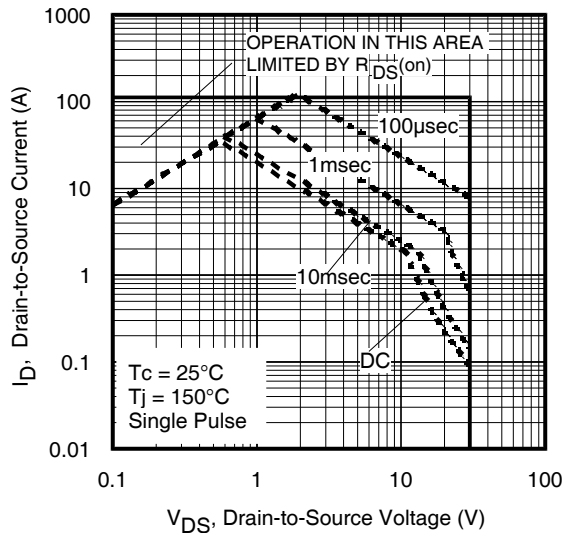
**Thermal Resistance**

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub> (Bottom)	Junction-to-Case ④	—	6.2	°C/W
R <sub>θJC</sub> (Top)	Junction-to-Case ④	—	50	
R <sub>θJA</sub>	Junction-to-Ambient ⑤	—	49	
R <sub>θJA</sub> (<10s)	Junction-to-Ambient ⑤	—	34	

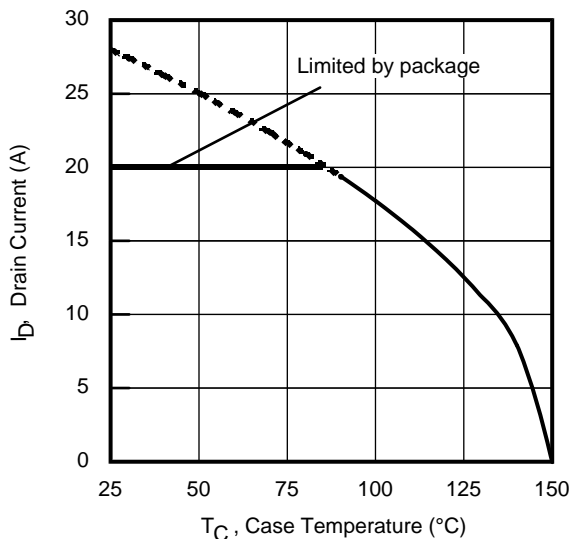

**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. Typical Transfer Characteristics**

**Fig 4. Normalized On-Resistance vs. Temperature**

**Fig 5. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage**



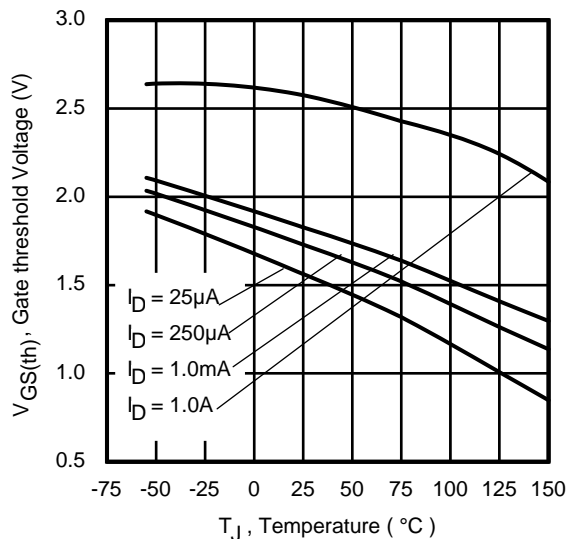
**Fig 7.** Typical Source-Drain Diode Forward Voltage



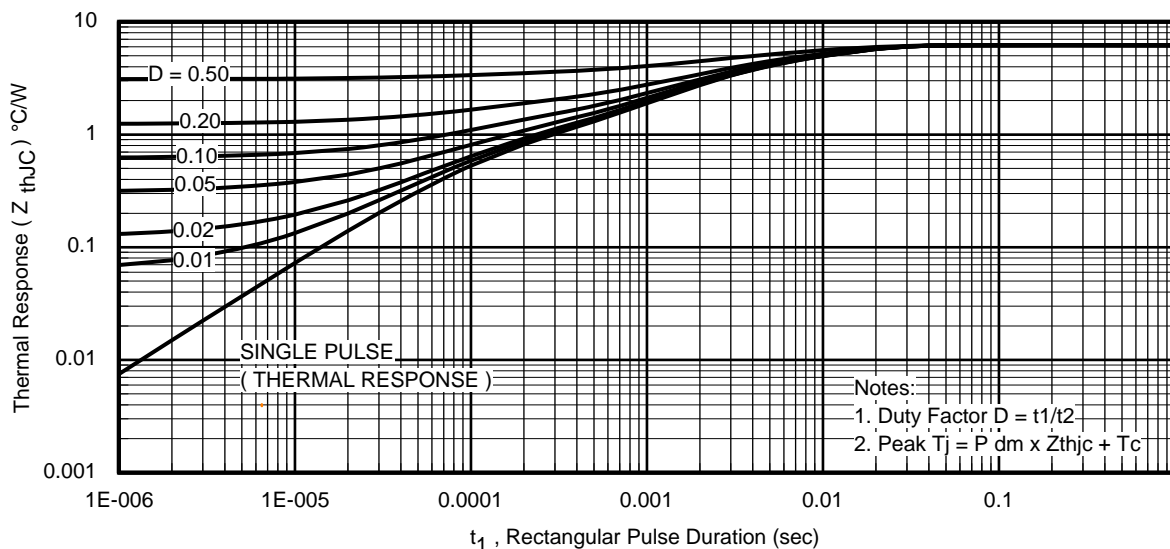
**Fig 8.** Maximum Safe Operating Area



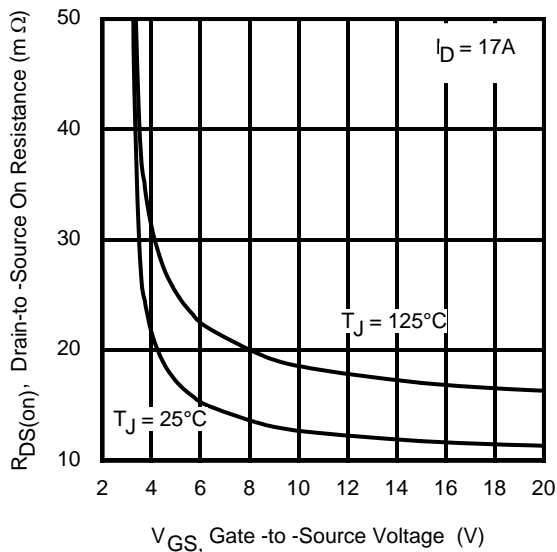
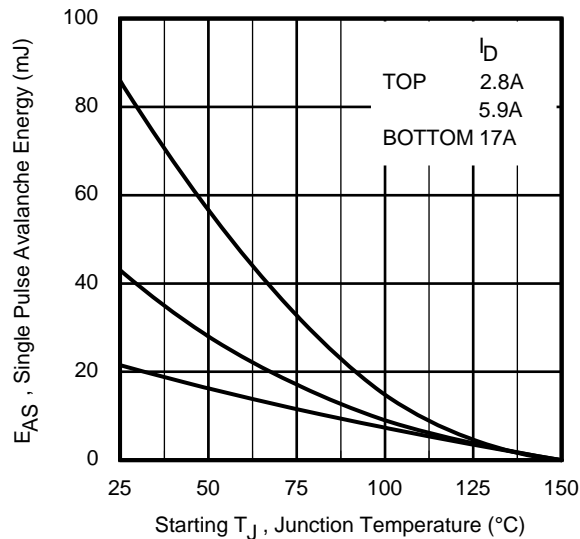
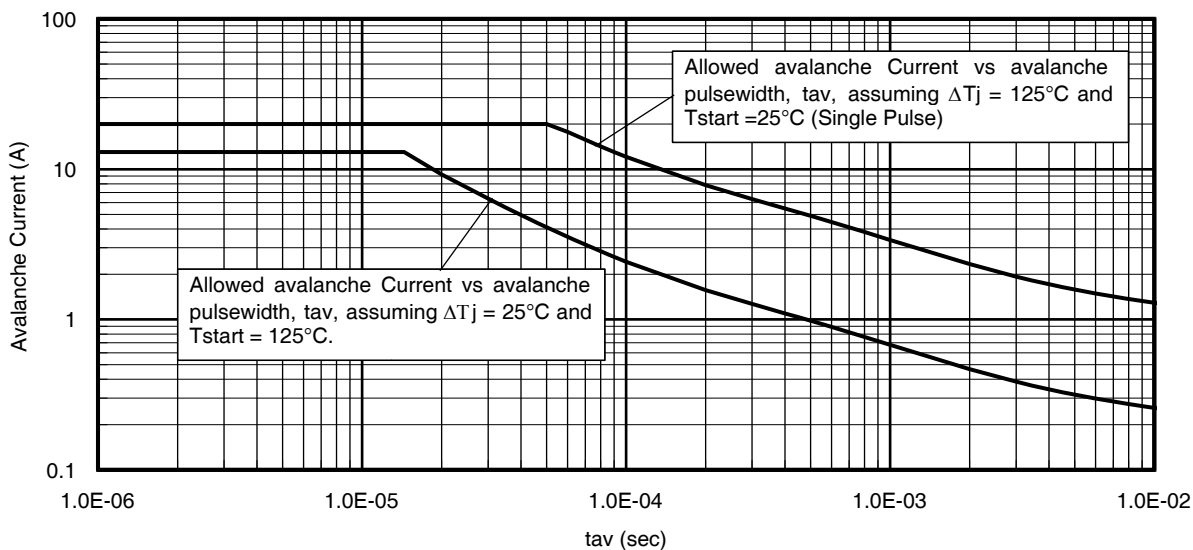
**Fig 9.** Maximum Drain Current vs. Case Temperature

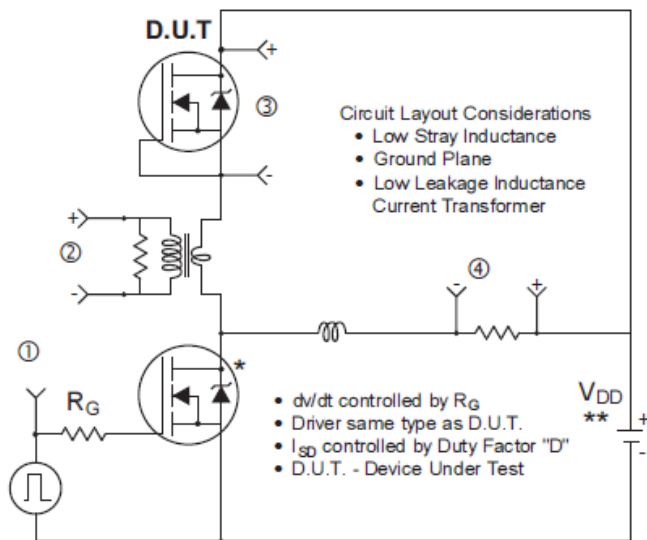


**Fig 10.** Drain-to-Source Breakdown Voltage



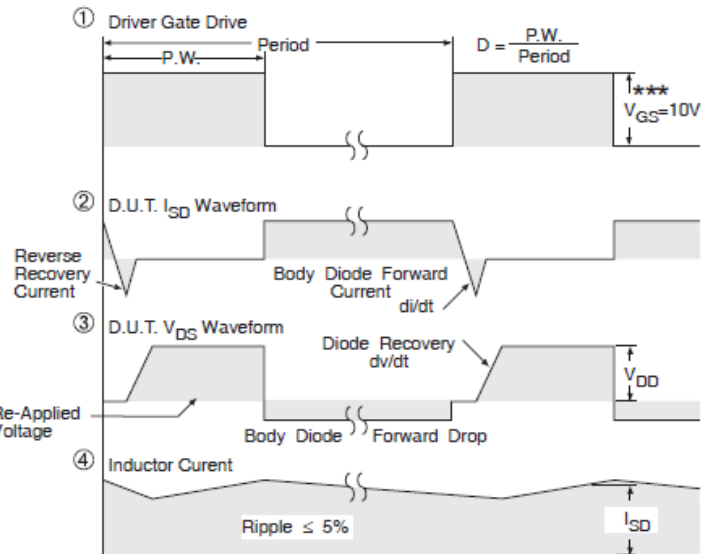
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case


**Fig 12.** On-Resistance vs. Gate Voltage

**Fig 13.** Maximum Avalanche Energy vs. Drain Current

**Fig 14.** Single Avalanche Event: Pulse Current vs. Pulse Width

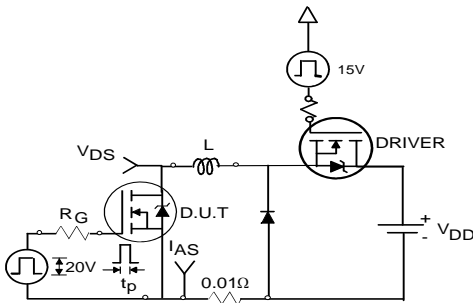


\* Use P-Channel Driver for P-Channel Measurements  
 \*\* Reverse Polarity for P-Channel

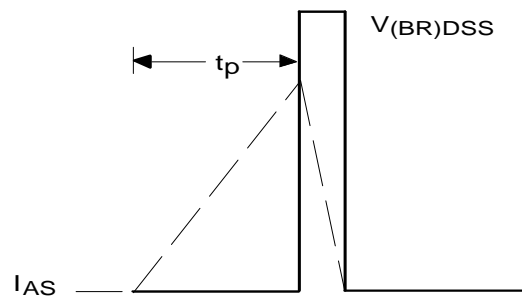
**Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET<sup>®</sup> Power MOSFETs**



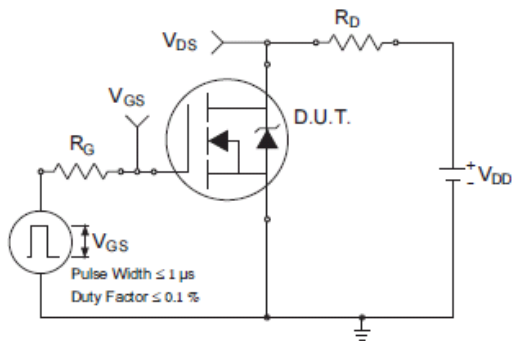
\*\*\*  $V_{GS} = 5V$  for Logic Level Devices



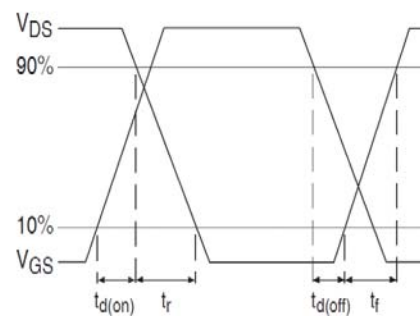
**Fig 16a. Unclamped Inductive Test Circuit**



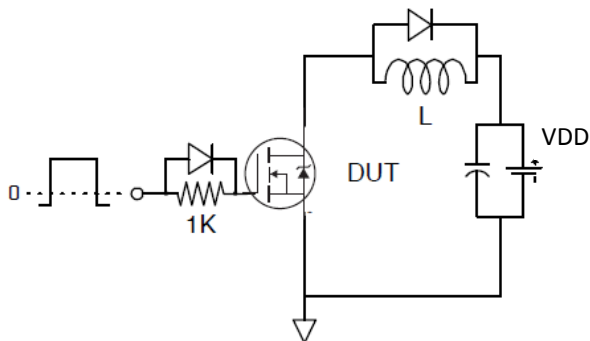
**Fig 16b. Unclamped Inductive Waveforms**



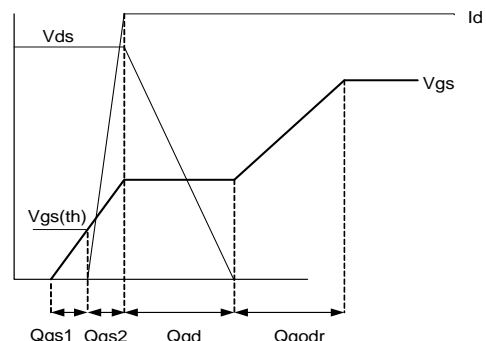
**Fig 17a. Switching Time Test Circuit**



**Fig 17b. Switching Time Waveforms**



**Fig 18. Gate Charge Test Circuit**



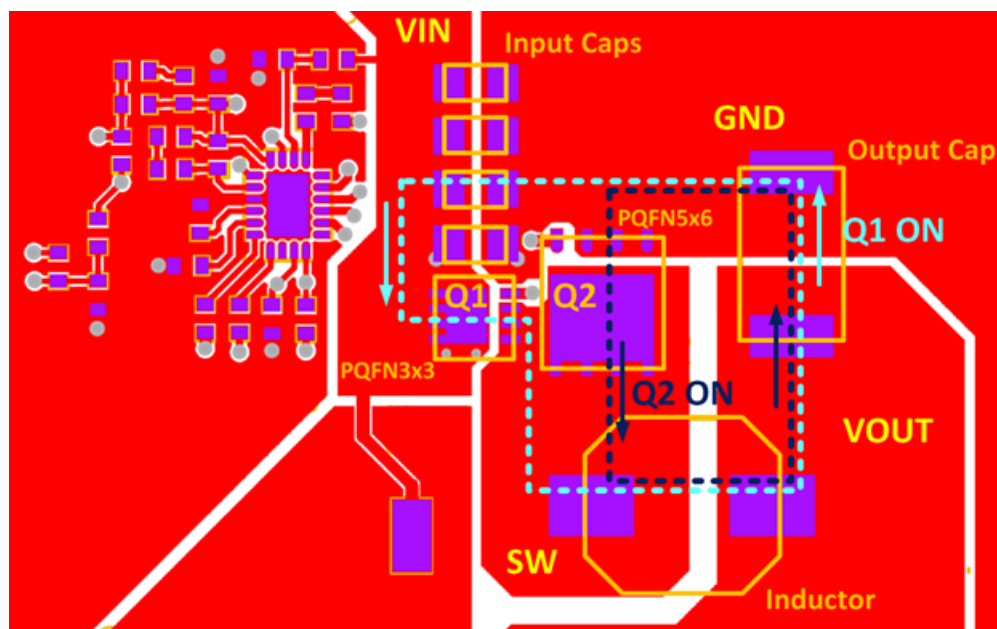
**Fig 19. Gate Charge Waveform**

### Placement and Layout Guidelines

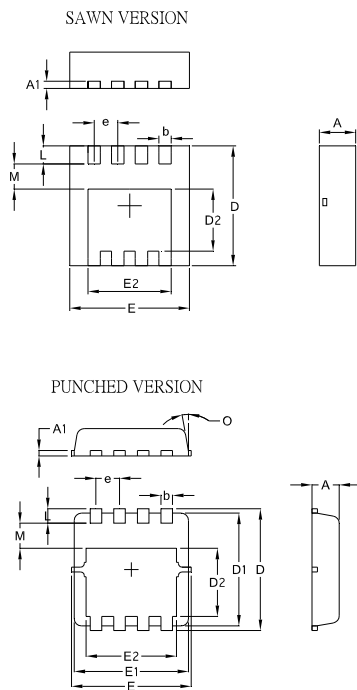
The typical application topology for this product is the synchronous buck converter. These converters operate at high frequencies (typically around 400 kHz). During turn-on and turn-off switching cycles, the high di/dt currents circulating in the parasitic elements of the circuit induce high voltage ringing which may exceed the device rating and lead to undesirable effects. One of the major contributors to the increase in parasitics is the PCB power circuit inductance.

This section introduces a simple guideline that mitigates the effect of these parasitics on the performance of the circuit and provides reliable operation of the devices.

To reduce high frequency switching noise and the effects of Electromagnetic Interference (EMI) when the control MOSFET (Q1) is turned on, the layout shown in Figure 20 is recommended. The input bypass capacitors, control MOSFET and output capacitors are placed in a tight loop to minimize parasitic inductance which in turn lowers the amplitude of the switch node ringing, and minimizes exposure of the MOSFETs to repetitive avalanche conditions.



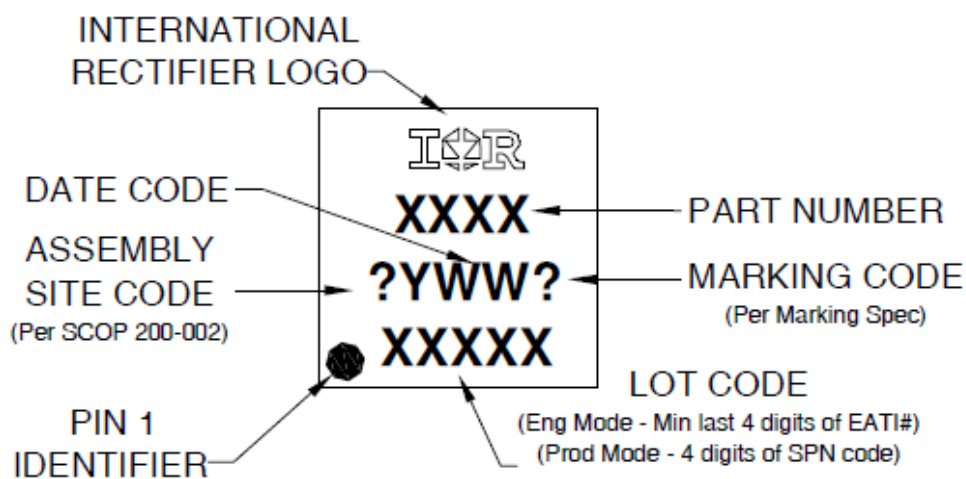
**Fig 20.** Placement and Layout Guidelines

**PQFN 3.3 x 3.3 Package Details**


SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	0.70	1.05	0.0276	0.0413
A1	0.12	0.39	0.0047	0.0154
b	0.25	0.39	0.0098	0.0154
D	3.20	3.45	0.1260	0.1358
D1	3.00	3.20	0.1181	0.1417
D2	1.69	2.20	0.0665	0.0866
E	3.20	3.40	0.1260	0.1339
E1	3.00	3.20	0.1181	0.1417
E2	2.15	2.59	0.0846	0.1020
e	0.65 BSC		0.0256 BSC	
L	0.15	0.55	0.0059	0.0217
M	0.59	—	0.0232	—
O	9Deg	12Deg	9Deg	12Deg

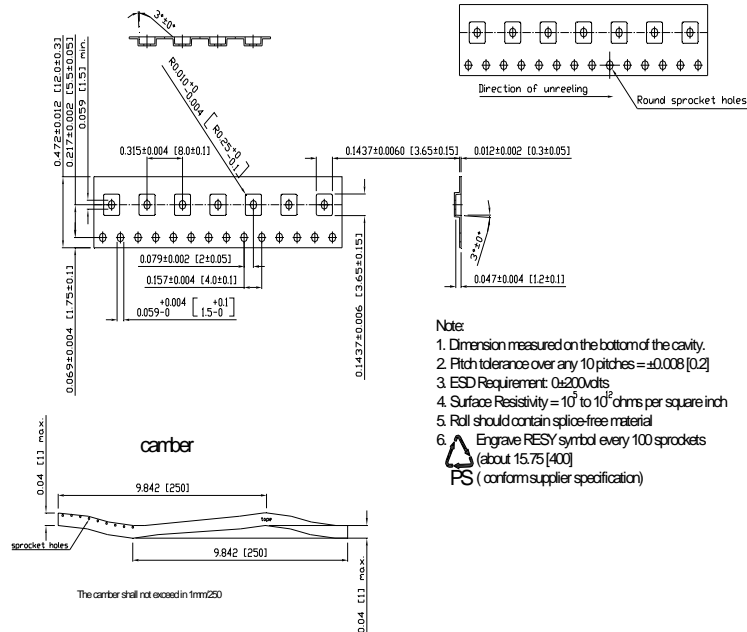
For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

**PQFN 3.3 x 3.3 Part Marking**


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



**PQFN 3.3 x 3.3 Tape and Reel**


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information†**

<b>Qualification Level</b>	Consumer (per JEDEC JESD47F <sup>††</sup> guidelines)	
<b>Moisture Sensitivity Level</b>	PQFN 3.3mm x 3.3mm	MSL1 (per JEDEC J-STD-020D <sup>††</sup> )
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.15\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 17\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑤ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details: <http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Current is limited to 20A by source bonding technology.