Integrated Device Technology, Inc.

512K x 8 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7M4048
IDT7MB4048

FEATURES:

- High density 4 megabit (512K x 8) static RAM module
- Equivalent to the JEDEC standard for future monolithic 512K x 8 static RAMs
- Fast access time: 30ns (max.)
- Low power consumption (commercial grade L version)
  - — Active: 110mA (max.)
  - — CMOS Standby: 8mA (max.)
- Very low power version (commercial grade SCD 4591)
  - — Data Retention: 200µA (max.) Vcc = 2V
  - — CMOS Standby: 400µA (max.)
- Surface mounted plastic packages or leadless chip carriers on a 32-pin, 600 mil ceramic DIP substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible

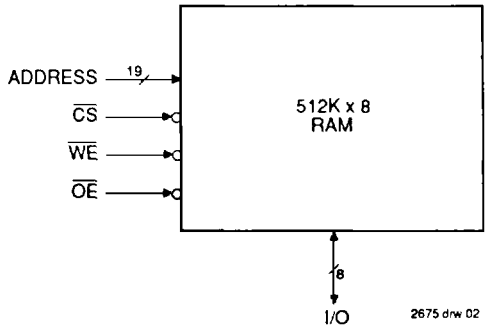
DESCRIPTION:

The IDT7M4048/7MB4048 is a 4 megabit (512K x 8) static RAM module constructed on a co-fired ceramic or multilayer epoxy laminate (FR-4) substrate using four 1 Megabit static RAMS and a decoder. The IDT7M4048/ 7MB4048 is available with access times as fast as 30ns. For battery backup applications, a very low power version is available, offering a data retention current of 200µA.

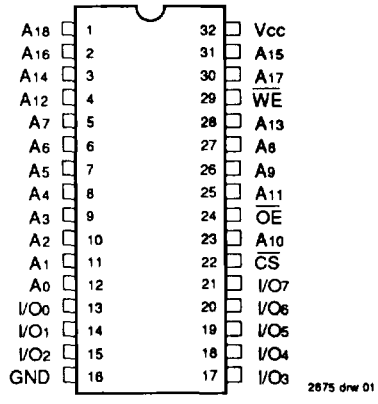
The IDT7M4048 is packaged in a 32-pin ceramic DIP. This results in a package 1.7 inches long and 600 mils wide, packing 4 megabits into the JEDEC DIP footprint. The IDT7MB4048 likewise is packaged in a 32-pin FR-4 DIP resulting in the same JEDEC footprint in a package 1.6 inches long and 600 mils wide.

All inputs and outputs of the IDT7M4048 and 7MB4048 are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use. All IDT military module semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883 Class B, making them ideally suited for applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION[1]



DIP
TOP VIEW

PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-18	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2675 tbl 01

NOTE:
1. For module dimensions, please refer to module drawing M3, M4, or M5 (7M4048L, 7M4048S, 7MB4048S) in the packaging section.

8

CEMOS is a trademark of Integrated Device Technology Inc.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

2675 tbl 09

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
$C_{IN(C)}$	Input Capacitance ($\overline{CS}$)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	35	pF

NOTE: 2675 tbl 10
1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2675 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2675 tbl 03
1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%
Military	-55°C to +125°C	0V	5V ±10%

2675 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	Test Conditions	7M4048LxxN (COM'L ONLY)		7MB4048SxxP 7M4048SxxC 7M4048SxxCB (COM'L)		(MILITARY)		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	4	—	8	—	40	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	4	—	8	—	40	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2mA[2], I_{OL} = 8mA[3]	—	0.4	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -1mA[2], I_{OH} = –4mA[3]	2.4	—	2.4	—	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \le V_{IL}$; f = f_{MAX}, Outputs Open	—	110	—	360	—	480	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS} \ge V_{IH}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	—	12	—	240	—	240	mA
I_{SB1}[1]	Full Standby Supply Current (CMOS Levels)	$\overline{CS} \ge V_{CC}$ - 0.2V, $V_{IN} \ge V_{CC}$ - 0.2V or ≤ 0.2V	—	8	—	40	—	80	mA

NOTES: 2675 tbl 05
1. For low power version I_{SB1} = 400µA, refer to SCD4591 when ordering. For Commercial grade 7M4048L version only
2. For Commercial grade 7M4048L version only.
3. For 7MB4048SxxP, 7M4048SxxC, and 7M4048SxxCB versions.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2675 tbl 07

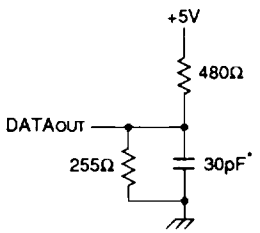


Figure 1. Output Load

* Including scope and jig

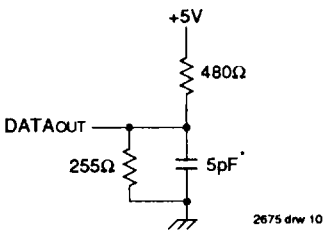


Figure 2. Output Load
(for tOLZ, tCHZ, tOHZ, tWHZ, tOW and tCLZ)

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	7M4048S30C 7MB4048S30P		7M4048S35C 7MB4048S35P		7M4048S40C 7M4048S40CB 7MB4048S40P		7M4048S45C 7M4048S45CB 7MB4048S45P		7M4048S50C 7M4048S50CB 7MB4048S50P		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tRC	Read Cycle Time	30	—	35	—	40	—	45	—	50	—	ns
tAA	Address Access Time	—	30	—	35	—	40	—	45	—	50	ns
tACS	Chip Select Access Time	—	30	—	35	—	40	—	45	—	50	ns
tOE	Output Enable to Output Valid	—	11	—	15	—	20	—	25	—	30	ns
tOHZ(1)	Output Disable to Output in High Z	—	10	—	15	—	20	—	20	—	20	ns
tOLZ(1)	Output Enable to Output in Low Z	2	—	2	—	5	—	5	—	5	—	ns
tCLZ(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tCHZ(1)	Chip Deselect to Output in High Z	—	16	—	20	—	20	—	20	—	20	ns
tOH	Output Hold from Address Change	3	—	3	—	5	—	5	—	5	—	ns
tPU(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD(1)	Chip Deselect to Power-Down Time	—	30	—	35	—	40	—	45	—	50	ns
Write Cycle												
tWC	Write Cycle Time	30	—	35	—	40	—	45	—	50	—	ns
tWP	Write Pulse Width	20	—	25	—	30	—	35	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	5	—	5	—	5	—	ns
tAW	Address Valid to End of Write	25	—	30	—	35	—	40	—	45	—	ns
tCW	Chip Select to End of Write	25	—	30	—	35	—	40	—	45	—	ns
tDS	Data Set-up Time	—	—	—	—	—	—	—	—	—	—	ns
tDH	Data Hold Time	3	—	3	—	3	—	5	—	5	—	ns
tWR	Write Recovery Time	3	—	3	—	5	—	5	—	5	—	ns
tWHZ(1)	Write Enable to Output in High Z	—	11	—	15	—	15	—	15	—	20	ns
tOW(1)	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2675 tbl 08

8

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C and -55°C to +125°C)

Symbol	Parameter	7M4048S60C 7M4048S60CB 7MB4048S60P		7M4048S70C 7M4048S70CB 7M4048L70N		7M4048S85C 7M4048S85CB 7M4048L85N		7M4048S100C 7M4048S100CB 7M4048L100N		7M4048S120C 7M4048S120CB 7M4048L120N		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	60	—	70	—	85	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	60	—	70	—	85	—	100	—	120	ns
t_{ACS}	Chip Select Access Time	—	60	—	70	—	85	—	100	—	120	ns
t_{OE}	Output Enable to Output Valid	—	35	—	45	—	48	—	50	—	60	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	25	—	30	—	33	—	35	—	40	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	5	—	0	—	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	25	—	40	—	43	—	45	—	50	ns
t_{OH}	Output Hold from Address Change	5	—	10	—	10	—	10	—	10	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	60	—	70	—	85	—	100	—	120	ns
Write Cycle												
t_{WC}	Write Cycle Time	60	—	70	—	85	—	100	—	120	—	ns
t_{WP}	Write Pulse Width	50	—	55	—	65	—	75	—	90	—	ns
t_{AS}	Address Set-up Time	5	—	0	—	2	—	5	—	5	—	ns
t_{AW}	Address Valid to End of Write	55	—	65	—	82	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	55	—	65	—	80	—	85	—	100	—	ns
t_{DS}	Data Set-up Time			35	—	38	—	40	—	45	—	ns
t_{DH}	Data Hold Time	5	—	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	5	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	25	—	30	—	33	—	35	—	40	ns
t_{OW}[1]	Output Active from End of Write	5	—	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

2675 tbl 08

DATA RETENTION CHARACTERISTICS[1, 4]

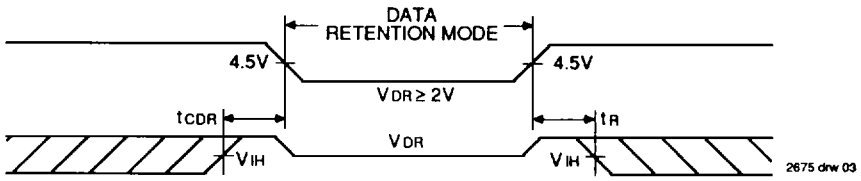
(T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min.	Max. V_{CC} @ 2.0V	Unit
V_{DR}	V_{CC} for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ - 0.2V	—	200	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC}$ - 0.2V or	0	—	ns
t_R[3]	Operation Recovery Time	$V_{IN} \geq$ 0.2V	t_{RC}[2]	—	ns

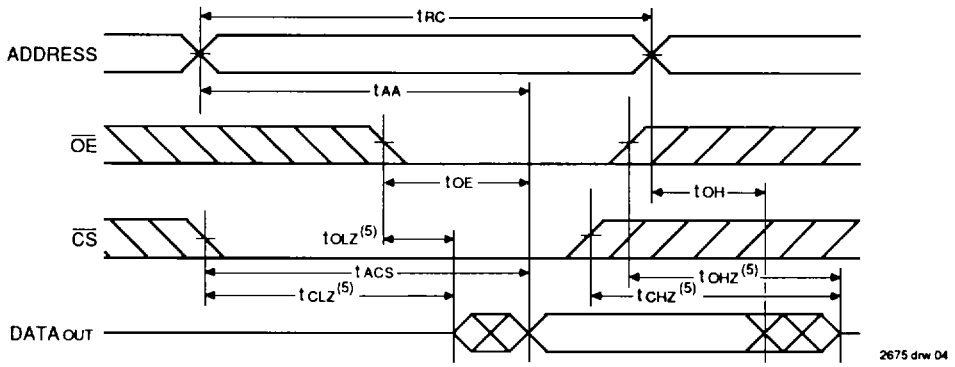
NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by design, but not tested.
4. This option is only offered when ordering to 7M4048LxxN SCD4591.

2675 tbl 09

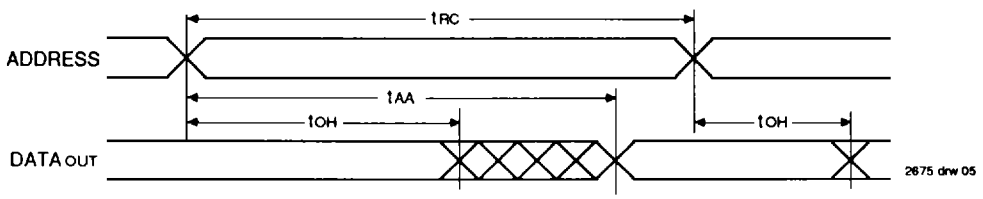
DATA RETENTION WAVEFORM



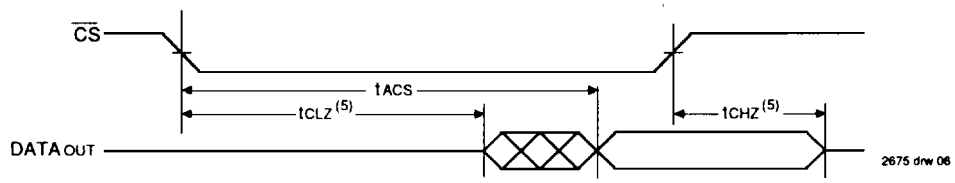
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



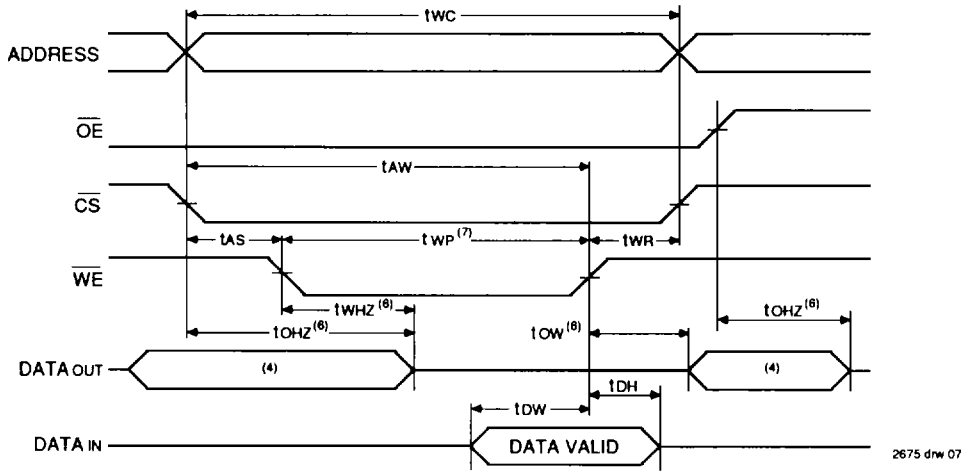
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



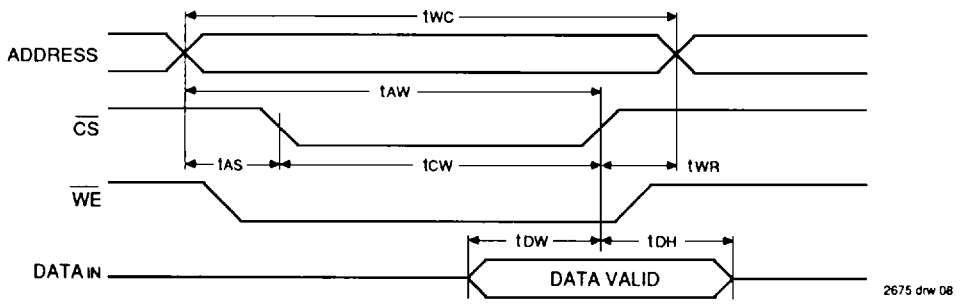
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guranateed by design, but not tested.

8

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

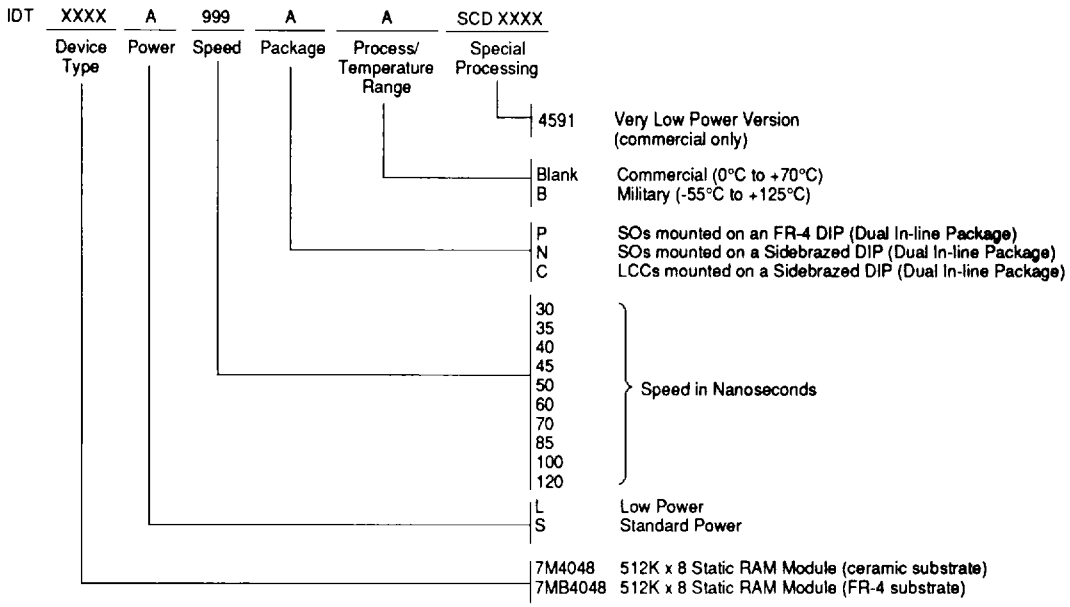


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, write pulse ((tWP) > tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION



2675 drw 09

8