Advanced Micro **Devices**

Am82520

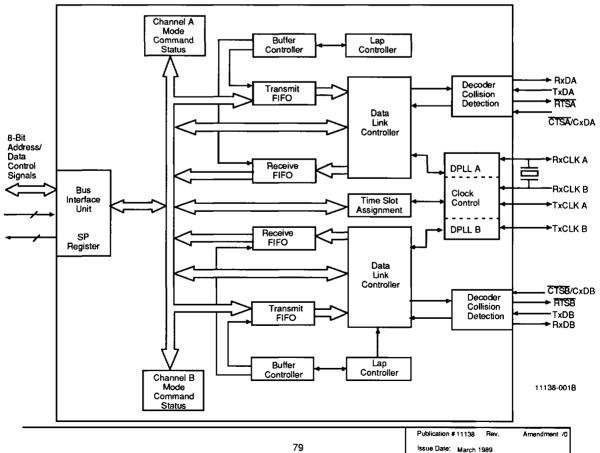
High-Level Serial Communications Controller (HSCC)

DISTINCTIVE CHARACTERISTICS

- Two independent HDLC channels
- Implementation of X.25 LAPB/LAPD protocol
- Programmable timeout and retry conditions
- FIFO buffers for efficient transfer of data packets
- Digital phase locked loop for each channel
- Baud rate generator and oscillator
- Different modes for clock recovery and data encoding
- High-speed data rate (up to 4 MHz)
- Supports bus configuration by collision resolution

- Telecom-specific features programmable
- 8-bit parallel µP interface
- Advanced CMOS technology
- Low power consumption: active: 25 mW at 4 MHz standby: 3 mW
- Package: 28-Pin Plastic DIP or 28-Pin Plastic Leaded Chip Carrier
- Operating temperature 0 to +70° C
- Industrial: operating temperature -40 to +85°C

BLOCK DIAGRAM



GENERAL DESCRIPTION

The Am82520, High-Level Serial Communications Controller (HSCC), has been designed to free the user from tasks occurring in communication with networks and trunk lines. It is an X.25 LAPB/LAPD controller which to a large degree performs communication procedures independent of CPU support.

A parallel processor bus constitutes the microprocessor system. The serial communications interface consists of two full-duplex HDLC channels that can be operated independently from one another. The HSCC is connected to the transmission line by additional line drivers or mo-

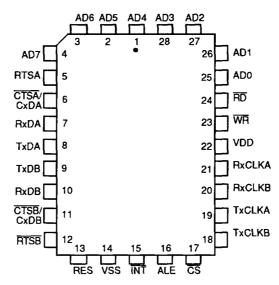
dems. The need for external hardware is reduced because of added functions on-chip. The functions incorporated include an oscillator, DPLL (one per channel), programmable baud rate generator, and time slot assigner.

The chip contains a serial interface for two channels including a DPLL and collision-detection block, a datalink controller, and FIFO buffers. The μP interface, including the status and command registers, is used for both channels. The HSCC is implemented in a 2 micron CMOS technology.

CONNECTION DIAGRAMS Top View

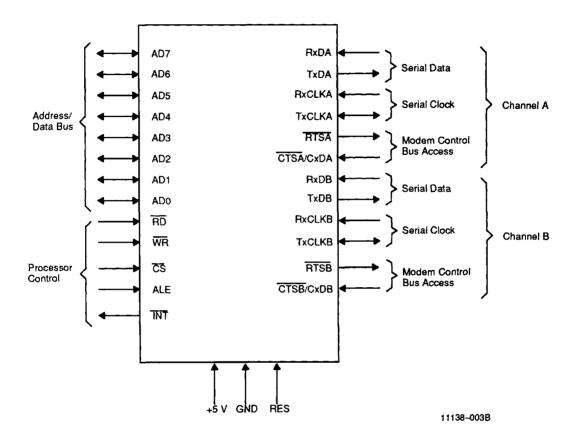
28-Pin PDIP AD4 28 AD3 AD2 AD5 2 27 AD6 3 AD1 26 AD7 AD0 25 4 RTSA RD 5 24 CTSA/CxDA WR 6 23 7 22 RxDA VDD TxDA **RxCLKA** 8 21 TxDB[9 **RxCLKB** 20 RxDB [19 **TxCLKA** 10 CTSB/CXDB **TxCLKB** 11 18 ĊS RTSB 12 17 RES 7 ALE 13 16 INT V_{ss}[14 15

28-Pin PLCC



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

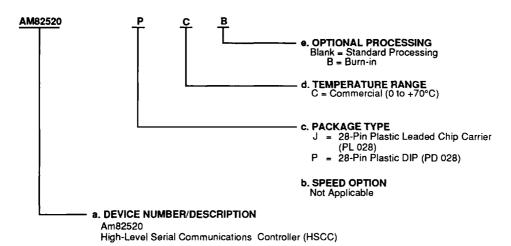


ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable) c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM82520	PC, JC, PCB, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly re-leased combinations, and to obtain additional data on AMD's standard military grade products.