Radiation Hardened High Speed, Quad SPST, CMOS Analog Switch

HS-201HSRH, HS-201HSEH

The HS-201HSRH, HS-201HSEH are monolithic CMOS analog switch featuring power-off high input impedance, very fast switching speeds and low ON-resistance. Fabrication on our DI RSG process assures SEL immunity and only very slight sensitivity to low dose rate (ELDRS). These Class V/Q devices are tested and guaranteed for 300krad (Si) total dose performance.

Power-off high input impedance enables the use of this device in redundant circuits without causing data bus signal degradation. ESD protection, overvoltage protection, fast switching times, low ON-resistance, and guaranteed radiation hardness, make the HS-201HSRH ideal for any space application where improved switching performance is required.

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-99618. A "hot-link" is provided on our homepage for downloading.

Features

- Electrically screened to DLA SMD# 5962-99618
- QML qualified per MIL-PRF-38535
- Radiation performance
  - High dose rate (50-300rad(Si)/s) . . . . . 300krad(Si)
  - Low dose rate (0.01rad(SI)/s) . . . . . 50krad(Si)
  - SEL immune . . . . . DI RSG process
- Overvoltage protection (power on, switch off) . . . . . ±30V
- Power off high impedance . . . . . ±17V
- Fast switching times
  - t_{ON} . . . . . 110ns (max)
  - t_{OFF} . . . . . 80ns (max)
- Low "ON" resistance . . . . . 50Ω (max)
- Pin compatible with industry standard 201 types
- Operating supply range . . . . . ±10V to ±15V
- Wide analog voltage range (±15V supplies) . . . . . ±15V
- TTL compatible

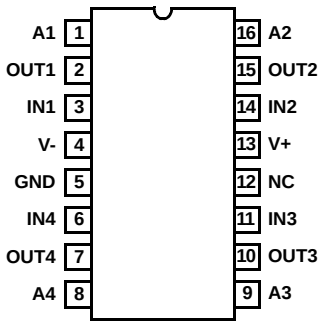
Applications

- High speed multiplexing
- Sample and hold circuits
- Digital filters
- Operational amplifier gain switching networks

Integrator reset circuits

Pin Configuration

HS1-201HSRH, HS1-201HSEH SBDIP (CDIP2-T16)
HS9-201HSRH, HS9-201HSEH FLATPACK (CDFP4-F16)
TOP VIEW



Ordering Information

ORDERING SMD NUMBER (Note 3)	INTERNAL MKT. NUMBER (Notes 1, 2)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962F9961801VEC	HS1-201HSRH-Q	Q 5962F99 61801VEC	-55 to +125	16 Ld SBDIP	D16.3
5962F9961802VEC	HS1-201HSEH-Q	Q 5962F99 61802VEC	-55 to +125	16 Ld SBDIP	D16.3
5962F9961801QEC	HS1-201HSRH-8	Q 5962F99 61801QEC	-55 to +125	16 Ld SBDIP	D16.3
5962F9961801VXC	HS9-201HSRH-Q	Q 5962F99 61801VXC	-55 to +125	16 Ld Flatpack	K16.A
5962F9961802VXC	HS9-201HSEH-Q	Q 5962F99 61802VXC	-55 to +125	16 Ld Flatpack	K16.A
5962F9961801QXC	HS9-201HSRH-8	Q 5962F99 61801QXC	-55 to +125	16 Ld Flatpack	K16.A
5962F9961801V9A	HS0-201HSRH-Q		-55 to +125	Die	
5962F9961802V9A	HS0-201HSEH-Q		-55 to +125	Die	
HS1-201HSRH/PROTO	HS1-201HSRH/PROTO	HS1-201HSRH/PROTO	-55 to +125	16 Ld SBDIP	D16.3
HS9-201HSRH/PROTO	HS9-201HSRH/PROTO	HS9-201HSRH/PROTO	-55 to +125	16 Ld Flatpack	K16.A
HS0-201HSRH/SAMPLE	HS0-201HSRH/SAMPLE		-55 to +125	Die	

NOTE:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. For Moisture Sensitivity Level (MSL), please see device information page for HS-201HSRH, HS-201HSEH. For more information on MSL, please see tech brief TB363.
3. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the “Ordering Information” table on page 2 must be used when ordering

Die Characteristics

DIE DIMENSIONS

2790µm x 4950µm (110 mils x 195 mils)
Thickness: 483µm ±25.4µm (19 mils ±1 mil)

INTERFACE MATERIALS

Glassivation

Type: Phosphorus Silicon Glass (PSG)
Thickness: 8.0kÅ ±1.0kÅ

Metallization

Type: Ti/AlCu
Thickness: 16.0kÅ ± 2kÅ

Substrate

Rad Hard Silicon Gate, Dielectric Isolation

Backside Finish

Silicon

ASSEMBLY RELATED INFORMATION

Substrate Potential

Unbiased (DI)

ADDITIONAL INFORMATION

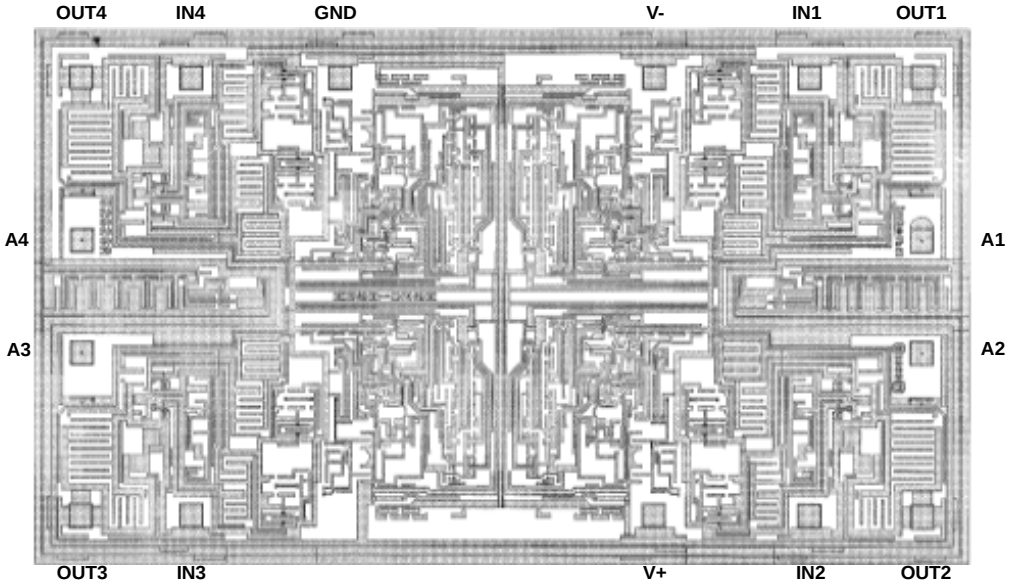
Worst Case Current Density

$< 2.0 \times 10^5$ A/cm^2

Transistor Count

328

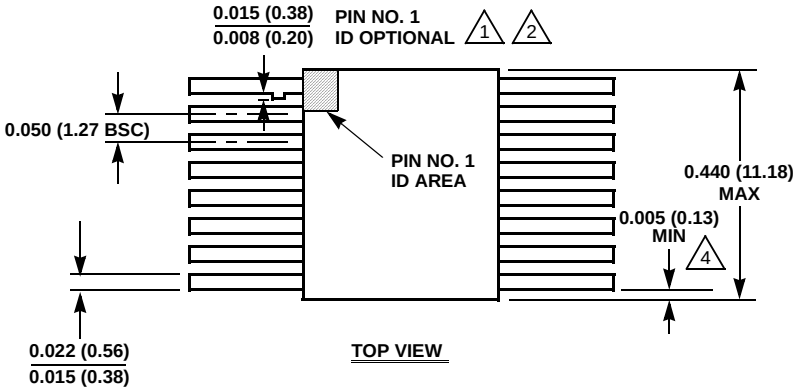
Metallization Mask Layout

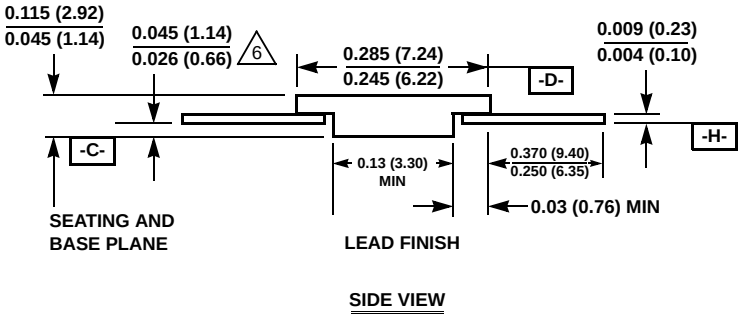


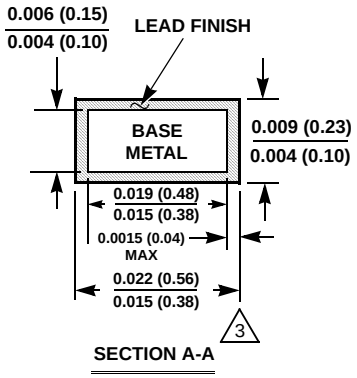
Package Outline Drawing

K16.A

16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE
Rev 2, 1/10



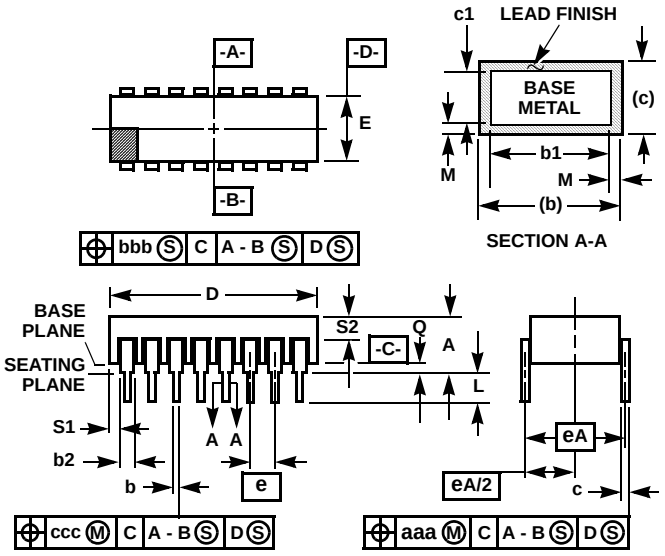




NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

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