TOSHIBA CDMOS Integrated Circuit Silicon Monolithic

TC62D749CFG

16-Output Constant Current LED Driver (Output switching high-speed version)

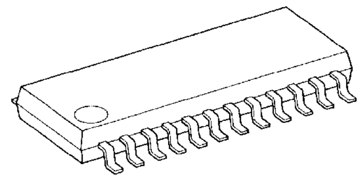
The TC62D749CFG is a constant-current driver for LED and LED display lighting applications.

The output current from each of the 16 outputs is programmable via a single external resistor.

The TC62D749CFG contains a 16-channel shift register, a 16-channel latch, a 16-channel AND gate and a 16-channel constant-current output.

Fabricated with a CMOS process, the TC62D749CFG allows high-speed data transfer.

It operates with a 3.3- or 5-V power supply.



SSOP24-P-300-1.00B

Weight: 0.29 g (Typ.)

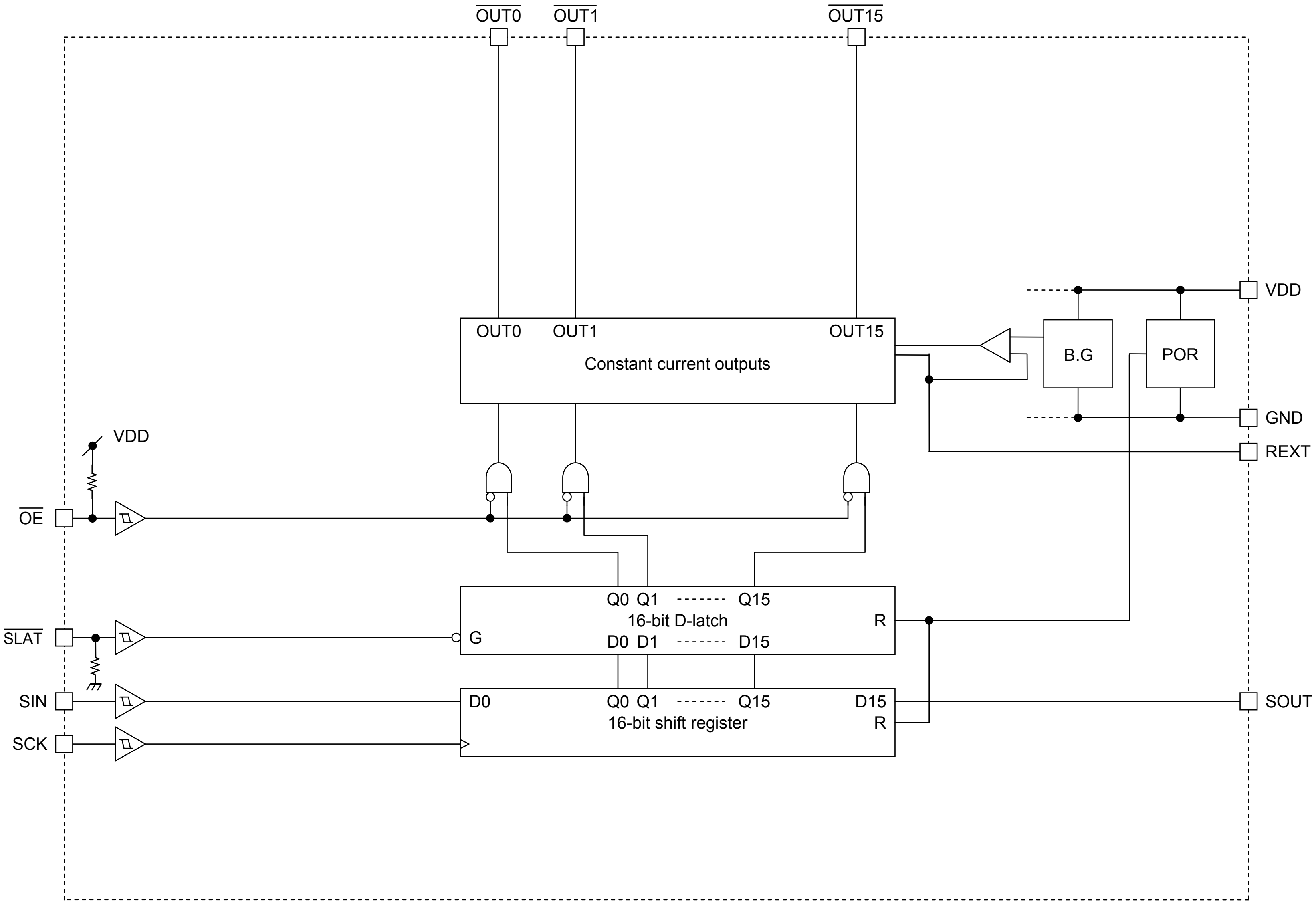
Features

- Supply voltages : V_{DD} = 3.0 V to 5.5 V
- 16-output built-in
- Output current setup range : I_{OUT} = 1.5 to 90 mA
- Constant current output accuracy (@ R_{EXT} = 1.2 kΩ, V_{OUT} = 1.0 V, V_{DD} = 3.3 V, 5.0 V)
  - : S rank ; between outputs ± 1.5 % (max)
  - : S rank ; between devices: ± 1.5 % (max)
  - : N rank ; between outputs ± 2.5 % (max)
  - : N rank ; between devices: ± 2.5 % (max)
- Output voltage : V_{OUT} = 17 V (max)
- High-speed output switching : t_{wOE} = 25 ns (min), t_{or} = 10ns (typ.), t_{of} = 10ns (typ.)
  There is TC62D748 as an output switching standard-speed version of this product.
- I/O interface : CMOS interfaces (Schmitt trigger input)
- Data transfer frequency : f_{SCK} = 25 MHz (max)
- Operation temperature range : T_{opr} = −40 to 85 °C
- Power-on-reset function built-in. (When the power supply is turned on, internal data is reset)
- Package : SSOP24-P-300-1.00B

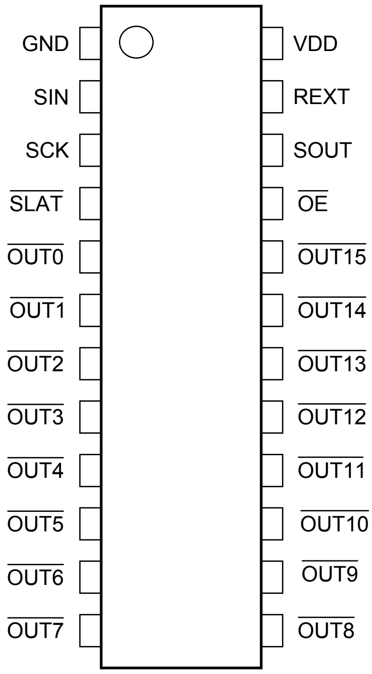
For detailed part naming conventions, contact your local Toshiba sales representative or distributor.

When the LED driver of high-speed output switching is used, back EMF may occur at the time of output OFF, and output terminal voltage may rise. Please be careful. It is necessary to reduce inductance to prevent the back EMF. It is possible to reduce inductance of a substrate by making the power supply for LED wiring shorter and wider designing the layout pattern.

Block Diagram



Pin Assignment (top view)



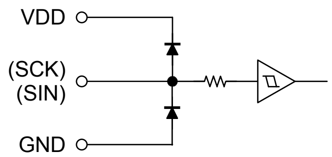
Short circuiting an output pin to a power supply pin (Power-supply voltage V_{DD} and LED anode power supply), or short-circuiting the REXT pin to the GND pin will likely exceed the absolute maximum ratings, which in turn may result in smoldering and/or permanent damage. Please keep this in mind when determining the wiring layout for the power supply and GND pins.

Pin Functions

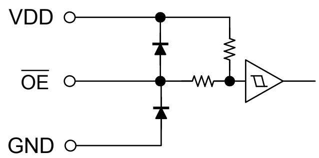
Pin No	Pin Name	I/O	Function
1	GND	—	GND terminal
2	SIN	I	Serial data input terminal
3	SCK	I	Serial data transfer clock input terminal
4	$\overline{\text{SLAT}}$	I	Latch signal input pin.
5	$\overline{\text{OUT0}}$	O	Constant-current output terminal
6	$\overline{\text{OUT1}}$	O	Constant-current output terminal
7	$\overline{\text{OUT2}}$	O	Constant-current output terminal
8	$\overline{\text{OUT3}}$	O	Constant-current output terminal
9	$\overline{\text{OUT4}}$	O	Constant-current output terminal
10	$\overline{\text{OUT5}}$	O	Constant-current output terminal
11	$\overline{\text{OUT6}}$	O	Constant-current output terminal
12	$\overline{\text{OUT7}}$	O	Constant-current output terminal
13	$\overline{\text{OUT8}}$	O	Constant-current output terminal
14	$\overline{\text{OUT9}}$	O	Constant-current output terminal
15	$\overline{\text{OUT10}}$	O	Constant-current output terminal
16	$\overline{\text{OUT11}}$	O	Constant-current output terminal
17	$\overline{\text{OUT12}}$	O	Constant-current output terminal
18	$\overline{\text{OUT13}}$	O	Constant-current output terminal
19	$\overline{\text{OUT14}}$	O	Constant-current output terminal
20	$\overline{\text{OUT15}}$	O	Constant-current output terminal
21	$\overline{\text{OE}}$	I	An output current enable signal input terminal In "H" level input, outputs are turned off compulsorily. In "L" level input, outputs are ON/OFF controlled according to serial data.
22	SOUT	O	Serial data output terminal.
23	REXT	—	An external resistance for an output current setup is connected between this terminal and ground.
24	VDD	—	Power supply terminal

I/O Equivalent Circuits

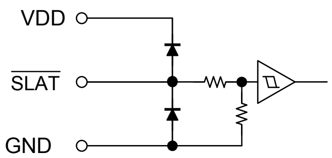
1. SCK, SIN



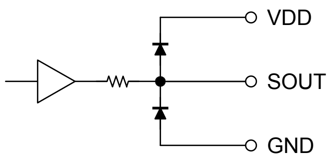
2. $\overline{\text{OE}}$



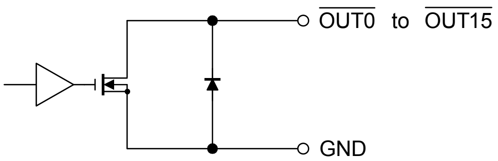
3. $\overline{\text{SLAT}}$



4. SOUT



5. $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$



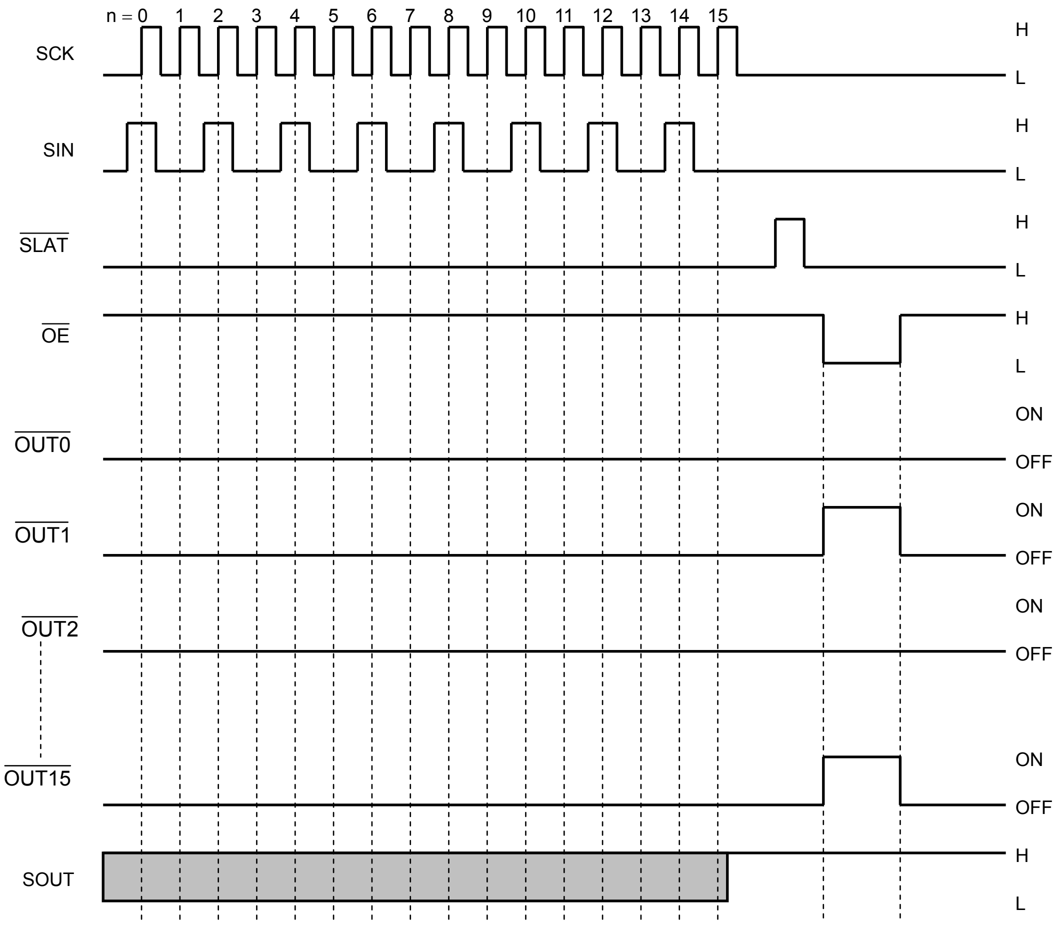
Truth Table

SCK	$\overline{\text{SLAT}}$	$\overline{\text{OE}}$	SIN	$\overline{\text{OUT0}}$ … $\overline{\text{OUT7}}$ … $\overline{\text{OUT15}}$ (Note1)	SOUT
↑	H	L	Dn	Dn … Dn − 7 … Dn − 15	Dn − 15
↑	L	L	Dn + 1	No Change	Dn − 14
↑	H	L	Dn + 2	Dn + 2 … Dn − 5 … Dn − 13	Dn − 13
↓	− (Note2)	L	Dn + 3	Dn + 2 … Dn − 5 … Dn − 13	Dn − 13
↓	− (Note2)	H	Dn + 3	OFF	Dn − 13

Note1: When $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$ output pins are set to "H" the respective output will be ON and when set to "L" the respective output will be OFF.

Note2: "-" is irrelevant to the truth table.

Timing Diagram



- The latch circuit is a leveled-latch circuit. Please exercise precaution as it is not triggered-latch circuit.
- Keep the $\overline{\text{SLAT}}$ pin is set to "L" to enable the latch circuit to hold data. In addition, when the $\overline{\text{SLAT}}$ pin is set to "H" the latch circuit does not hold data. The data will instead pass onto output.
  When the $\overline{\text{OE}}$ pin is set to "L" the $\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$ output pins will go ON and OFF in response to the data. In addition, when the $\overline{\text{OE}}$ pin is set to "H" all the output pins will be forced OFF regardless of the data.
- This product can use 3.3V and 5.0V power supply, but power supply and input (SCK/SIN/ $\overline{\text{SLAT}}$ / $\overline{\text{OE}}$) must use same voltage.

Absolute Maximum Ratings (T_a = 25°C)

Characteristics	Symbol	Rating (Note1)	Unit
Supply voltage	V_{DD}	−0.3 to 6.0	V
Output current	I_{OUT}	95	mA
Logic input voltage	V_{IN}	−0.3 to V_{DD} + 0.3 (Note2)	V
Output voltage	V_{OUT}	−0.3 to 17	V
Operating temperature	T_{opr}	−40 to 85	°C
Storage temperature	T_{stg}	−55 to 150	°C
Thermal resistance	Rth(j-a)	94 (Note3)	°C/W
Power dissipation	P_D	1.32 (Note3, 4)	W

Note1: Voltage is ground referenced.
Note2: Do not exceed 6.0V.
Note3: PCB condition 76.2 x 114.3 x 1.6 mm, Cu 30% (SEMI conforming)
Note4: The power dissipation decreases the reciprocal of the saturated thermal resistance (1/ Rth(j-a)) for each degree (1°C) that the ambient temperature is exceeded (Ta = 25°C).

Operating Conditions

DC Items (Unless otherwise specified, V_{DD} = 3.0 to 5.5 V, T_a = −40°C to 85°C)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
Supply voltage	V_{DD}	—	3.0	—	5.5	V
High level logic input voltage	V_{IH}	Test terminal are SIN,SCK, $\overline{\text{SLAT}}$, $\overline{\text{OE}}$	0.7 × V_{DD}	—	V_{DD}	V
Low level logic input voltage	V_{IL}	Test terminal are SIN,SCK, $\overline{\text{SLAT}}$, $\overline{\text{OE}}$	GND	—	0.3 × V_{DD}	V
High level SOUT output current	I_{OH}	—	—	—	−1	mA
Low level SOUT output current	I_{OL}	—	—	—	1	mA
Constant current output	I_{OUT}	Test terminal is $\overline{\text{OUTn}}$	1.5	—	90	mA

AC Items (Unless otherwise specified, V_{DD} = 3.0 to 5.5 V, T_a = −40°C to 85°C)

Characteristics	Symbol	Test Circuits	Test Conditions	Min	Typ.	Max	Unit
Serial data transfer frequency	f_{SCK}	6	—	—	—	25	MHz
Serial data Hold time	t_{HOLD1}	6	—	5	—	—	ns
	t_{HOLD2}	6	—	5	—	—	ns
Serial data Setup time	t_{SETUP1}	6	—	5	—	—	ns
	t_{SETUP2}	6	—	5	—	—	ns
Maximum clock rise time	t_r	6	(Note1)	—	—	500	ns
Maximum clock fall time	t_f	6	(Note1)	—	—	500	ns

Note1: If the device is connected in a cascade and the tr/tf of the clock waveform increases due to deceleration of the clock waveform,it may not be possible to achieve the timing required for data transfer. Please keep these timing conditions in mind when designing your application.

Electrical Characteristics (Unless otherwise specified, V_{DD} = 3.3V, T_a = 25°C)

Characteristics	Symbol	Test Circuits	Test Conditions	Min	Typ.	Max	Unit
High level SOUT output voltage	V_{OH}	1	I_{OH} = −1 mA	V_{DD} − 0.4	—	—	V
Low level SOUT output voltage	V_{OL}	1	I_{OL} = +1 mA	—	—	0.4	V
High level logic input current	I_{IH}	2	V_{IN} = V_{DD}, $\overline{OE}$, SIN, SCK	—	—	1	μA
Low level logic input current	I_{IL}	3	V_{IN} = GND, $\overline{SLAT}$, SIN, SCK	—	—	−1	μA
Power supply current	I_{DD}	4	R_{EXT} = 1.2 kΩ, All output on	—	—	8.0	mA
Output current	I_{OUT}	5	V_{DD} = 3.3 V, V_{OUT} = 1.0 V, R_{EXT} = 1.2 kΩ, 1 output on	—	14.4	—	mA
Constant current error(Ch to Ch) (S rank)	$\Delta I_{OUT(Ch)}$	5	V_{DD} = 3.3 V, V_{OUT} = 1.0 V, R_{EXT} = 1.2 kΩ, 1 output on	—	±1	±1.5	%
Constant current error(IC to IC) (S rank)	$\Delta I_{OUT(IC)}$	5	V_{DD} = 3.3 V, V_{OUT} = 1.0 V, R_{EXT} = 1.2 kΩ, 1 output on	—	±1	±1.5	%
Constant current error(Ch to Ch) (N rank)	$\Delta I_{OUT(Ch)}$	5	V_{DD} = 3.3 V, V_{OUT} = 1.0 V, R_{EXT} = 1.2 kΩ, 1 output on	—	±1	±2.5	%
Constant current error(IC to IC) (N rank)	$\Delta I_{OUT(IC)}$	5	V_{DD} = 3.3 V, V_{OUT} = 1.0 V, R_{EXT} = 1.2 kΩ, 1 output on	—	±1	±2.5	%
Output OFF leak current	I_{OK}	5	V_{DD} = 3.3 V, V_{OUT}= 17 V, R_{EXT} = 1.2 kΩ	—	—	0.5	μA
Constant current output power supply voltage regulation	$\%V_{DD}$	5	V_{DD} = 3.0 to 3.6 V, V_{OUT} = 1.0 V, R_{EXT} = 1.2 kΩ, 1 output on	—	±1	±5	%/V
Constant current output output voltage regulation	$\%V_{OUT}$	5	V_{DD} = 3.3 V, V_{OUT} = 1.0 to 3.0 V, R_{EXT} = 1.2 kΩ, 1 output on	—	±0.1	±0.5	%/V
Pull-up resistor	$R_{(Up)}$	3	$\overline{OE}$	400	500	600	kΩ
Pull-down resistor	$R_{(Down)}$	2	$\overline{SLAT}$	400	500	600	kΩ

Electrical Characteristics (Unless otherwise specified, V_{DD} = 5.0V, Ta = 25°C)

Characteristics	Symbol	Test Circuits	Test Conditions	Min	Typ.	Max	Unit
High level SOUT output voltage	V_{OH}	1	I_{OH} = −1 mA	V_{DD} − 0.4	—	—	V
Low level SOUT output voltage	V_{OL}	1	I_{OL} = +1 mA	—	—	0.4	V
High level logic input current	I_{IH}	2	V_{IN} = V_{DD}, $\overline{OE}$, SIN, SCK	—	—	1	μA
Low level logic input current	I_{IL}	3	V_{IN} = GND, $\overline{SLAT}$, SIN, SCK	—	—	−1	μA
Power supply current	I_{DD}	4	R_{EXT} = 1.2 kΩ, All output on	—	—	8.0	mA
Output current	I_{OUT}	5	V_{DD} = 5.0 V, V_{OUT} = 1.0 V, R_{EXT} = 1.2 kΩ, 1 output on	—	14.4	—	mA
Constant current error(Ch to Ch) (S rank)	$\Delta I_{OUT(Ch)}$	5	V_{DD} = 3.3 V, V_{OUT} = 1.0 V, R_{EXT} = 1.2 kΩ, 1 output on	—	±1	±1.5	%
Constant current error(IC to IC) (S rank)	$\Delta I_{OUT(IC)}$	5	V_{DD} = 3.3 V, V_{OUT} = 1.0 V, R_{EXT} = 1.2 kΩ, 1 output on	—	±1	±1.5	%
Constant current error(Ch to Ch) (N rank)	$\Delta I_{OUT(Ch)}$	5	V_{DD} = 5.0 V, V_{OUT} = 1.0 V, R_{EXT} = 1.2 kΩ, 1 output on	—	±1	±2.5	%
Constant current error(IC to IC) (N rank)	$\Delta I_{OUT(IC)}$	5	V_{DD} = 5.0 V, V_{OUT} = 1.0 V, R_{EXT} = 1.2 kΩ, 1 output on	—	±1	±2.5	%
Output OFF leak current	I_{OK}	5	V_{DD} = 5.0 V, V_{OUT} = 17 V, R_{EXT} = 1.2 kΩ	—	—	0.5	μA
Constant current output power supply voltage regulation	$\%V_{DD}$	5	V_{DD} = 4.5 to 5.5 V, V_{OUT} = 1.0 V, R_{EXT} = 1.2 kΩ, 1 output on	—	±1	±5	%/V
Constant current output output voltage regulation	$\%V_{OUT}$	5	V_{DD} = 5.0 V, V_{OUT} = 1.0 to 3.0 V, R_{EXT} = 1.2 kΩ, 1 output on	—	±0.1	±0.5	%/V
Pull-up resistor	$R_{(Up)}$	3	$\overline{OE}$	400	500	600	kΩ
Pull-down resistor	$R_{(Down)}$	2	$\overline{SLAT}$	400	500	600	kΩ

Switching Characteristics (Unless otherwise specified, V_{DD} = 3.3V, T_a = 25°C)

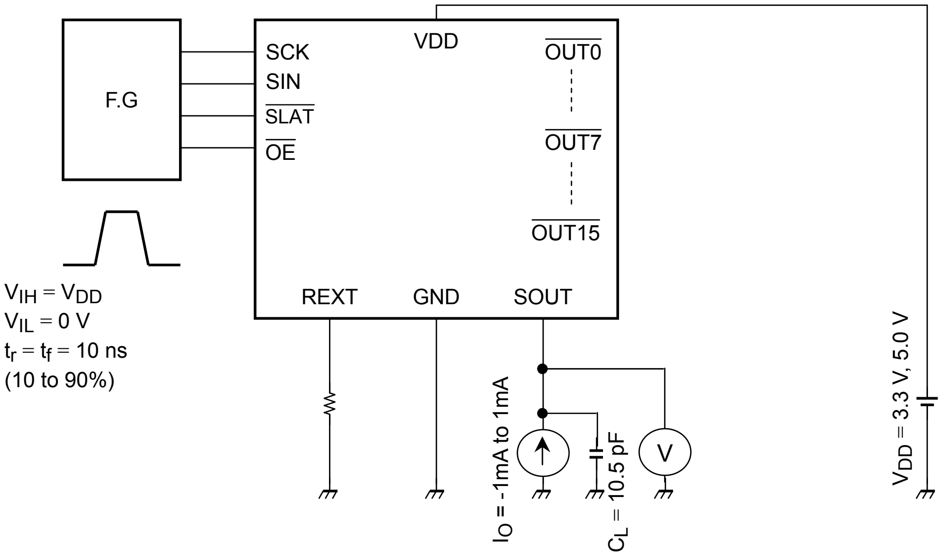
Characteristics		Symbol	Test Circuits	Test Conditions	Min	Typ.	Max	Unit
Propagation delay time	SCK-$\overline{OUT0}$	t_{pLH1}	6	$\overline{SLAT}$ = "H", $\overline{OE}$ = "L"	—	50	65	ns
	$\overline{SLAT}$ - $\overline{OUT0}$	t_{pLH2}	6	$\overline{OE}$ = "L"	—	50	65	ns
	$\overline{OE}$ - $\overline{OUT0}$	t_{pLH3}	6	$\overline{SLAT}$ = "H"	—	50	65	ns
	SCK-SOUT	t_{pLH}	6	C_L=10.5 pF	10	20	35	ns
	SCK-$\overline{OUT0}$	t_{pHL1}	6	$\overline{SLAT}$ = "H", $\overline{OE}$ = "L"	—	30	40	ns
	$\overline{SLAT}$ - $\overline{OUT0}$	t_{pHL2}	6	$\overline{OE}$ = "L"	—	30	40	ns
	$\overline{OE}$ - $\overline{OUT0}$	t_{pHL3}	6	$\overline{SLAT}$ = "H"	—	30	40	ns
	SCK-SOUT	t_{pHL}	6	C_L=10.5 pF	10	20	35	ns
Output rise time		t_{or}	6	10 to 90% of voltage waveform	—	10	20	ns
Output fall time		t_{of}	6	90 to 10% of voltage waveform	—	10	20	ns
Enable pulse width		t_{wOE}	6	$\overline{OE}$ = "H" or "L"	25	—	—	ns
Clock pulse width		t_{wSCK}	6	SCK = "H" or "L"	20	—	—	ns
Latch pulse width		t_{wSLAT}	6	$\overline{SLAT}$ = "H"	20	—	—	ns

Switching Characteristics (Unless otherwise specified, V_{DD} = 5.0V, T_a = 25°C)

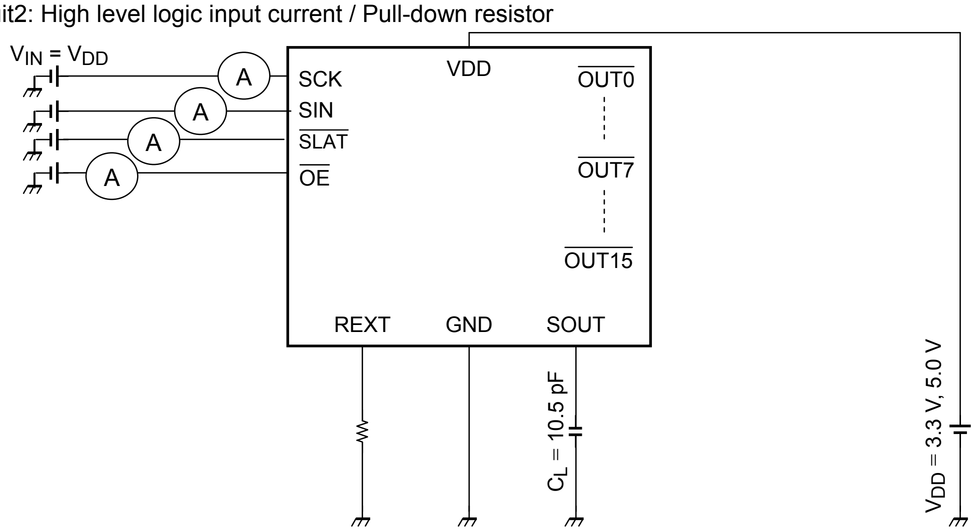
Characteristics		Symbol	Test Circuits	Test Conditions	Min	Typ.	Max	Unit
Propagation delay time	SCK-$\overline{OUT0}$	t_{pLH1}	6	$\overline{SLAT}$ = "H", $\overline{OE}$ = "L"	—	50	65	ns
	$\overline{SLAT}$ - $\overline{OUT0}$	t_{pLH2}	6	$\overline{OE}$ = "L"	—	50	65	ns
	$\overline{OE}$ - $\overline{OUT0}$	t_{pLH3}	6	$\overline{SLAT}$ = "H"	—	50	65	ns
	SCK-SOUT	t_{pLH}	6	C_L=10.5 pF	10	20	35	ns
	SCK-$\overline{OUT0}$	t_{pHL1}	6	$\overline{SLAT}$ = "H", $\overline{OE}$ = "L"	—	30	40	ns
	$\overline{SLAT}$ - $\overline{OUT0}$	t_{pHL2}	6	$\overline{OE}$ = "L"	—	30	40	ns
	$\overline{OE}$ - $\overline{OUT0}$	t_{pHL3}	6	$\overline{SLAT}$ = "H"	—	30	40	ns
	SCK-SOUT	t_{pHL}	6	C_L=10.5 pF	10	20	35	ns
Output rise time		t_{or}	6	10 to 90% of voltage waveform	—	10	20	ns
Output fall time		t_{of}	6	90 to 10% of voltage waveform	—	10	20	ns
Enable pulse width		t_{wOE}	6	$\overline{OE}$ = "H" or "L"	25	—	—	ns
Clock pulse width		t_{wSCK}	6	SCK = "H" or "L"	20	—	—	ns
Latch pulse width		t_{wSLAT}	6	$\overline{SLAT}$ = "H"	20	—	—	ns

Test Circuits

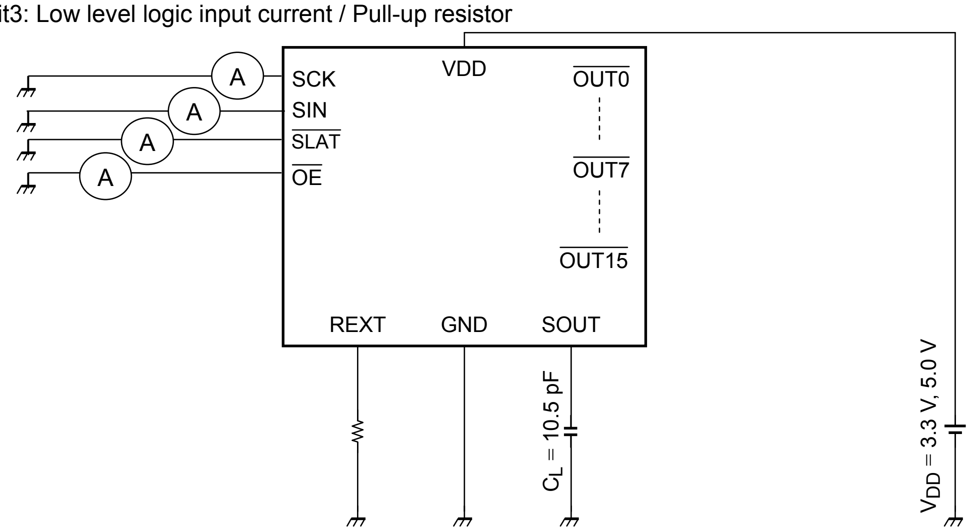
Test Circuit1: High level SOUT output voltage / Low level SOUT output voltage



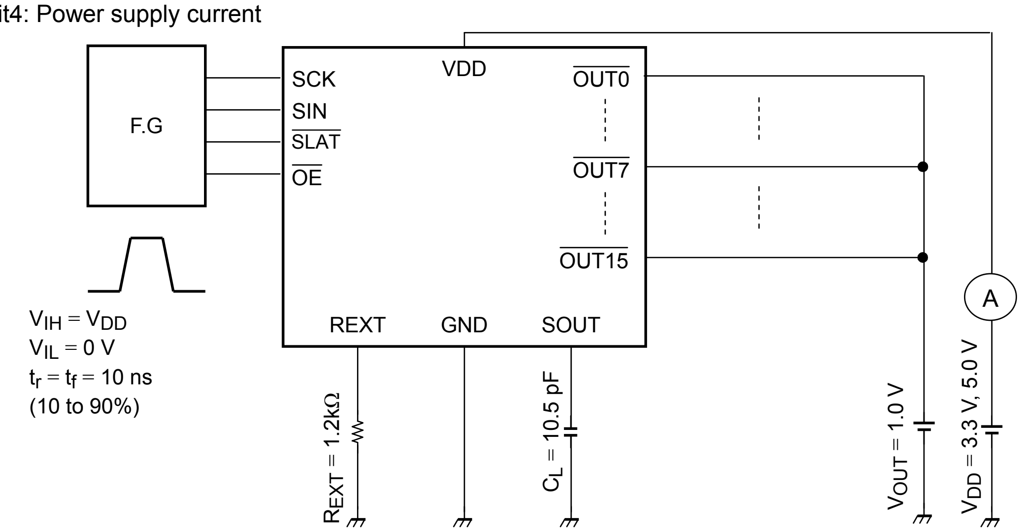
Test Circuit2: High level logic input current / Pull-down resistor



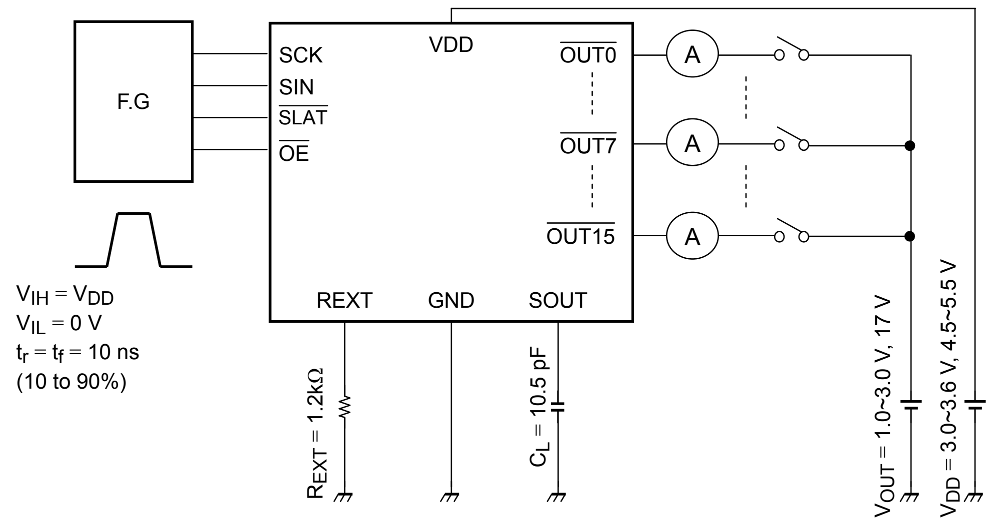
Test Circuit3: Low level logic input current / Pull-up resistor



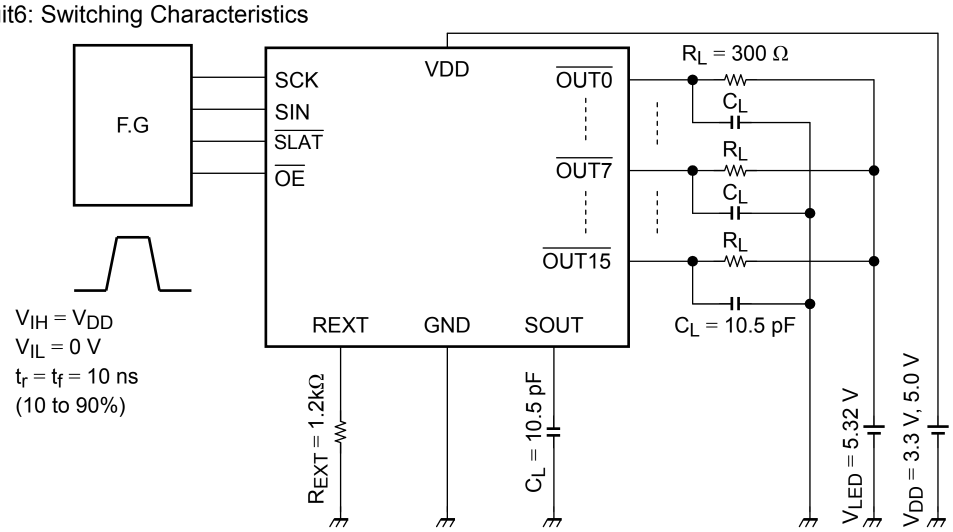
Test Circuit4: Power supply current



Test Circuit5: Constant current output / Output OFF leak current / Constant current error
Constant current output power supply voltage regulation
Constant current output output voltage regulation

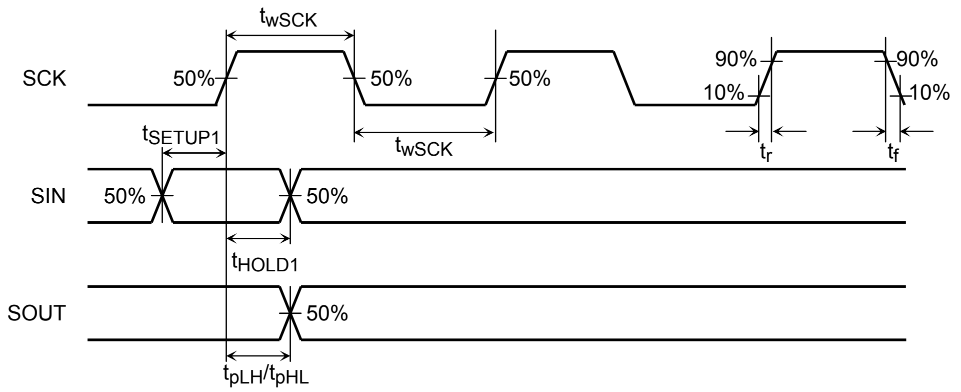


Test Circuit6: Switching Characteristics

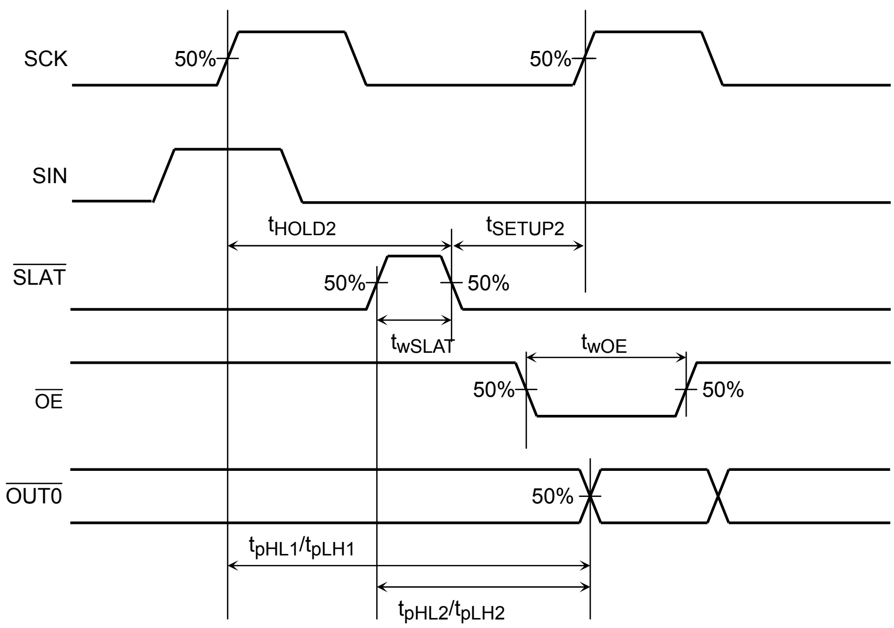


Timing Waveforms

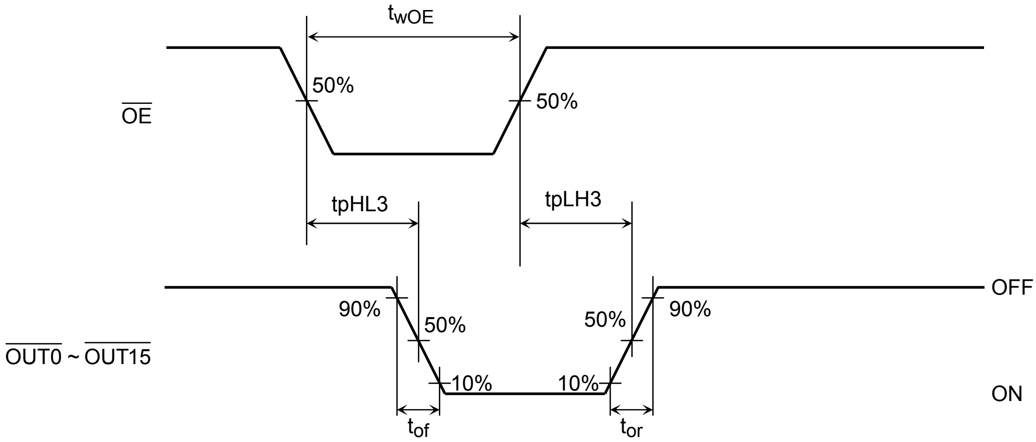
1. SCK, SIN, SOUT



2. SCK, SIN, $\overline{\text{SLAT}}$, $\overline{\text{OE}}$, $\overline{\text{OUT0}}$



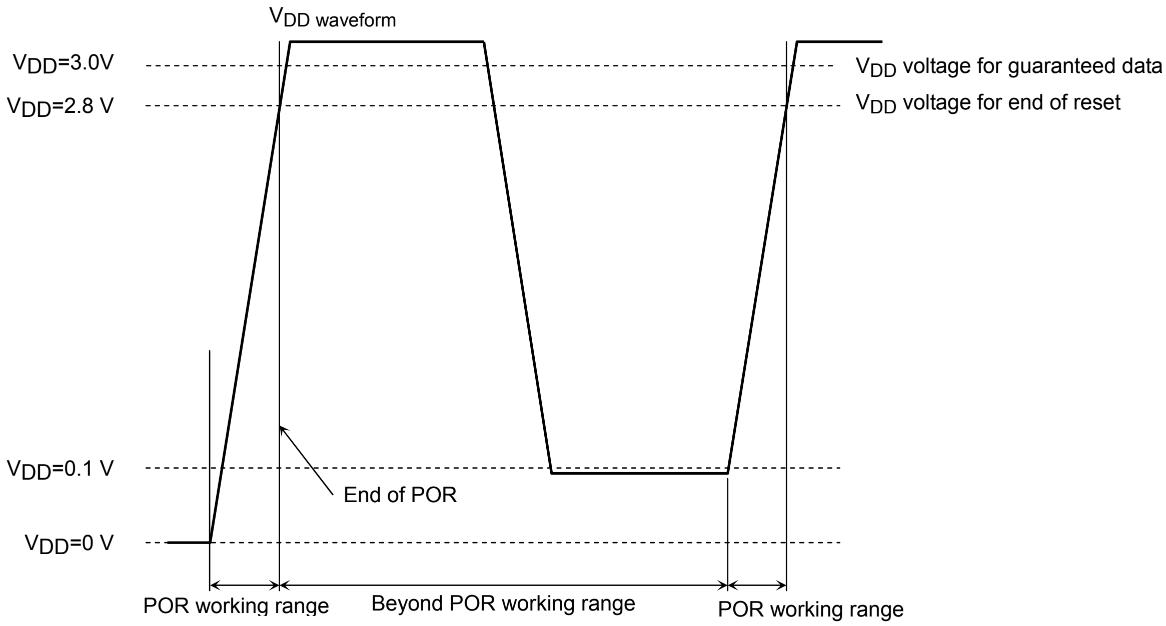
3. $\overline{\text{OE}}$, $\overline{\text{OUT0}}$ ~ $\overline{\text{OUT15}}$



Power on reset (POR)

The TC62D749CFG provides a power-on reset to reset all internal data in order to prevent malfunctions.

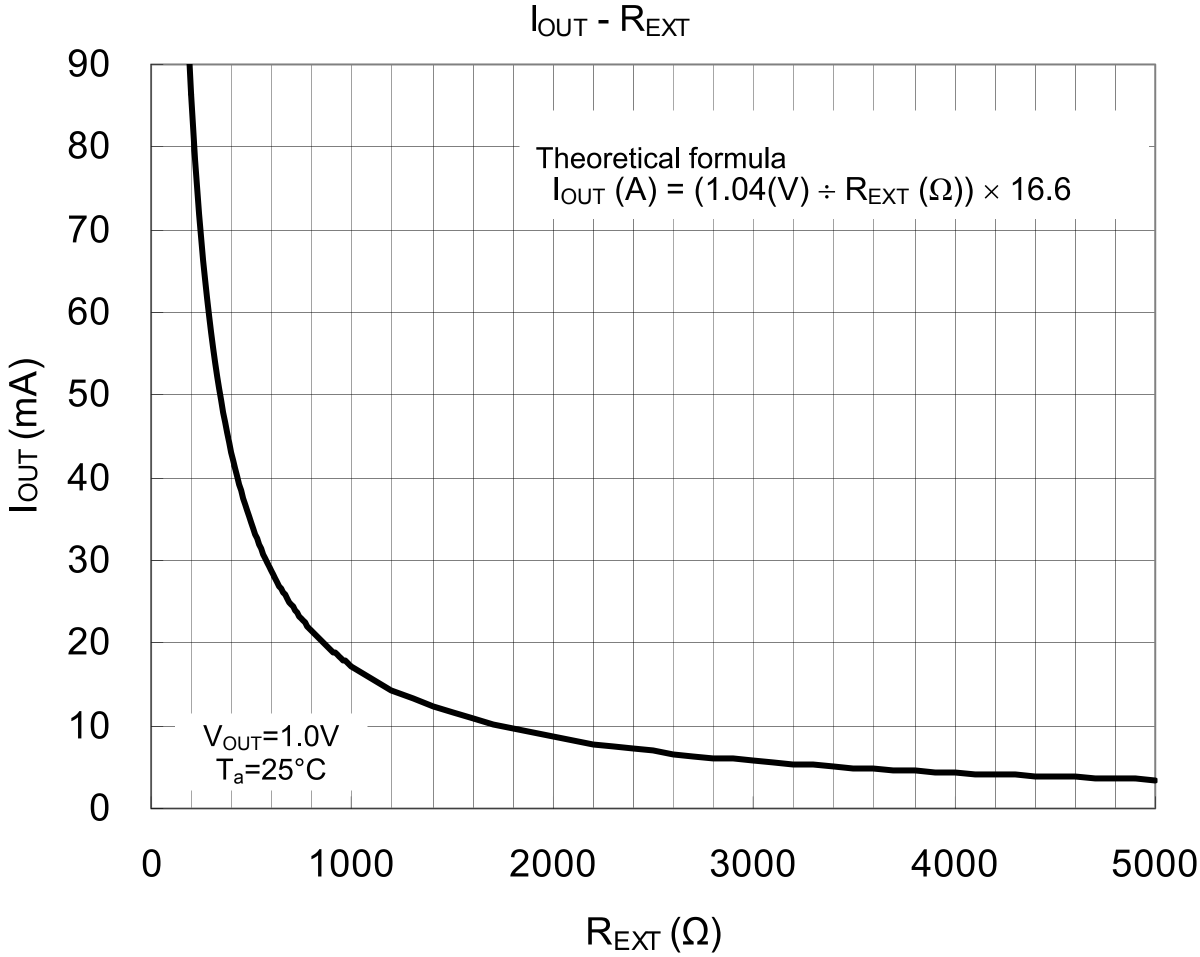
The POR circuitry works properly only when V_{DD} rises from 0 V. To re-activate the POR circuitry, V_{DD} must be brought to less than 0.1 V. Internal data is guaranteed to be retained after V_{DD} exceeds 3.0 V.



Reference data

The above data is for reference only, not guaranteed. Careful evaluation is required prior to creating a production design.

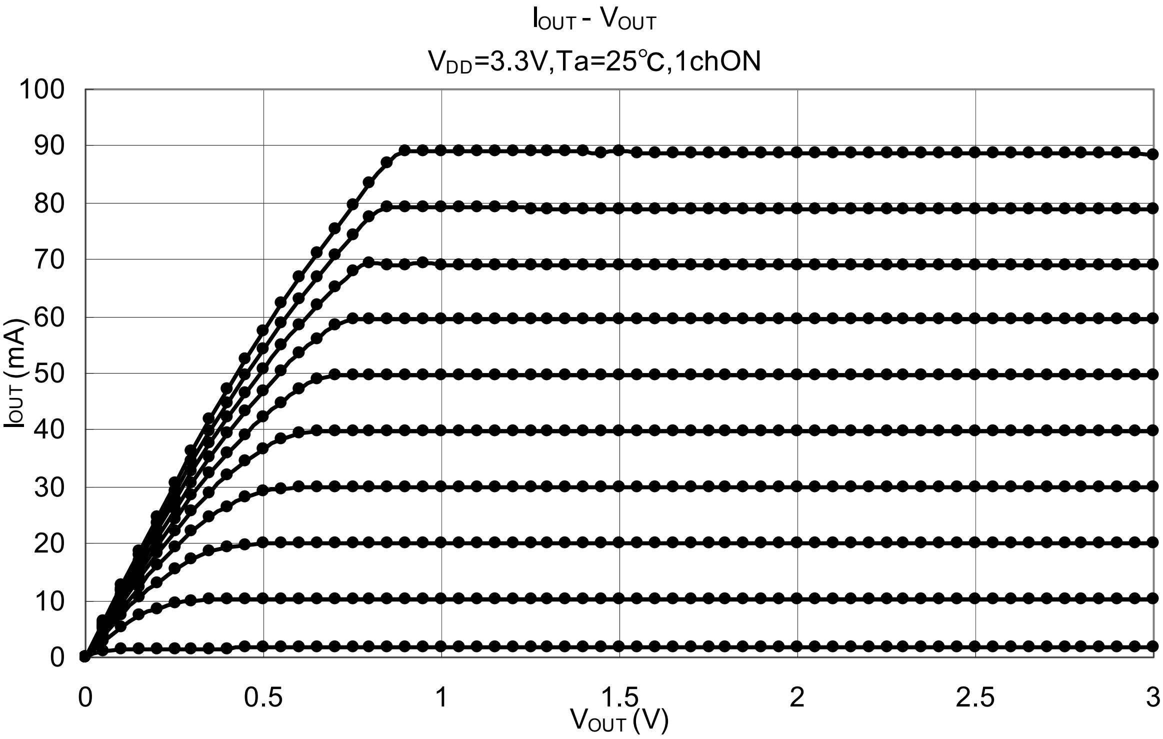
Output Current (I_{OUT}) – Output current setting resistance (R_{EXT})

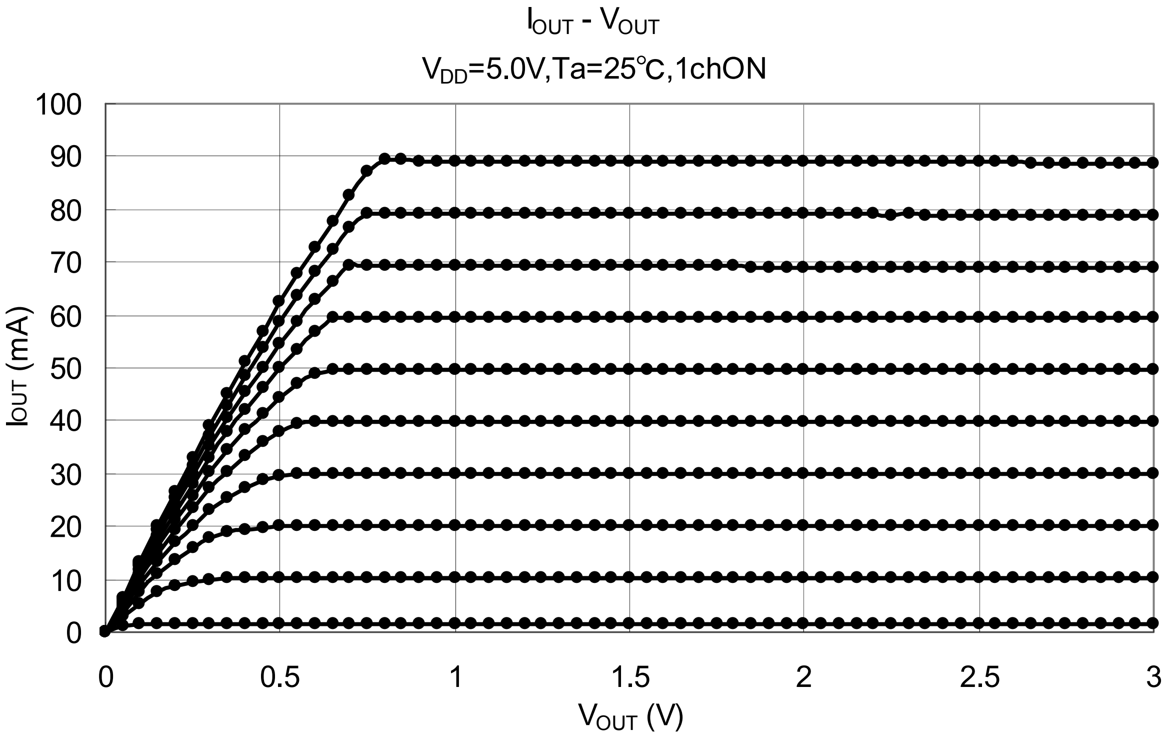


Reference data

The above data is for reference only, not guaranteed. Careful evaluation is required prior to creating a production design.

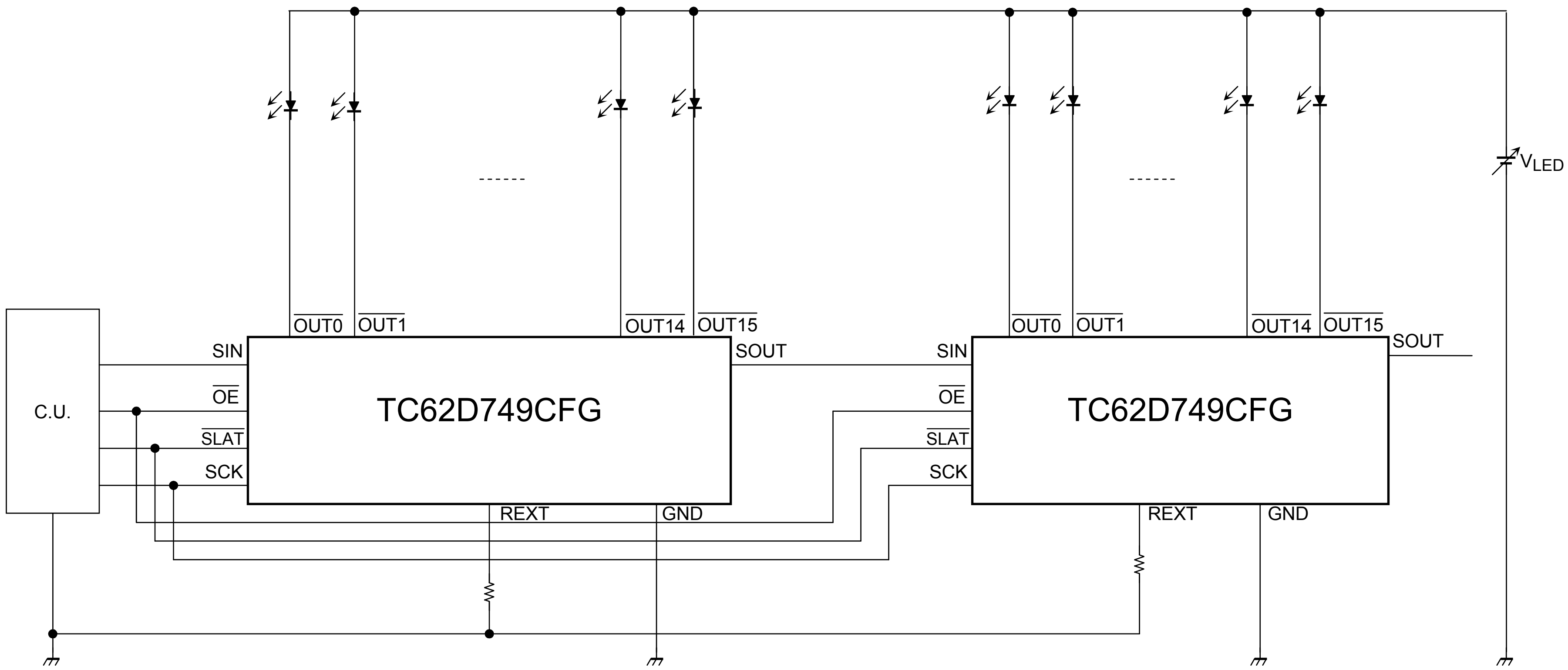
Output current (I_{OUT}) – Output voltage (V_{OUT})





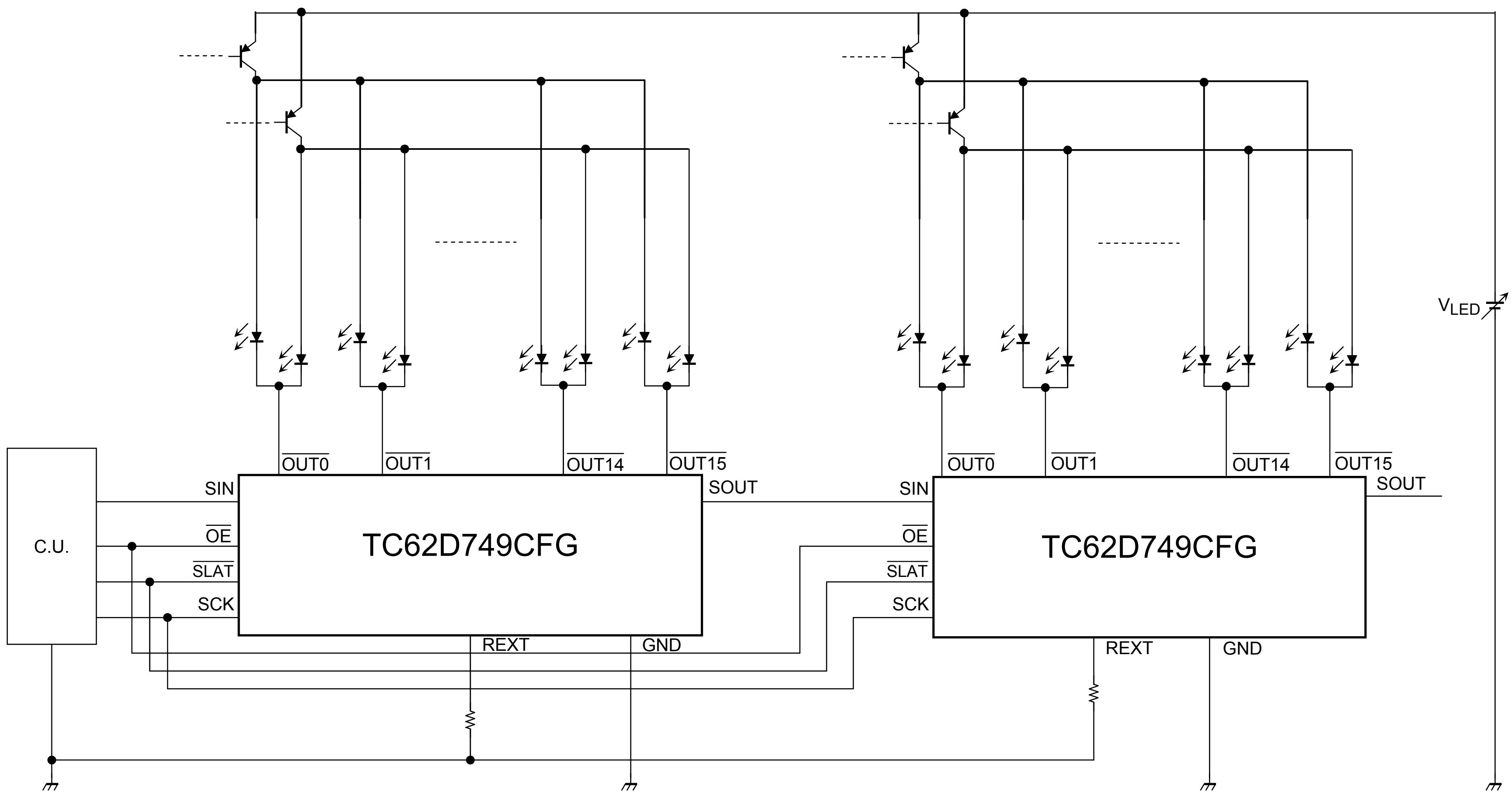
Application Circuit: General Composition for Static Lighting of LEDs

In the following diagram, it is recommended that the LED supply voltage (V_{LED}) be equal to or greater than the sum of V_f (max) of all LEDs plus 1.0 V.



Application Circuit: General Composition for Dynamic Lighting of LEDs

In the following diagram, it is recommended that the LED supply voltage (V_{LED}) be equal to or greater than the sum of V_f (max) of all LEDs plus 1.0 V.



Notes on design of ICs

1. Decoupling capacitors between power supply and GND
   It is recommended to place decoupling capacitors between power supply and GND as close to the IC as possible.

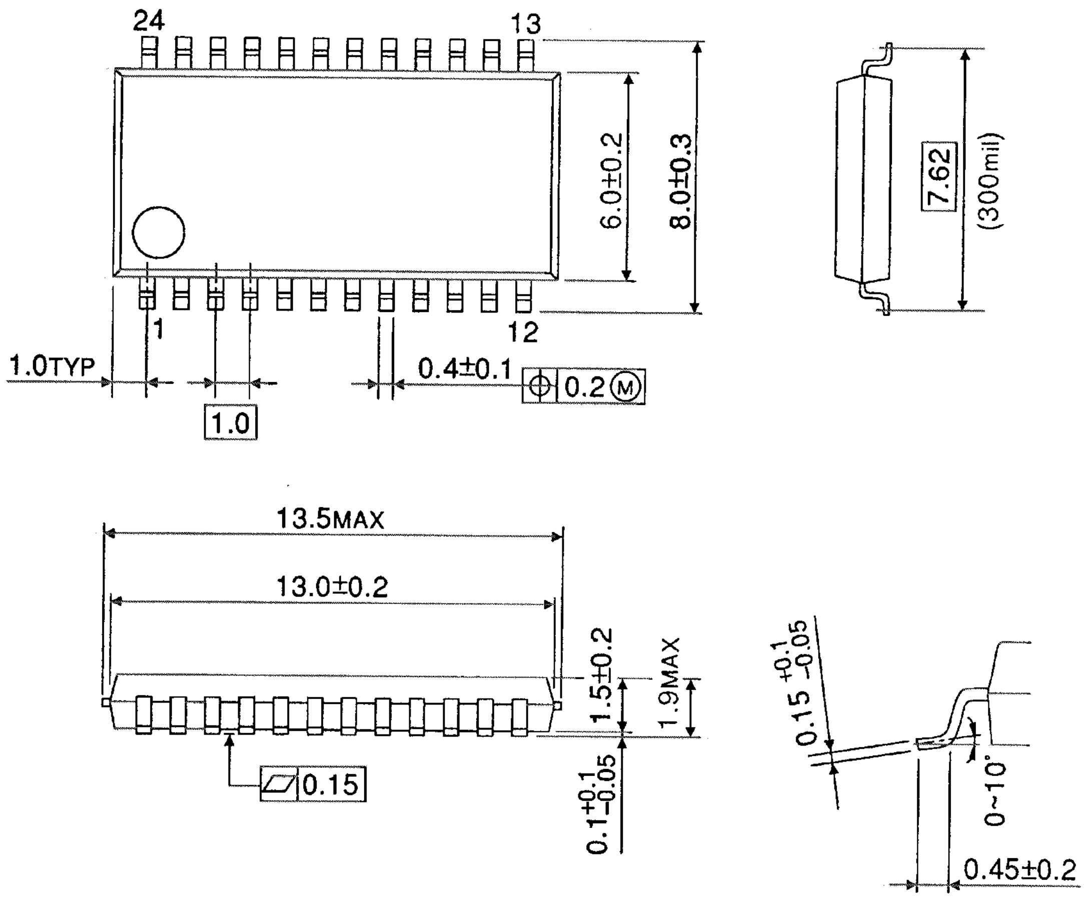
2. Output current setting resistors
   When the output current setting resistors (R_{EXT}) are shared among multiple ICs, production design should be evaluated carefully.

3. Board layout
   Ground noise generated by output switching might cause the IC to malfunction if the ground line exhibits inductance and resistance due to PC board traces and wire leads. Also, the inductance between the IC output pins and the LED cathode pins might cause large surge voltage, damaging LEDs and the IC outputs. To avoid this situation, PC board traces and wire leads should be carefully laid out.

4. Consult the latest technical information for mass production.

Package Dimensions

SSOP24-P-300-1.00B Unit : mm



Weight: 0.29 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

[5] Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

(1) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_J) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(2) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

About solderability, following conditions were confirmed

Solderability

(1) Use of Sn-37Pb solder Bath

- **solder bath temperature: 230°C**
- **dipping time: 5 seconds**
- **the number of times: once**
- **use of R-type flux**

(2) Use of Sn-3.0Ag-0.5Cu solder Bath

- **solder bath temperature: 245°C**
- **dipping time: 5 seconds**
- **the number of times: once**
- **use of R-type flux**

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