Product Specification

PE42556 Flip Chip

UltraCMOS® SPDT RF Switch
9 kHz - 13500 MHz

Features

- HaRP™ technology enhanced
  - Eliminates gate lag
  - No insertion loss or phase drift
  - Fast settling time
- Next Gen 0.25 µm process technology
- Single-pin 3.3V CMOS logic control
- High isolation: 26 dB@ 13.5 GHz
- Low insertion loss: 1.7 dB @ 13.5 GHz
- P1dB: 33 dBm typical
- Return loss: 13 dB @ 13.5 GHz (typ)
- IIP3: +56 dBm typical
- High ESD: 4kV HBM
- Absorptive switch design
- Flip Chip packaging

Product Description

The PE42556 RF switch is designed for use in Test/ATE, cellular and other wireless applications. This broadband general purpose switch maintains excellent RF performance and linearity from 9 kHz through 13500 MHz. The PE42556 integrates on-board CMOS control logic driven by a single-pin, low voltage CMOS control input. It also has a logic select pin which enables changing the logic definition of the control pin. Additional features include a novel user defined logic table, enabled by the on-board CMOS circuitry. The PE42556 also exhibits excellent isolation of 26 dB at 13500 MHz, fast settling time, and is offered in a tiny Flip Chip package.

The PE42556 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

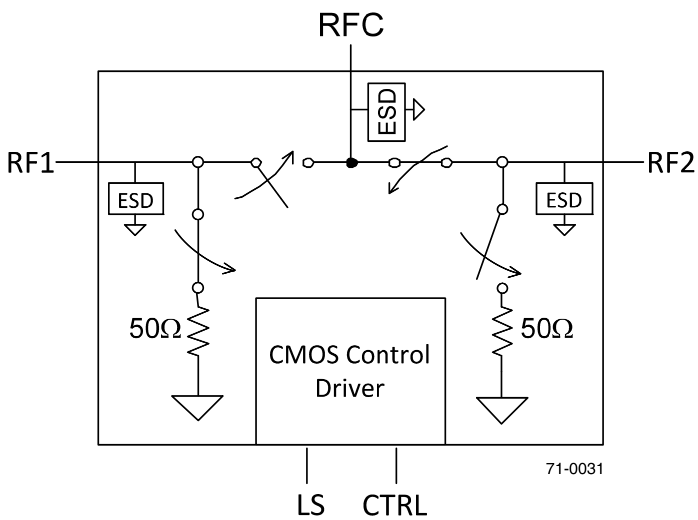


Figure 2. Die Photo (Bumps Up)

Flip Chip Packaging

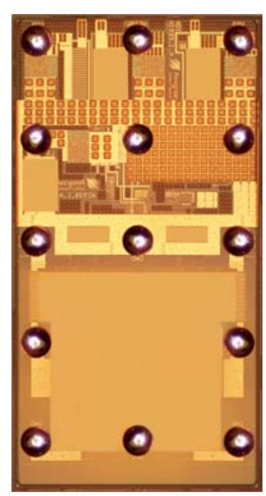


Table 1. Electrical Specifications: Temp = 25°C, V_{DD} = 3.3V

Parameter	Conditions	Min	Typical	Max	Units
Operation Frequency		9 kHz		13500 MHz	As shown
Insertion Loss	9 kHz - 10 MHz 10 - 3000 MHz 3000 - 7500 MHz 7500 - 10000 MHz 10000 - 13500 MHz		0.85 0.92 0.98 1.07 1.74	0.93 1.06 1.23 1.41 2.65	dB dB dB dB dB
Isolation – RF1 to RF2	9 kHz - 10 MHz 10 - 3000 MHz 3000 - 7500 MHz 7500 - 10000 MHz 10000 - 13500 MHz	76.5 43.5 30.0 24.0 15.5	88.5 46.0 31.5 25.5 17.5		dB dB dB dB dB
Isolation – RFC to RF1	9 kHz - 10 MHz 10 - 3000 MHz 3000 - 7500 MHz 7500 - 10000 MHz 10000 - 13500 MHz	72.5 39.0 31.5 27.0 21.5	84.0 40.5 33.0 30.5 26.5		dB dB dB dB dB
Isolation – RFC to RF2	9 kHz - 10 MHz 10 - 3000 MHz 3000 - 7500 MHz 7500 - 10000 MHz 10000 - 13500 MHz	75.5 39.5 31.5 27.5 21.0	87.0 41.0 33.0 30.5 26.0		dB dB dB dB dB
Return Loss	9 kHz - 10 MHz 10 - 3000 MHz 3000 - 7500 MHz 7500 - 10000 MHz 10000 - 13500 MHz		22.5 22.0 17.0 16.0 13.0		dB dB dB dB dB
Settling Time	50% CTRL to 0.05 dB final value (-40 to +85 °C) Rising Edge 50% CTRL to 0.05 dB final value (-40 to +85 °C) Falling Edge		8.5 9.5	10.0 13.5	µs µs
Switching Time	50% CTRL to 90% or 10% of final value (-40 to +85 °C)		3.3	4.0	µs
Input 1 dB Compression [1,2]	13500 MHz		33		dBm
Input IP3 [1]	13500 MHz		56		dBm
Input IP2 [1]	13500 MHz		107.5		dBm

Notes: 1. Linearity and power performance are derated at lower frequencies (< 1 MHz)
2. Please refer to Maximum Operating Pin (50Ω) in *Table 3*

Figure 3. Bump Configuration (Bumps Up)

Flip Chip Packaging

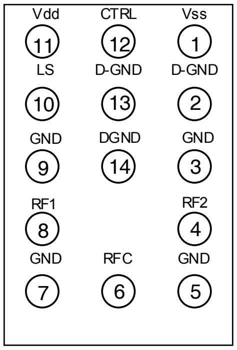


Table 2. Bump Descriptions

Bump No.	Bump Name	Description
1	V_{SS}	Negative supply voltage or GND connection (Note 3)
2, 13, 14	D-GND	Digital Ground
3, 5, 7, 9	GND	Ground
4	RF2	RF Port 2
6	RFC	RF Common
8	RF1	RF Port 1
10	LS	Logic Select - Used to determine the definition for the CTRL pin (see *Table 5*)
11	V_{DD}	Nominal 3.3V supply connection
12	CTRL	CMOS logic level

Note: 3. Use VSS (bump 1, VSS = -VDD) to bypass and disable internal negative voltage generator. Connect VSS (bump 1) to GND (VSS = 0V) to enable internal negative voltage generator.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Units
V_{DD} Positive Power Supply Voltage	3.0	3.3	3.6	V
V_{DD} Negative Power Supply Voltage	-3.6	-3.3	-3.0	V
I_{DD} Power Supply Current (V_{ss} = -3.3V, V_{DD} = 3.0 to 3.6V, -40 to +85 °C)		8.0	12.5	µA
I_{DD} Power Supply Current (V_{ss} = 0V, V_{DD} = 3.0 to 3.6V, -40 to +85 °C)		21.5	29.0	µA
I_{SS} Negative Power Supply Current (V_{ss} = -3.3V, V_{DD} = 3.0 to 3.6V, -40 to +85 °C)		-18.0	-24.0	µA
Control Voltage High	0.7xV_{DD}			V
Control Voltage Low			0.3xV_{DD}	V
P_{IN} RF Power In[4] (50Ω): 9 kHz ≤ 1 MHz 1 MHz ≤ 13.5 GHz			 *Fig. 4,5* 30	 dBm dBm

Note: 4. Please consult Figures 4 and 5 (low-frequency graphs) for recommended low-frequency operating power level.

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input except for CTRL and LS inputs	-0.3	V_{DD}+ 0.3	V
V_{CTRL}	Voltage on CTRL input		4.0	V
V_{LS}	Voltage on LS input		4.0	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
P_{IN}[5] (50Ω)	9 kHz ≤ 1 MHz 1 MHz ≤ 13.5 GHz		*Fig. 4,5* 30	dBm dBm
V_{ESD}	ESD voltage (HBM)[6] ESD voltage (Machine Model)		4000 300	V V

Notes: 5. Please consult *Figures 4* and *5* (low-frequency graphs) for recommended low-frequency operating power level.
6. Human Body Model (HBM, MIL_STD 883 Method 3015.7)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Table 5. Control Logic Truth Table

LS	CTRL	RFC-RF1	RFC-RF2
0	0	off	on
0	1	on	off
1	0	on	off
1	1	off	on

Logic Select (LS)

The Logic Select feature is used to determine the definition for the CTRL pin.

Spurious Performance

The typical spurious performance of the PE42556 is -116 dBm when VSS = 0V (bump 1 = GND). If further improvement is desired, the internal negative voltage generator can be disabled by setting VSS = -VDD.

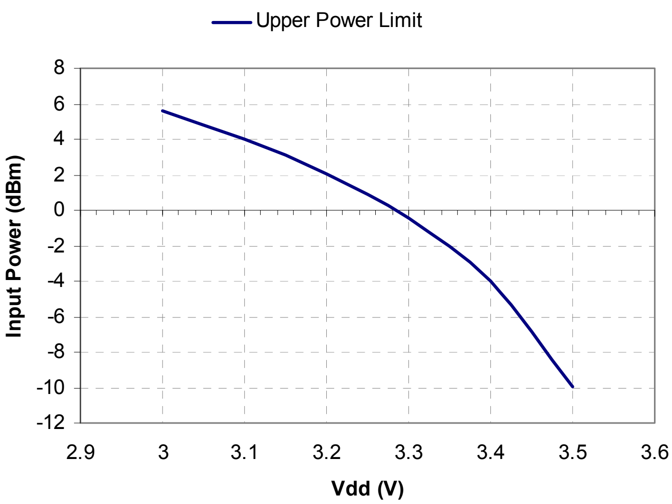
Switching Frequency

The PE42556 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (bump1 = GND). The rate at which the PE42556 can be switched is only limited to the switching time (*Table 1*) if an external negative supply is provided (bump1 = VSS).

Low Frequency Power Handling: $Z_L = 50\Omega$

Figure 4 provides guidelines of how to adjust the Vdd and Input Power to the PE42556 device. The upper limit curve represents the maximum Input Power vs Vdd recommended for this part at low frequencies only. Please consult *Table 3* for the 1 MHz ≤ 13.5 GHz range.

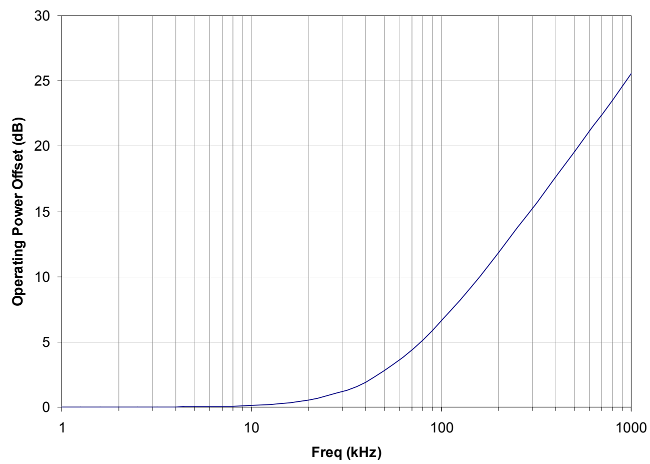
Figure 4. Maximum Operating Power Limit vs. Vdd and Input Power @ 9 kHz



To allow for sustained operation under any load VSWR condition, max power should be kept 6dB lower than max power in 50 Ohm.

Figure 5 shows how the power limit in *Figure 4* will increase with frequency. As the frequency increases, the contours and Maximum Power Limit Curve will increase with the increase in power handling shown on the curve.

Figure 5. Operating Power Offset vs. Frequency (Normalized to 9 kHz)



Power Handling Examples

Example 1: Maximum power handling at 100 kHz, Z = 50 ohms, VSWR 1:1, and Vdd = 3V

- The power handling offset for 100 kHz from *Fig. 5* is 7 dB
- The max power handling at Vdd = 3V is 5.5 dB from *Fig. 4*
- Derate power under mismatch conditions
- Total maximum power handling for this example is 7 dB + 5.5 dB = 12.5 dBm

Evaluation Kit

The SPDT switch EK Board was designed to ease customer evaluation of Peregrine's PE42556 (dual use with PE42554). The RF Common port is connected through a 50 ohm transmission line via the top SMA connector, J1. RF1 and RF2 are connected through 50 ohm transmission lines via SMA connectors J3, and J2, respectively. A through 50 ohm transmission line is available via SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a four metal layers with a total thickness of 62 mils. The top and bottom layers are ROGERS RO4003 material with an 8 mil core and Er = 3.55. The middle layers provide ground for the transmission lines. The RF transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 15 mils, and trace gaps of 10 mils.

Figure 6. Evaluation Board Layouts
Peregrine Specification 101/0402

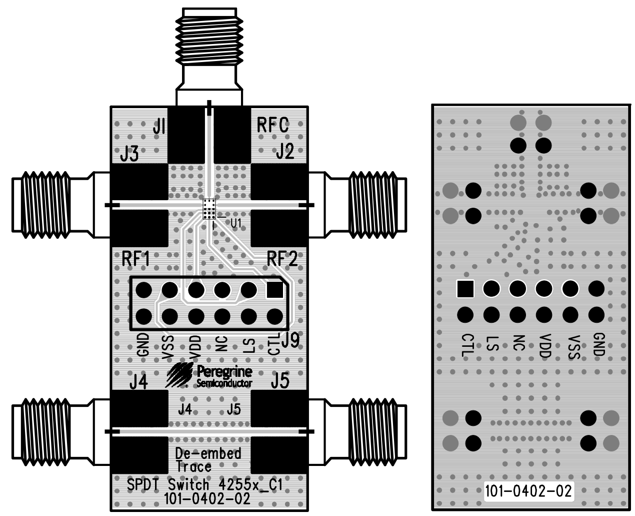
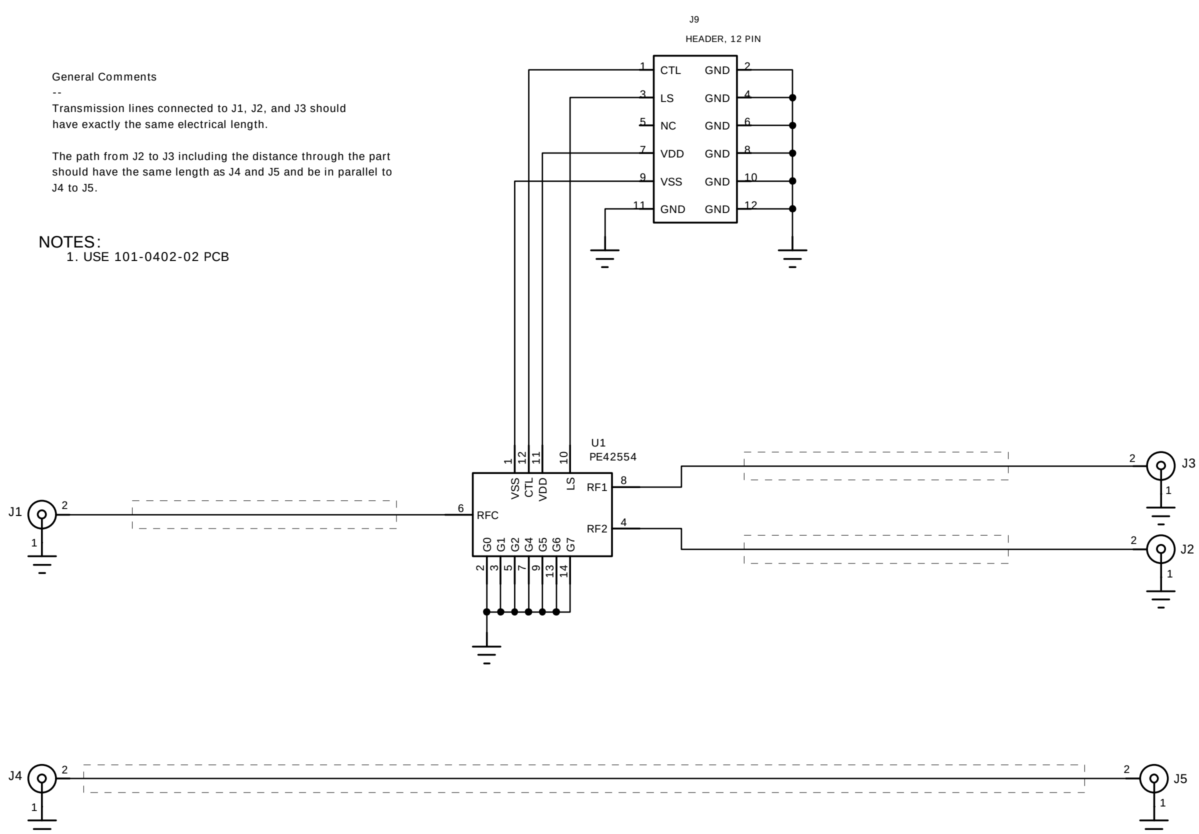


Figure 7. Evaluation Board Schematic
Peregrine Specification 102/0478



Performance Plots: Temperature = 25°C, V_{DD} = 3.3V unless otherwise indicated

Figure 8. Nominal Insertion Loss: RF1, RF2

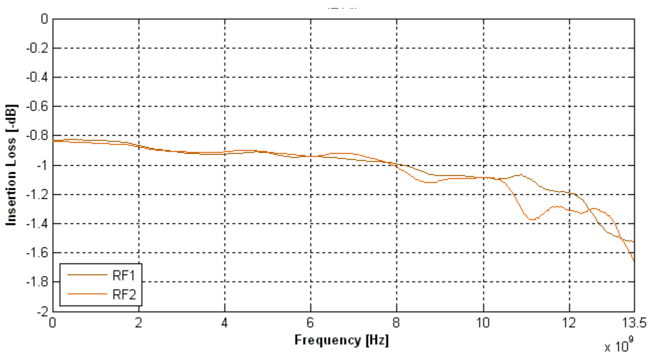


Figure 9. Insertion Loss: RFX @ 3.3V

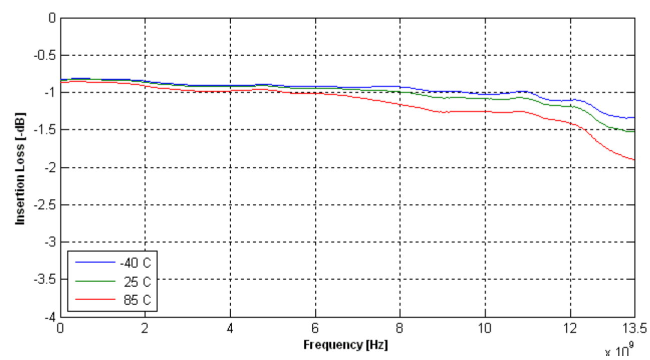


Figure 10. Insertion Loss: RFX @ 25°C

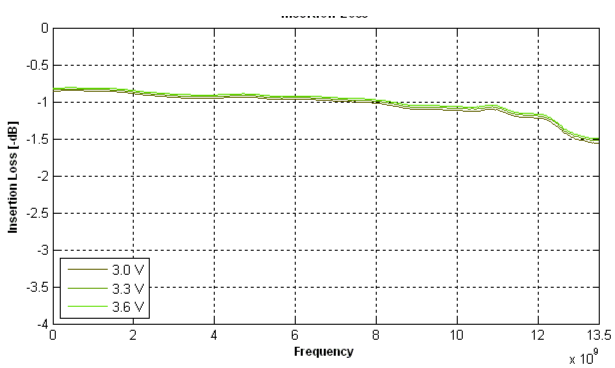


Figure 11. Isolation: Active Port to Isolated Port @ 3.3V

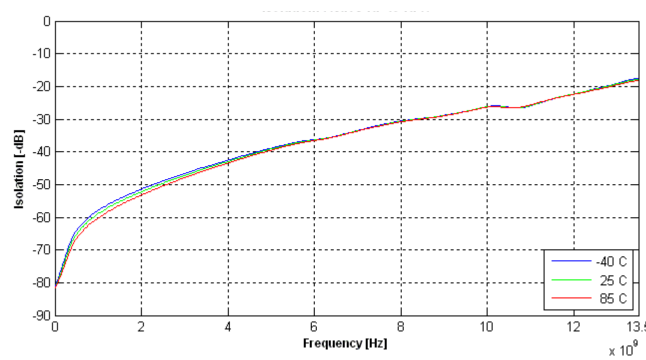


Figure 12. Isolation: Active Port to Isolated Port @ 25°C

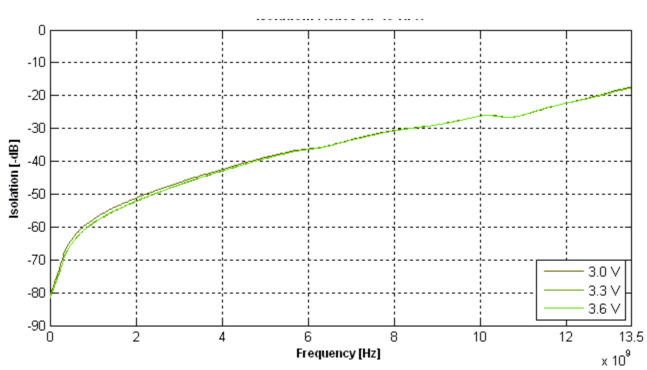
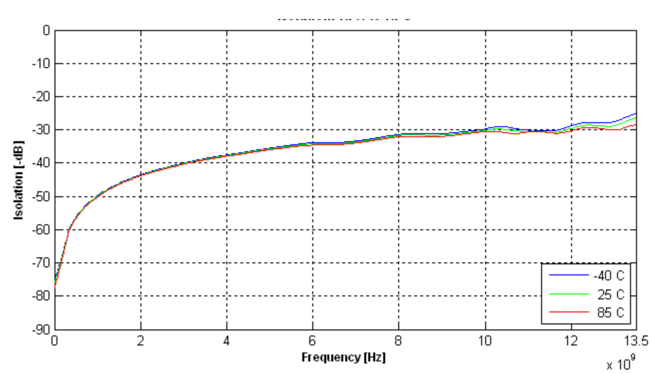


Figure 13. Isolation: RFC to Isolated Port @ 3.3V



Performance Plots: Temperature = 25 °C, V_{DD} = 3.3 V unless otherwise indicated

Figure 14. Isolation: RFC to Isolated Port @ 25°C

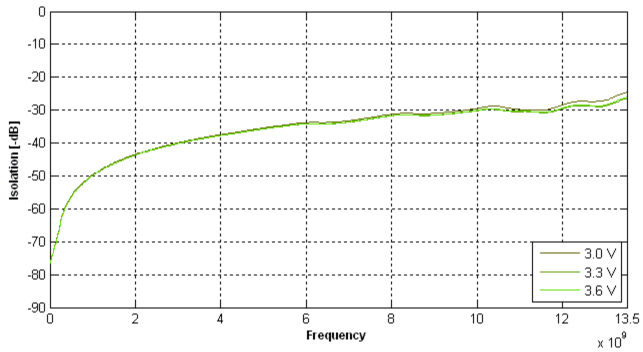


Figure 15. Return Loss at Active Port @ 3.3V

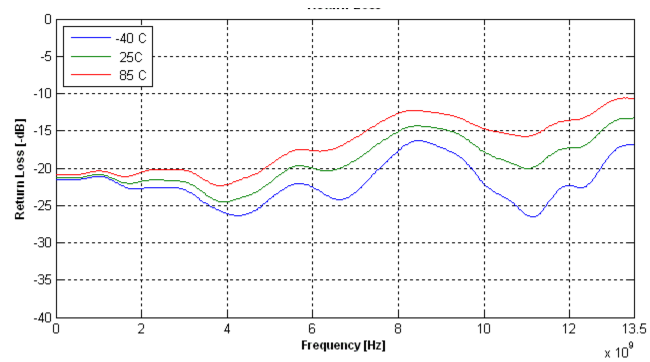


Figure 16. Return Loss at Active Port @ 25°C

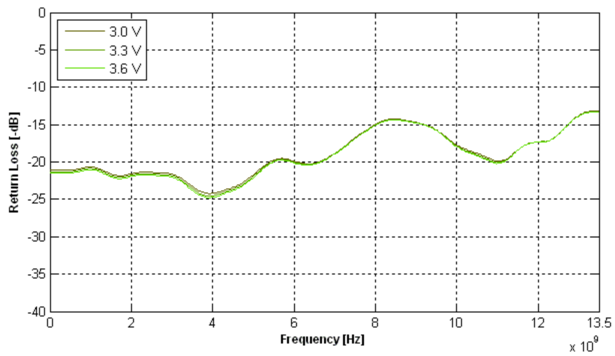


Figure 17. IIP3: Third Order Distortion from 9 kHz - 14 GHz

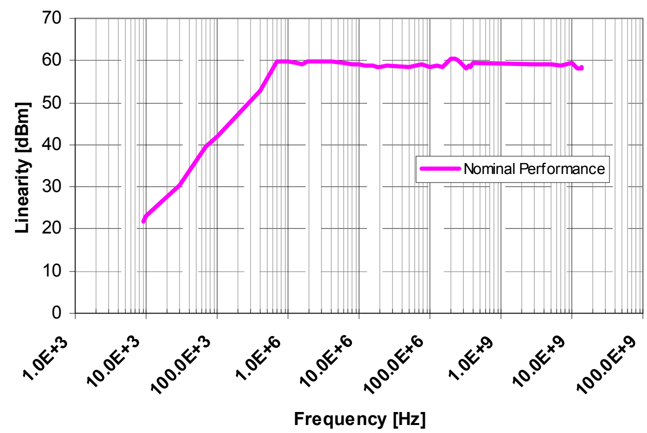


Table 6. Mechanical Specifications

Parameter	Minimum	Typical	Maximum	Units	Test Conditions
Die Size, Drawn (x,y)		996 x 1896		µm	As drawn
Die Size, Singulated (x,y)	1080 x 1980	1100 x 2000	1150 x 2050	µm	Including excess sapphire, max. tolerance = -20/+50 µm
Wafer Thickness	180	200	220	µm	
Wafer Size		150		mm	
Ball Pitch		400		µm	
Ball Height	72.25	85	97.75	µm	
Ball Diameter		110		µm	Typical
UBM Diameter	85	90	95	µm	

RoHS compliant lead-free solder balls

- Solder ball composition: 95.5%Sn/3.5%Ag/ 1.0%Cu

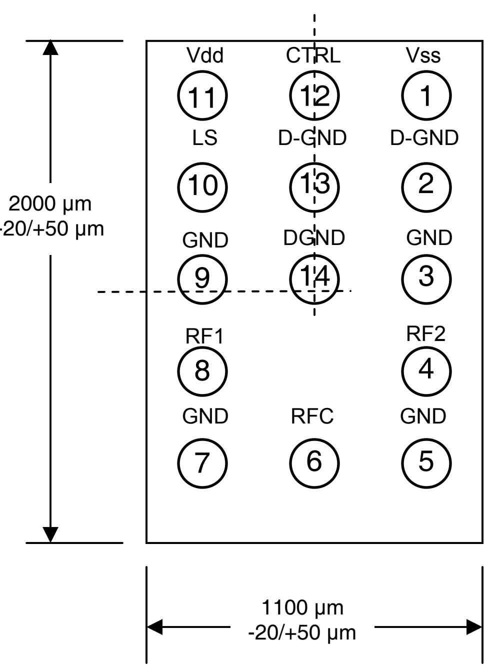
Table 7. Bump Coordinates

Bump #	Bump Name	Bump Center (µm) X	Bump Center (µm) Y
1	VSS	400	850
2	DGND	400	450
3	GND4	400	50
4	RF2	400	-350
5	GND3	400	-750
6	RFC	0	-750
7	GND1	-400	-750
8	RF1	-400	-350
9	GND2	-400	50
10	LS	-400	450
11	VDD	-400	850
12	CTRL	0	850
13	DGND	0	450
14	DGND	0	50

All bump locations originate from the die center and refer to the center of the bump.

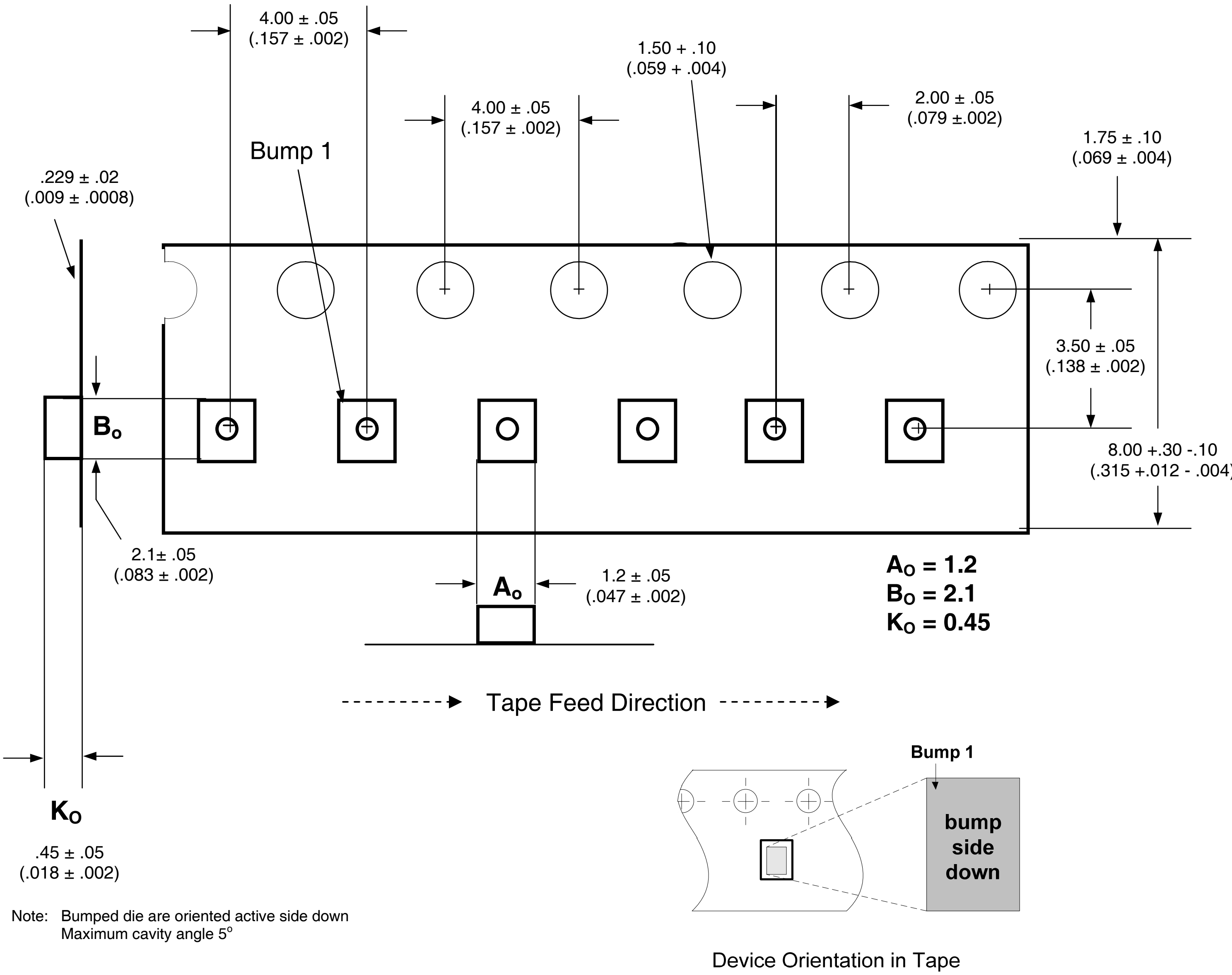
Ball pitch is 400 µm.

Figure 18. Pad Layout (Bumps Up)



Singulated Die size: 1.1 X 2.0 mm (400 µm ball pitch)

Figure 19. Tape and Reel Specifications



Note: Bumped die are oriented active side down
Maximum cavity angle 5°

Drawing not drawn to scale, pocket hole diameter 0.6 ± 0.05 mm

Table 8. Ordering Information

Order Code	Package	Specification	Shipping Method
PE42556DI	Die on cut Tape and Reel	81-0012	Loose or cut tape
PE42556DI-Z	Die on full Tape and Reel	81-0012	1,000 Dice / Reel
PE42556DBI	Die in waffle pack	81-0015	204 Dice / Waffle pack
EK42556-01	Evaluation Kit		1/ box

Sales Contact and Information

For Sales and contact information please visit www.psemi.com.