PAM3131

3A Adjustable Low Voltage Low Dropout CMOS Regulator

Key Features

- Low-Dropout Regulator Supports Input Voltages Down to 1.4V
- Low Dropout Voltage: 300mV@ 3A
- Output Voltage Adjustable from 0.9V-3.3V
- Stable with a Ceramic Output Capacitor of 1.0μF or Higher
- Low Quiescent Current
- Current Limit
- Over Temperature Shutdown
- Short Circuit Current Protection
- Low Temperature Coefficient
- Standard TO-263 and PSOP-8 (Exposed Pad) Packages
- Pb-Free Package

Applications

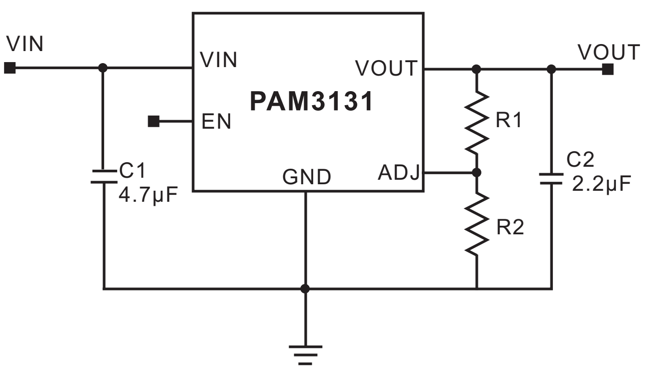
- DSP, FPGA, and Microprocessor Power Supplies
- 1.2V Core Voltage for DSPs
- SATA Power Supply
- LCD TV/ Monitors
- Wireless Devices
- Communication Devices
- Portable Electronics
- Post Regulator for SMPS

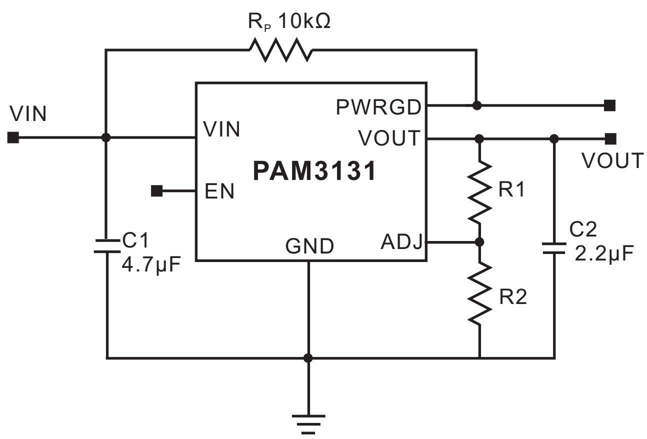
Description

The PAM3131 is a 3A CMOS adjustable LDO regulator that features a low quiescent current, ultra low input, output, and dropout voltages, as well as over temperature protection. It is available in TO-263 and PSOP-8 (Exposed Pad) packages. The output voltage is adjustable from 0.9V to 3.3V. The PAM3131 is stable with a ceramic output capacitor of 1.0μF or higher.

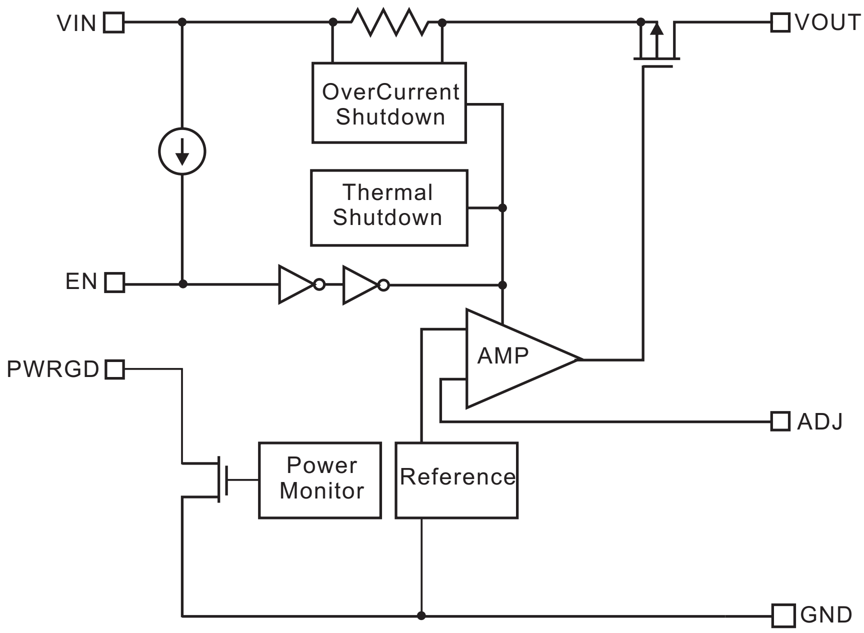
This family of regulators can provide either a stand-alone power supply solution or act as a post regulator for switch mode power supplies. They are particularly well suited for applications requiring low input and output voltages.

Typical Application



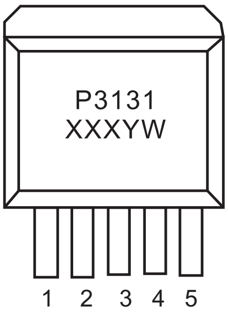


Block Diagram



Pin Configuration & Marking Information

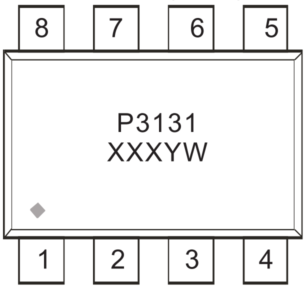
Top View
TO263-5L



P3131: PAM3131
X: Internal Code
Y: Year
W: Week

Pin Number	Name	Function
1	VIN	Input
2	EN	Enable Pin
3	GND	Ground（Heatsink）
4	ADJ	Adjustable Pin
5	VOUT	Output

Top View
PSOP-8 (EPD)



P3131: PAM3131
X: Internal Code
Y: Year
W: Week

Pin Number	Name	Function
1	GND	Ground
2	VIN	Input
3	EN	Enable Pin
4	GND	Ground
5	PWRGD	Power Good
6	ADJ	Adjustable Pin
7	VOUT	Output
8	GND	Ground

Absolute Maximum Ratings

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Input Voltage..4.0V
Output Pin Voltage....................-0.3V to V_{IN} +0.3V
Operation Temperature Range.........-40°C to 85°C
Operation Junction Temperature.....-40°C to 125°C
Maximum Output Current.....................$P_D/(V_{IN}-V_O)$
Storage Temperature................... -65°C to 150°C
Maximum Junction Temperature.................150°C
Soldering Temperature.....................300°C, 5sec

Recommended Operating Conditions

Supply Voltage Range......................1.4V to 3.6V
Operation Temperature Range.........-40°C to 85°C
Junction Temperature Range......... -40°C to 125°C

Thermal Information

Parameter	Symbol	Package	Maximum	Unit
Thermal Resistance (Junction to Case)	θ_{JC}	TO-263	7	°C/W
		PSOP-8	10	
Thermal Resistance (Junction to Ambient)	θ_{JA}	TO-263	35	
		PSOP-8	50	
Internal Power Dissipation (@TA=25°C)	P_D	TO-263	2800	mW
		PSOP-8	2000	

Electrical Characteristic

$V_{IN}=V_O+0.5V$, $T_A=25°C$, $C_{IN}=4.7\mu F$, $C_O=2.2\mu F$, unless otherwise noted.

Parameters	Symbol	Test Conditions		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			Note 1		3.6	V
ADJ Reference Voltage	Vref	Io=100mA		0.882	0.9	0.918	V
Dropout Voltage	V_{DROP}	I_O=500mA	Vo=0.9V		330	500	mV
			Vo=1.0V		220	400	
			2.5V>Vo≥1.2V		50	200	
			Vo≥2.5V		40	150	
		I_O=3.0A	Vo=0.9V		500		
			Vo=1.0V		400		
			2.5V>Vo≥1.2V		350		
			Vo≥2.5V		300		
Short Circuit Current	I_{SC}	Vo < 0.3V			1.0		A
Output Current	I_O			3.0		Note 2	A
Quiescent Current	I_Q	Io=0mA			90	150	μA
Ground Pin Current	I_{GND}	Io=1mA to 3.0A				1.0	mA
Line Regulation	LNR	Vo≤2.5V,Io=10mA V_{IN} =Vo+0.5V to Vo+1.5V			0.2	1.0	%/V
		Vo>2.5V,Io=10mA V_{IN} =3.3V to 3.6V					
Load Regulation	LDR	Io=1mA to 3.0A,V_{IN}=Vo+0.5V			0.5	2	%/A
Over Temperature Shutdown	OTS				150		°C
Over Temperature Hysteresis	OTH				50		°C
Temperature Coefficient	TC				40		ppm/°C
Power Supply Ripple Rejection	PSRR	Io=100mA, Vo=1.5V	f=100Hz		64		dB
			f=1kHz		58		
Output Noise	Vn	f=10Hz to 100kHz			40		μVrms

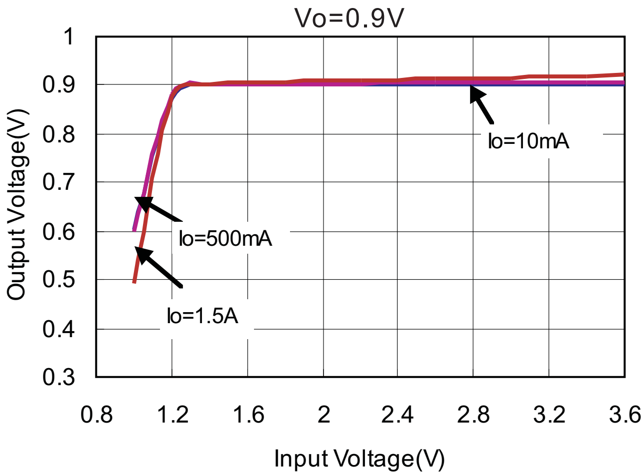
Note1: The minimum input voltage ($V_{IN(MIN)}$) of the PAM3131 is determined by output voltage and dropout voltage. The minimum input voltage is defined as:
$V_{IN(MIN)}=V_O+V_{drop}$

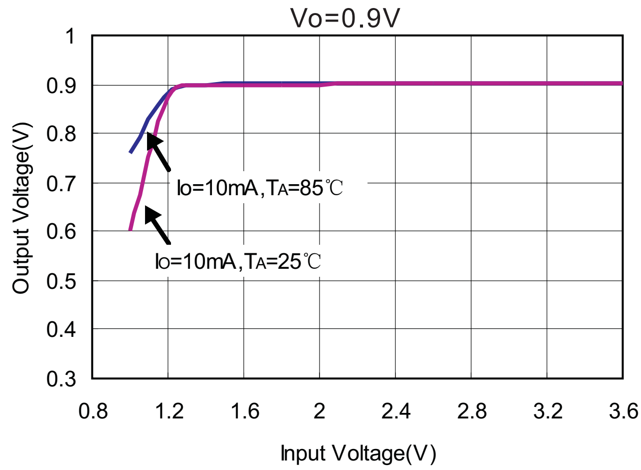
Note 2: Output current is limited by P_D, maximum $I_O=P_D/(V_{IN(MAX)}-V_O)$.

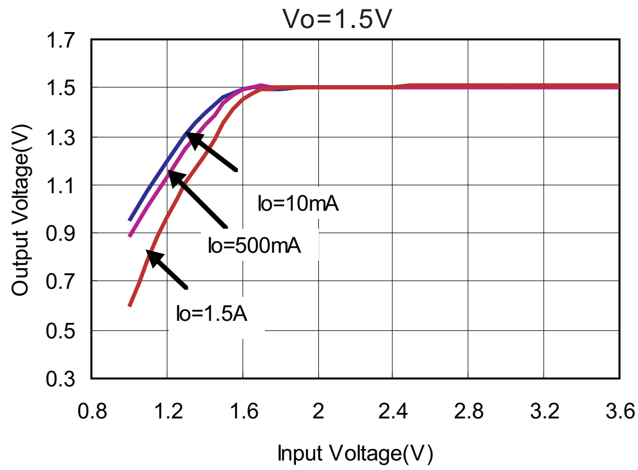
Typical Performance Characteristics

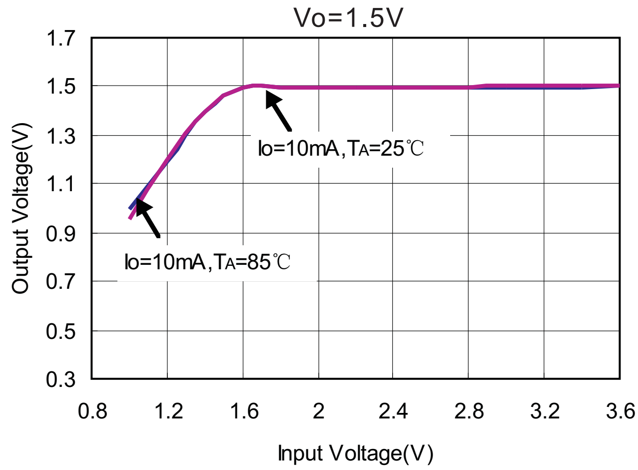
T_A=25°C, C_{IN} =4.7μF, C_O=2.2μF, unless otherwise noted.

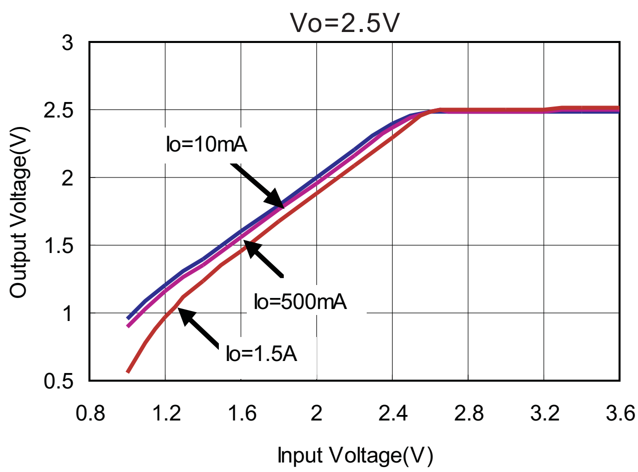
1. Output Voltage vs Input Voltage

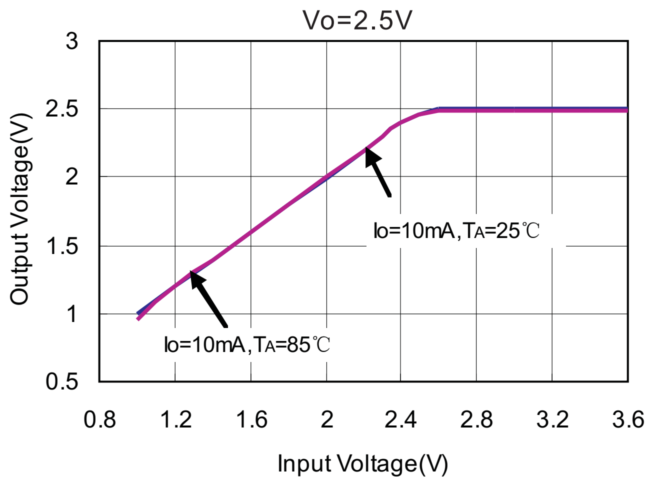






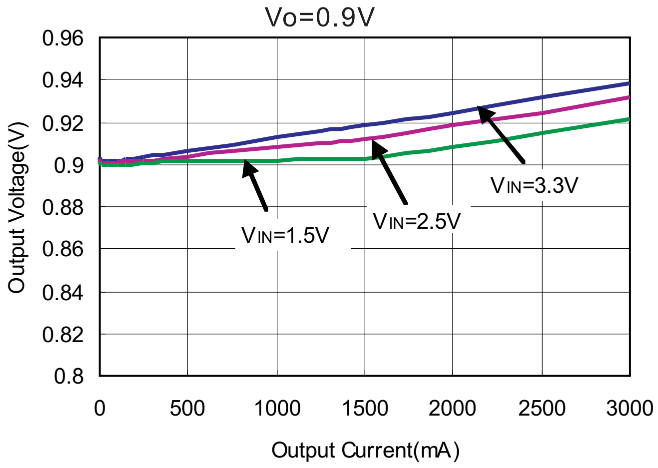


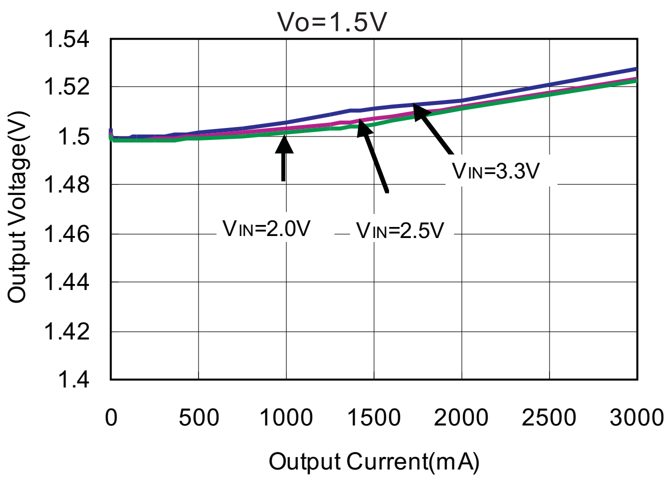


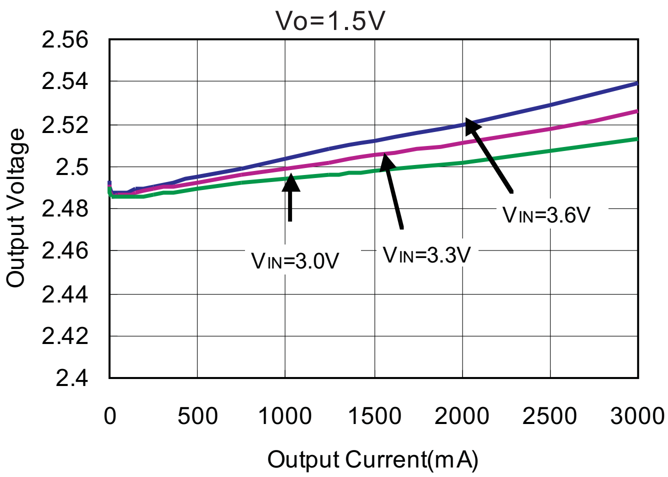


Typical Performance Characteristics (continued)

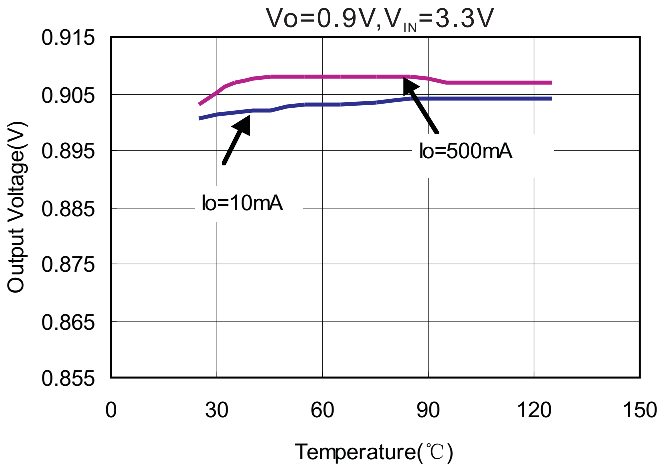
2. Output Voltage vs Output Current

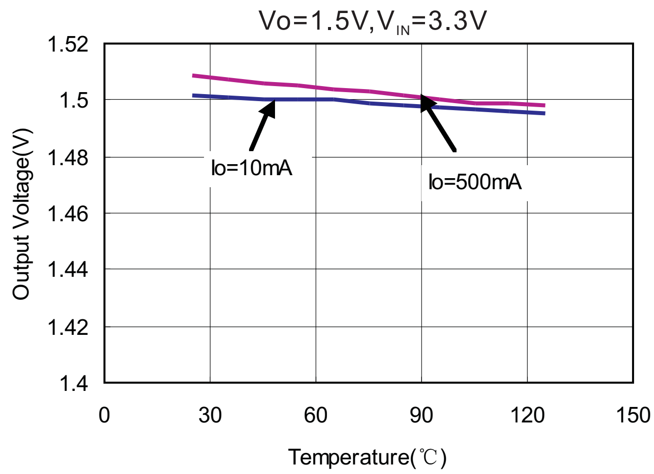


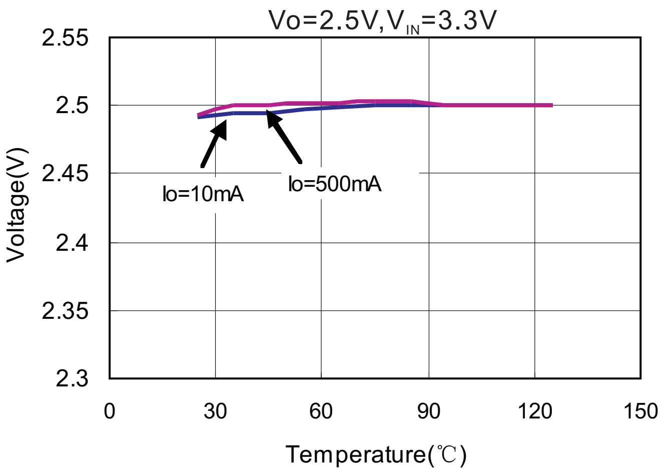




3. Output Voltage vs Temperature

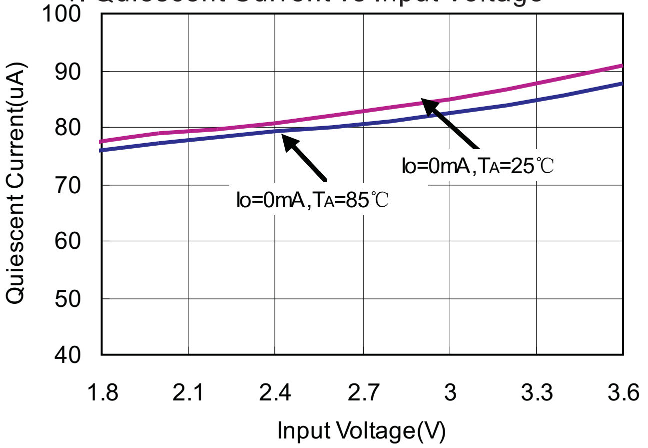




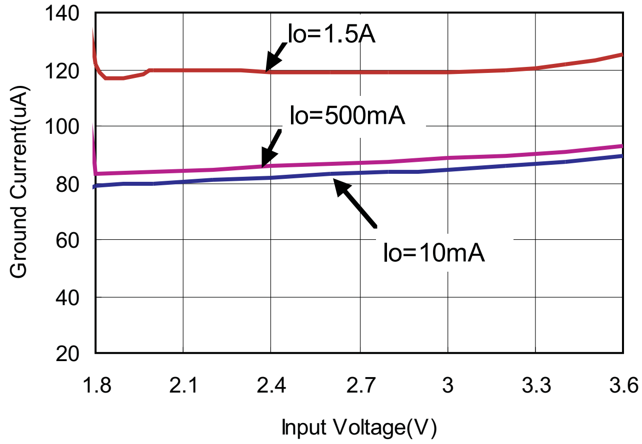


Typical Performance Characteristics (continued)

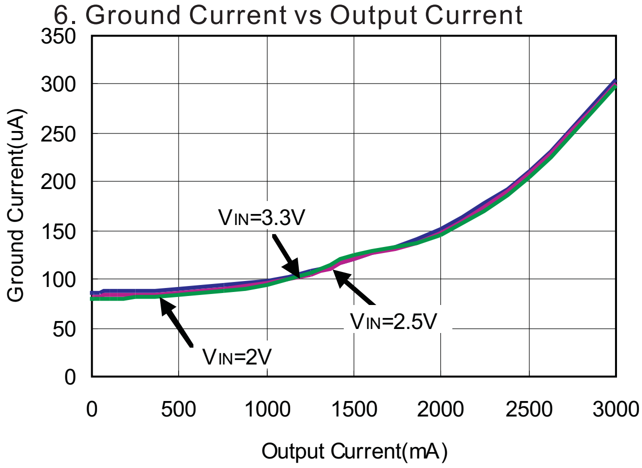
4. Quiescent Current vs Input Voltage



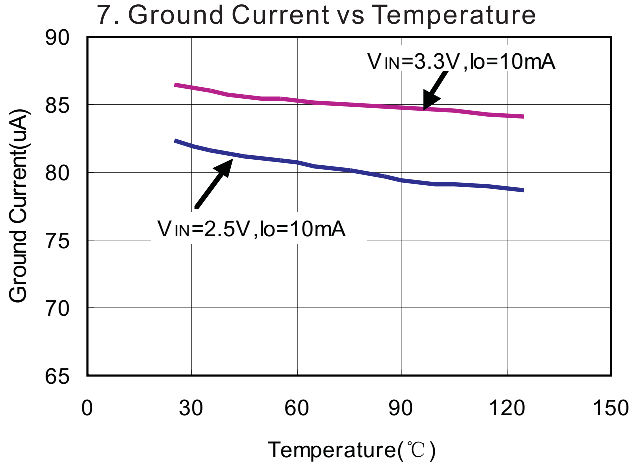
5. Ground Current vs Input Voltage



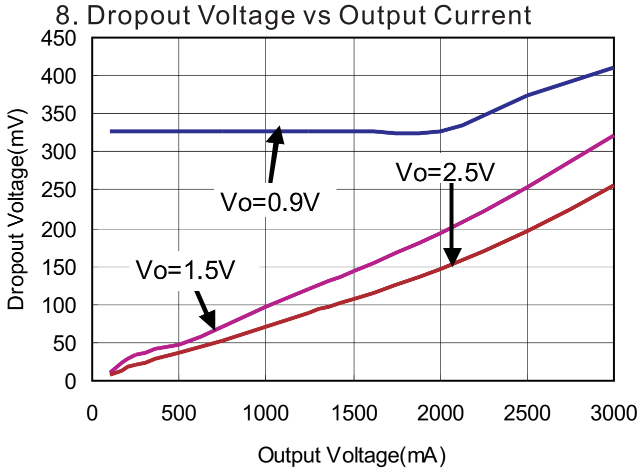
6. Ground Current vs Output Current



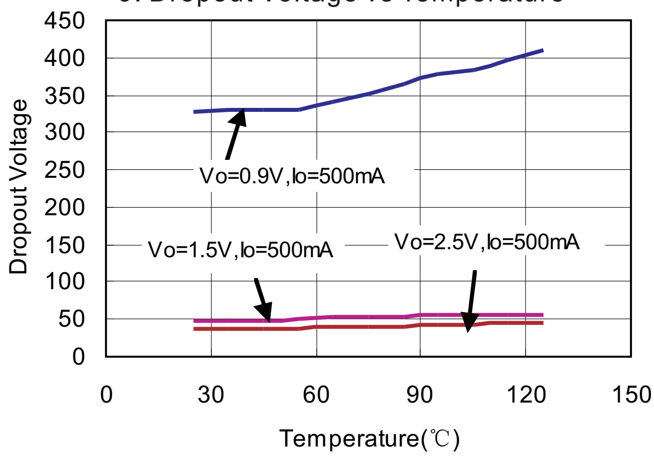
7. Ground Current vs Temperature



8. Dropout Voltage vs Output Current

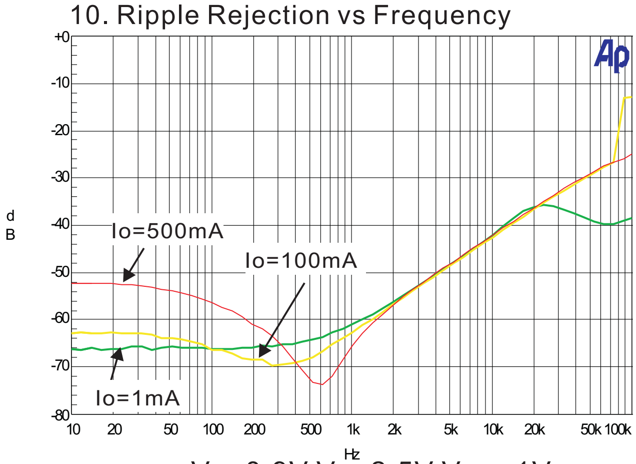


9. Dropout Voltage vs Temperature

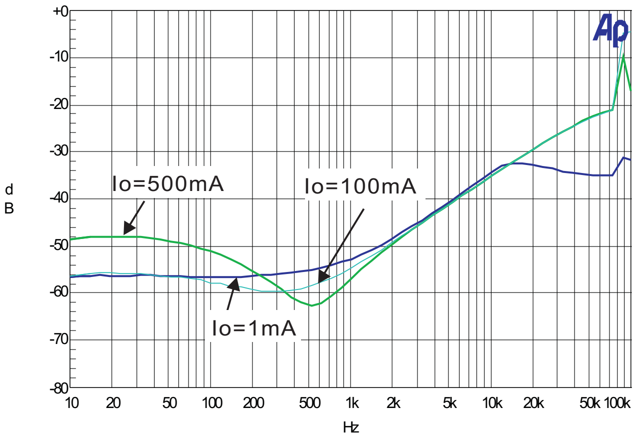


Typical Performance Characteristics (continued)

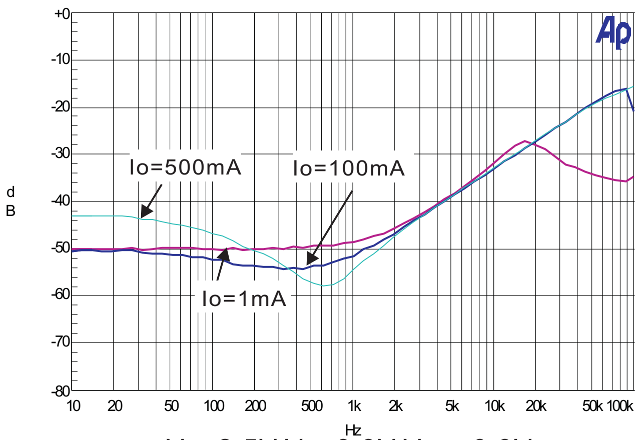
10. Ripple Rejection vs Frequency



Vo=0.9V, V_{IN}=2.5V, Vpp=1V

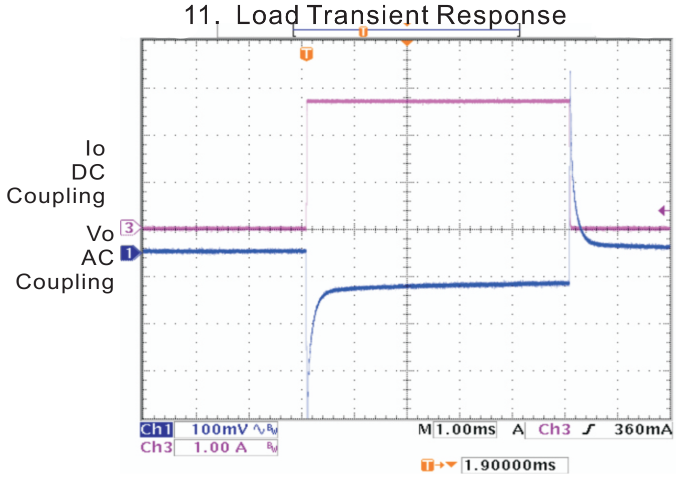


Vo=1.5V, V_{IN}=2.5V, Vpp=1V

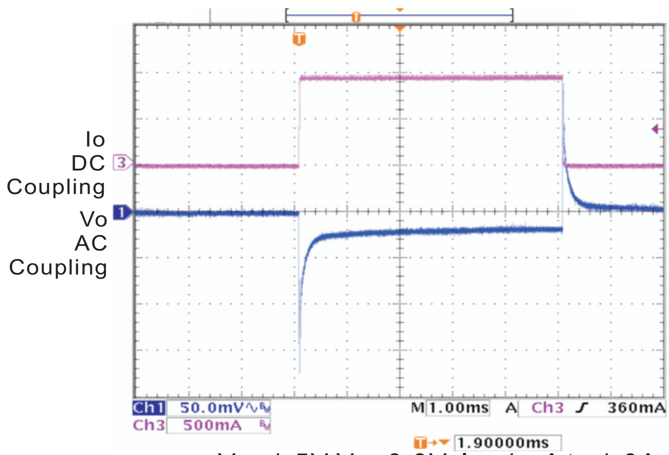


Vo=2.5V, V_{IN}=3.3V, Vpp=0.3V

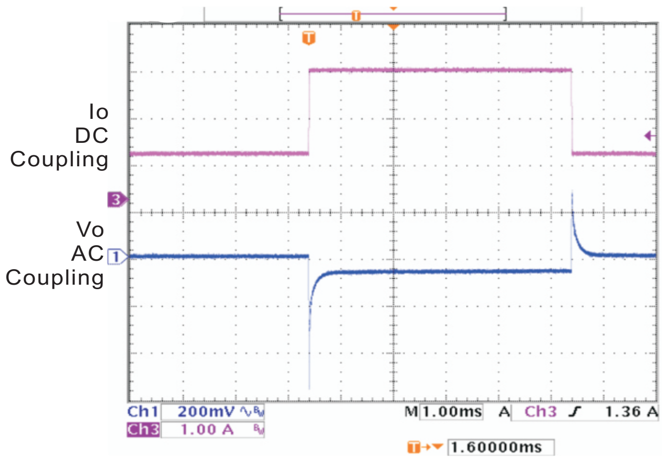
11. Load Transient Response



Vo=1.5V, V_{IN}=3.3V, Io=1mA to 3.0A



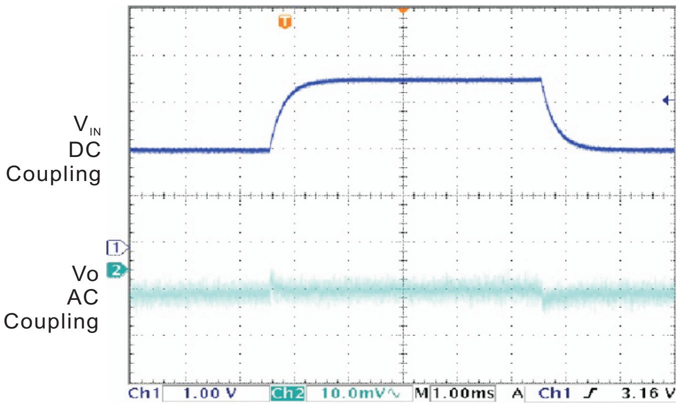
Vo=1.5V, V_{IN}=3.3V, Io=1mA to 1.0A



Vo=1.5V, V_{IN}=3.3V, Io=1A to 3.0A

Typical Performance Characteristics (continued)

12. Line Transient Response



Vo=1.5V,Io=100mA, V_{IN}=2.0V to 3.3V

Application Information

The PAM3131 family of low-dropout (LDO) regulators have several features that allow them to apply to a wide range of applications. The family operates with very low input voltage (1.4V) and low dropout voltage (typically 300mV at full load), making it an efficient stand-alone power supply or post regulator for battery or switch mode power supplies. The 3A output current make the PAM3131 family suitable for powering many microprocessors and FPGA supplies. The PAM3131 family also has low output noise (typically 40μVRMS with 2.2μF output capacitor), making it ideal for use in telecom equipment.

External Capacitor Requirements

A 2.2μF or larger ceramic input bypass capacitor, connected between V_{IN} and GND and located close to the PAM3131, is required for stability. A 1.0μF minimum value capacitor from V_O to GND is also required. To improve transient response, noise rejection, and ripple rejection, an additional 10μF or larger, low ESR capacitor is recommended at the output. A higher value, low ESR output capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source, especially if the minimum input voltage of 1.4V is used.

Regulator Protection

The PAM3131 features internal current limiting, thermal protection and short circuit protection. During normal operation, the PAM3131 limits output current to about 4.5A. When current limiting engages, the output voltage scales back linearly until the over current condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C, thermal-protection circuitry will shut down. Once the device has cooled down to approximately 50°C below the high temp trip point, regulator operation resumes. The short circuit current of the PAM3131 is about 1A when its output pin is shorted to ground.

Output Adjustment

The PAM3131 uses external feedback resistors to generate an output voltage from 0.9V to 3.3V. V_{adj} is trimmed to 0.9V and V_{OUT} is given by the equation: $V_{OUT} = V_{adj}\,(1 + R1 / R2)$

Feedback resistors R1 and R2 should be high enough to keep quiescent current low, but increasing R1+R2 will reduce stability. In general, R1 and R2 in the 10's of kΩ will produce adequate stability, given reasonable layout precautions. To improve stability characteristics, keep parasitics on the ADJ pin to a minimum, and lower R1 and R2 values.

Thermal Information

The amount of heat that an LDO linear regulator generates is: $P_D=(V_{IN}-V_O)I_O$.

All integrated circuits have a maximum allowable junction temperature (T_J max) above which normal operation is not assured. A system designer must design the operating environment so that the operating junction temperature (T_J) does not exceed the maximum junction temperature (T_J max). The two main environmental variables that a designer can use to improve thermal performance are air flow and external heatsinks. The purpose of this information is to aid the designer in determining the proper operating environment for a linear regulator that is operating at a specific power level.

In general, the maximum expected power (P_D(max)) consumed by a linear regulator is computed as:

$$P_{D}max=\left(V_{I(avg)}-V_{O(avg)}\right)\times I_{O(avg)}+V_{I(avg)}\times I_{(Q)} \quad (1)$$

Where:
- $V_{I(avg)}$ is the average input voltage.
- $V_{O(avg)}$ is the average output voltage.
- $I_{O(avg)}$ is the average output current.
- $I_{(Q)}$ is the quiescent current.

For most LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term $V_{I(avg)} \times I_{(Q)}$ can be neglected. The operating junction temperature is computed by adding the ambient temperature (T_A) and the increase in temperature due to the regulator' s power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ($R_{\theta JC}$), the case to heatsink ($R_{\theta CS}$), and the heatsink to ambient ($R_{\theta SA}$). Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation so that the object 's thermal resistance will be lower.

Ordering Information

PAM3131 X X X X

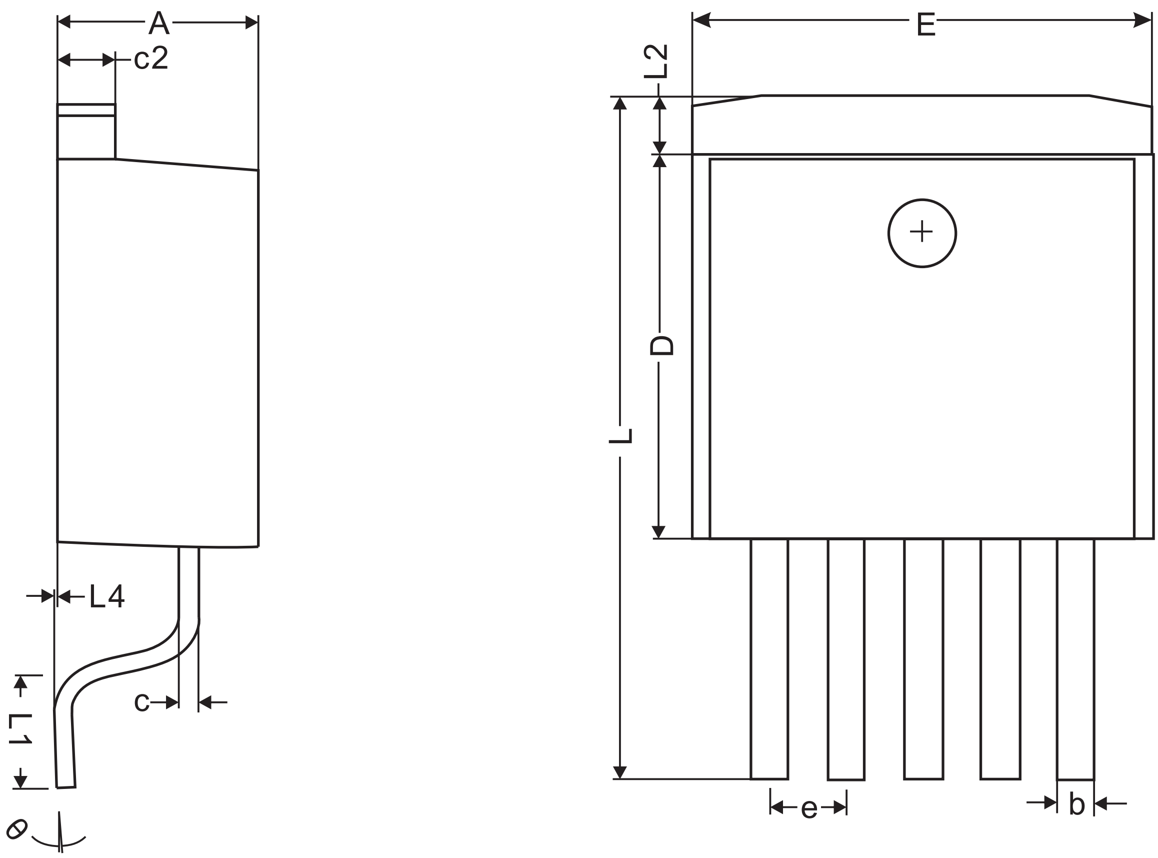
- Packing
- Number of Pins
- Package Type
- Pin Configuration

Pin Configuration	Package Type	Number of Pins
A Type 1. VIN 2. EN 3. GND 4. ADJ 5. VOUT B Type 1. GND 2. VIN 3. EN 4. GND 5. PWRGD 6. ADJ 7. VOUT 8. GND	M: TO-263 E: PSOP	B: 5 C: 8

Part Number	Package Type	Standard Package
PAM3131AMBR	TO263-5L	800 Units/Tape&Reel
PAM3131BECR	PSOP-8	2,500 Units/Tape&Reel

Outline Dimension

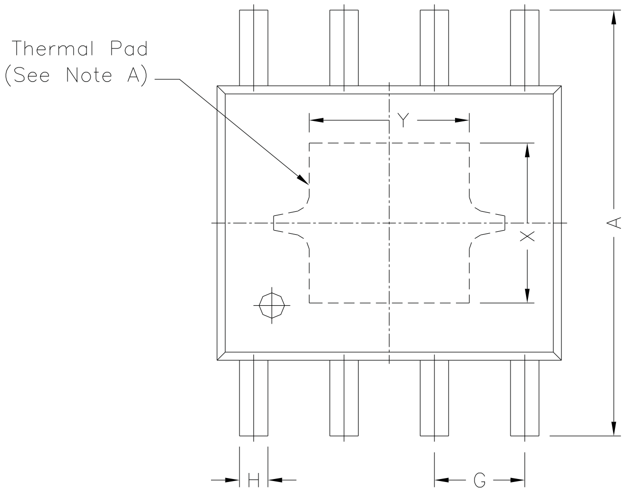
TO263-5L



Dimensions(Millimeter)			
Symbol	MIN	NOM	MAX
A	4.40	4.60	4.80
b	0.66	0.78	0.91
L4	0.00	0.15	0.30
c	0.36	0.43	0.50
L3	1.50 REF.		
L1	2.29	2.54	2.79
E	9.80	10.1	10.4
c2	1.25	1.35	1.45
L2	1.27 REF.		
D	8.6	8.8	9.0
e	1.70 REF.		
L	14.6	15.2	15.8
θ	0º	4º	8º

Outline Dimension

PSOP-8



REF.		DIMENSIONS Millimeters Min.	DIMENSIONS Millimeters Max.
A		5.80	6.20
B		4.80	5.00
C		3.80	4.00
D		0°	8°
E		0.40	0.90
F		0.19	0.25
M		0	0.15
H		0.35	0.49
L		1.35	1.75
G		1.27 TYP.	
Option1	X	2.28	
Option1	Y	2.28	
Option2	X	2.41	
Option2	Y	3.30