

FDC655AN

Single N-Channel, Logic Level, PowerTrench™ MOSFET

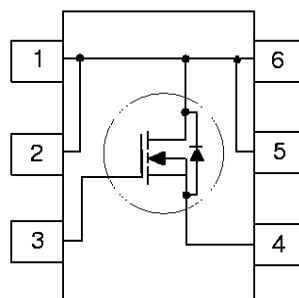
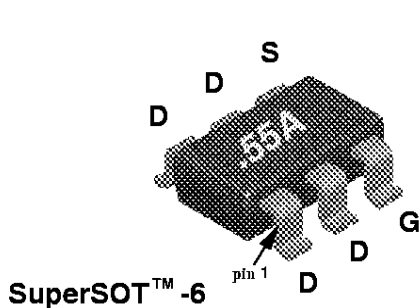
General Description

This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- 6.3 A, 30 V. $R_{DS(ON)} = 0.027 \Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 0.035 \Omega @ V_{GS} = 4.5 \text{ V}$.
- Fast switching.
- Low gate charge (typical 9 nC).
- SuperSOT™-6 package: small footprint (72% smaller than SO-8); low profile (1mm thick); pin compatible with TSOP-6.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise note

Symbol	Parameter	FDC655AN	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage - Continuous	± 20	V
I_D	Drain Current - Continuous (Note 1a)	6.3	A
	- Pulsed	20	
P_D	Maximum Power Dissipation (Note 1a) (Note 1b)	1.6	W
		0.8	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	30	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		23		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 55^\circ\text{C}$			1	μA
					10	μA
I_{DSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{DSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.6	3	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		-4.2		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 6.3\text{ A}$ $T_J = 125^\circ\text{C}$		0.023	0.027	Ω
				0.035	0.045	
				$V_{GS} = 4.5\text{ V}, I_D = 5.5\text{ A}$		0.029
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	20			A
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 6.3\text{ A}$		4.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		830		pF
C_{oss}	Output Capacitance			185		pF
C_{rss}	Reverse Transfer Capacitance			80		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		6	12	ns
t_r	Turn - On Rise Time			10	18	ns
$t_{D(off)}$	Turn - Off Delay Time			18	29	ns
t_f	Turn - Off Fall Time			5	12	ns
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 6.3\text{ A},$ $V_{GS} = 5\text{ V}$		9	13	nC
Q_{gs}	Gate-Source Charge			2.8		nC
Q_{gd}	Gate-Drain Charge			3.1		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Continuous Source Diode Current				1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)		0.73	1.2	V

Notes

1 $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a 78°C/W when mounted on a minimum on a 1 in^2 pad of 2oz Cu in FR-4 board

b 156°C/W when mounted on a minimum pad of 2oz Cu in FR-4 board

2 Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$

Typical Electrical Characteristics

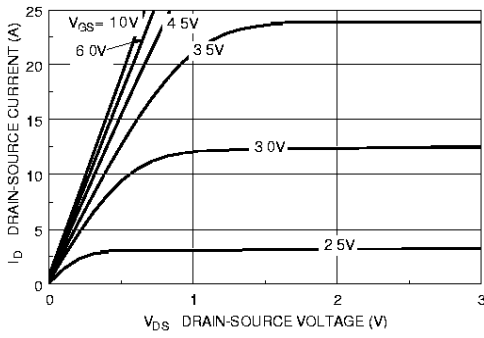


Figure 1. On-Region Characteristics.

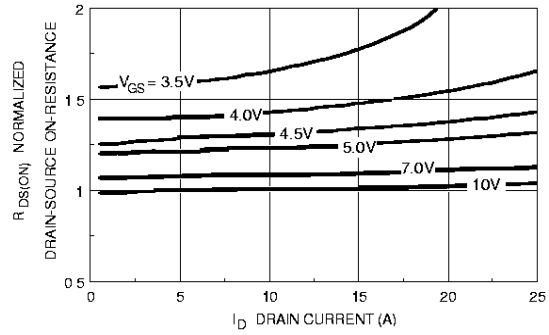


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

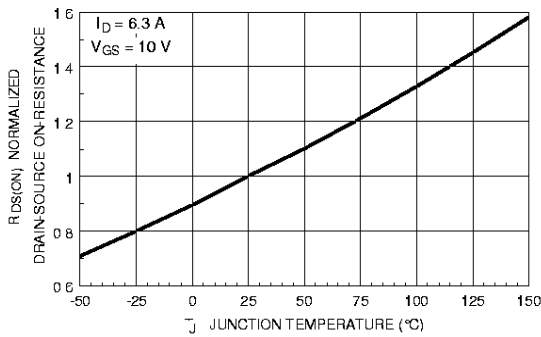


Figure 3. On-Resistance Variation with Temperature.

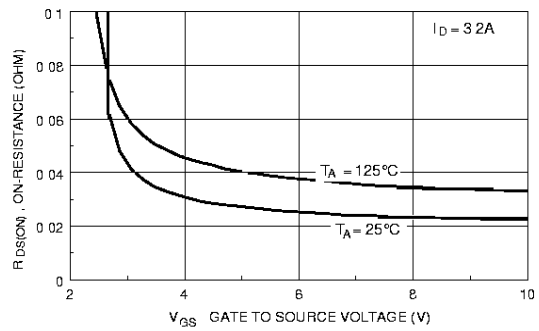


Figure 4. On-Resistance Variation with Gate-To-Source Voltage.

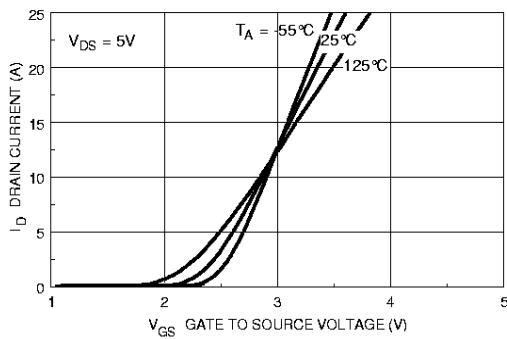


Figure 5. Transfer Characteristics.

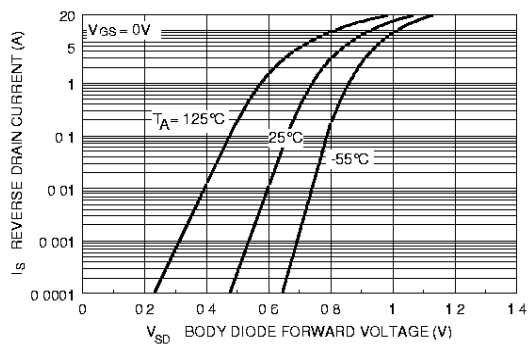


Figure 6. Body Diode Forward Voltage Variation with Source Current

Typical Electrical Characteristics

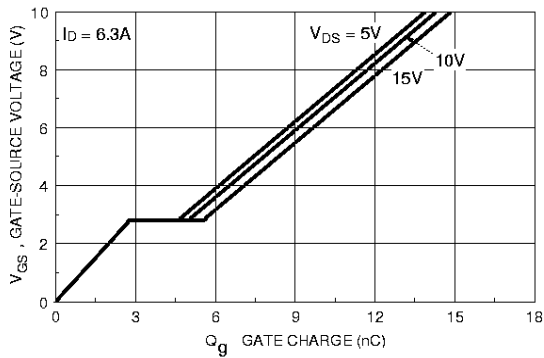


Figure 7. Gate Charge Characteristics.

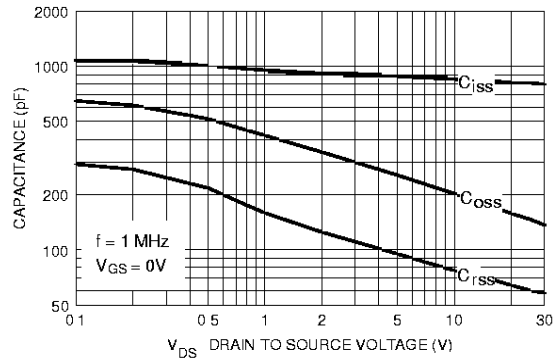


Figure 8. Capacitance Characteristics.

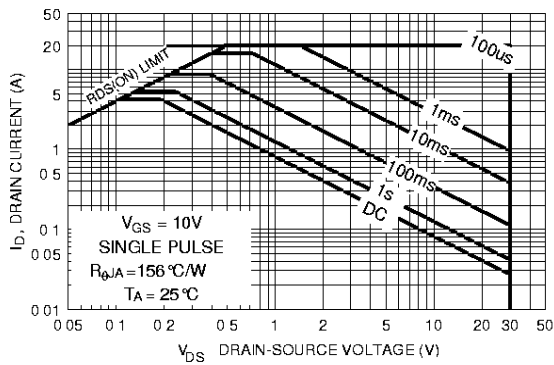


Figure 9. Maximum Safe Operating Area.

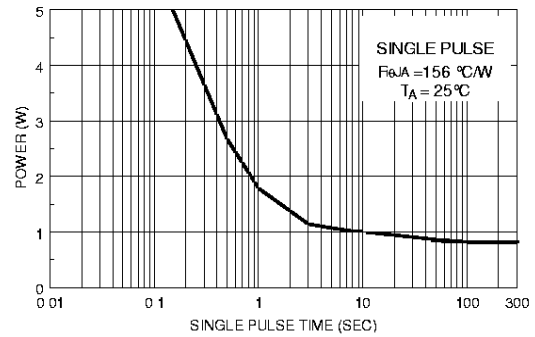


Figure 10. Single Pulse Maximum Power Dissipation.

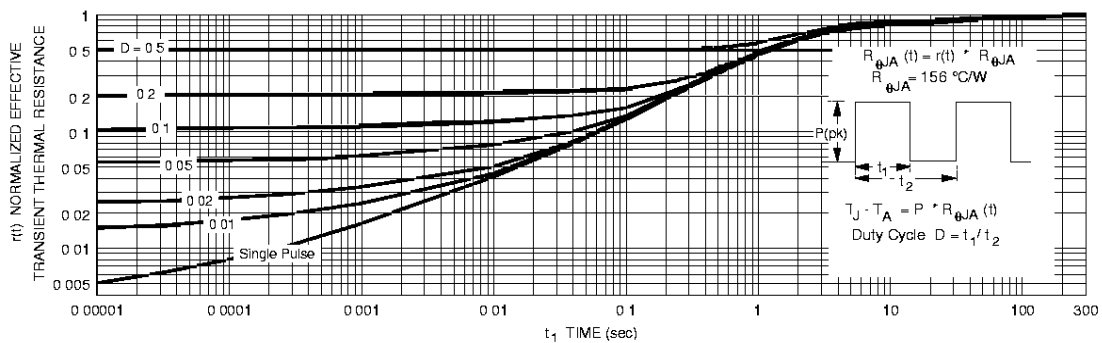


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1b
Transient thermal response will change depending on the circuit board design