24V, 3A DC-DC Synchronous Buck Converter

## Features

- **Wide Input Voltage Range from 7.5V to 24V**
- **3A Continuous Output Current**
- **Adjustable Output Voltage from 0.8V to 20V**
- **$V_{REF}$=0.8V±1% over all Load & Line Regulation & TC Range**
- **Integrated High/Low Side MOSFET**
- **High Efficiency Performance up to 95% scale**
- **Low Shutdown Current <1μA scale**
- **Built-in Internal 1.5ms Soft-Start & Soft-Stop Functions**
- **Fixed 600kHz Switching Frequency with Maximum 90% Duty**
- **Force PWM Mode Operation**
- **Built-in Current Mode Control for Fast Response & MLCC supports with Internal**
- **Stable with Low ESR Capacitors**
- **Power-On-Reset Detection on VCC & VIN**
- **Over-Temperature Protection**
- **Over Voltage Protection**
- **Current-Limit Protection with Frequency Foldback**
- **Enable/Shutdown Function**
- **Current-Mode Operation with Internal Compensation**
- **Small TDFN3x3-10 packages**
- **Lead Free and Green Devices Available (RoHS compliant)**

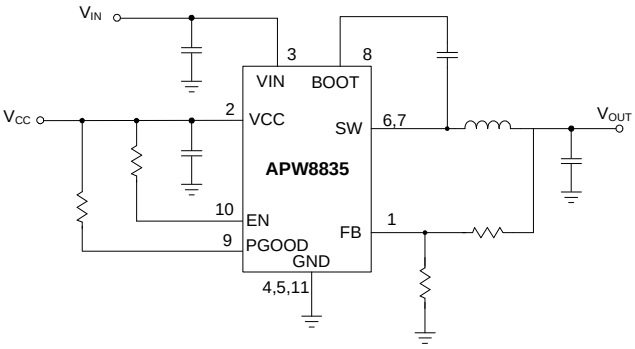
## General Description

APW8835 is a 3A synchronous buck converter with integrated power MOSFETs. The APW8835 design with a current-mode control scheme, can convert wide input voltage of 7.5V to 24V to the output voltage adjustable from 0.8V to 20V to provide excellent output voltage regulation.

The APW8835 is equipped with force PWM mode operation.

The APW8835 is also equipped with Power-on-reset, soft start and whole protections (under-voltage, over-voltage, over-temperature and current-limit) into a single package. This device, available TDFN3x3-10 provides a very compact system solution external components and PCB area.

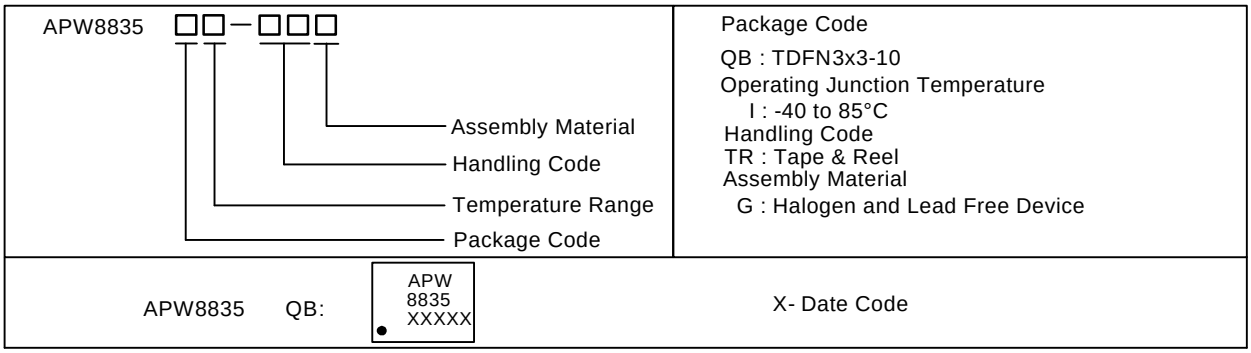
## Simplified Application Circuit




## Applications

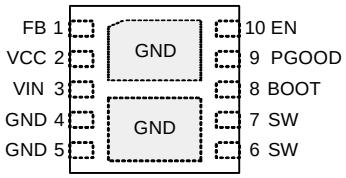
- **LCD Minitor/TV**
- **Set-Top Box**
- **DSL, Switch HUB**
- **Notebook Computer**

## Ordering and Marking Information




Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Pin Configuration




**TDFN3x3-10**
**(Top View)**

## Absolute Maximum Ratings (Note 1)

| Symbol | Parameter | | Rating | Unit |
|---|---|---|---|---|
| $V_{IN}$ | VIN Supply Voltage (VIN to GND) | | -0.3 ~ 30 | V |
| $V_{CC}$ | VCC Supply Voltage (VCC to GND) | | -0.3~6.5 | V |
| $V_{SW}$ | SW to GND Voltage | > 20ns | -1 ~$V_{IN}$+0.3 | V |
| | | < 20ns | -3 ~ $V_{IN}$+3 | V |
| | EN, FB, PGOOD to GND Voltage | | -0.3 ~ 6.5 | V |
| $V_{BOOT}$ | BOOT to GND Voltage | | $V_{SW}$-0.3 ~ $V_{SW}$+6 | V |
| $P_D$ | Power Dissipation | | Internally Limited | W |
| $T_J$ | Junction Temperature | | 150 | °C |
| $T_{STG}$ | Storage Temperature | | -65 ~ 150 | °C |
| $T_{SDR}$ | Maximum Lead Soldering Temperature(10 Seconds) | | 260 | °C |

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Thermal Characteristics

| Symbol | Parameter | Typical Value | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-Ambient Resistance in free air (Note 2) | 55 | °C/W |

Note 2: $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air.

## Recommended Operating Conditions (Note 3)

| Symbol | Parameter | Range | Unit |
|---|---|---|---|
| $V_{IN}$ | VIN Supply Voltage | 7.5 ~ 24 | V |
| $V_{CC}$ | VCC Supply Voltage | 3 ~ 5.5 | V |
| $V_{OUT}$ | Converter Output Voltage | 0.8 ~ 20 | V |
| $I_{OUT}$ | Converter Output Current | 0 ~ 3 | A |
| $V_{IH\_EN}$ | EN High-Level Input Voltage | 1.6~5 | V |
| $V_{IL\_EN}$ | EN Low-Level Input Voltage | 0~0.4 | V |
| $T_A$ | Ambient Temperature | -40 ~ 85 | °C |
| $T_J$ | Junction Temperature | -40 ~ 125 | °C |

Note 3: Refer to the application circuit.

## Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN}$=12V, $V_{CC}$=5V, $V_{EN}$=5V. Typical values are at $T_A$=25°C.

| Symbol | Parameter | Test Conditions | APW8835 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **SUPPLY CURRENT** | | | | | | |
| $I_{VCC}$ | VCC Supply Current | $V_{FB}$=0.8V | - | 1.1 | - | mA |
| $I_{VCC\_SD}$ | VCC Shutdown Supply Current | $V_{EN}$=0V | - | - | 1 | µA |
| **POWER-ON-RESET (POR)** | | | | | | |
| | VIN POR Voltage Threshold | $V_{IN}$ Rising | 6.4 | 6.9 | 7.4 | V |
| | VIN POR Voltage Hysteresis | $V_{IN}$ Falling | - | 0.6 | - | V |
| | VCC POR Voltage Threshold | $V_{CC}$ Rising | 2.65 | 2.8 | 2.95 | V |
| | VCC POR Voltage Hysteresis | $V_{CC}$ Falling | - | 0.3 | - | V |
| **REFERENCE VOLTAGE** | | | | | | |
| $V_{REF}$ | Reference Voltage | | - | 0.8 | - | V |
| | Output Voltage Accuracy | $I_{OUT}$=10mA~3A, $V_{CC}$=3~5V, $T_A$=25°C | -1.5 | - | +1.5 | % |
| **OSCILLATOR AND DUTY CYCLE** | | | | | | |
| $F_{OSC}$ | Oscillator Frequency | | - | 600 | - | kHz |
| | Maximum Converter's Duty | | - | 90 | - | % |
| | Minimum on Time | | - | 100 | - | ns |
| **POWER MOSFET** | | | | | | |
| | High Side MOSFET Resistance | $I_{OUT}$=3A | - | 70 | 105 | mΩ |
| | Low Side MOSFET Resistance | $I_{OUT}$=3A | - | 70 | 105 | mΩ |
| | High Side MOSFET Leakage Current | $V_{EN}$=0V, $V_{SW}$=0V, $V_{IN}$=24V | - | - | 10 | µA |
| | Low Side MOSFET Leakage Current | $V_{EN}$=0V, $V_{SW}$=24V, $V_{IN}$=24V | - | - | 10 | µA |

## Electrical Characteristics

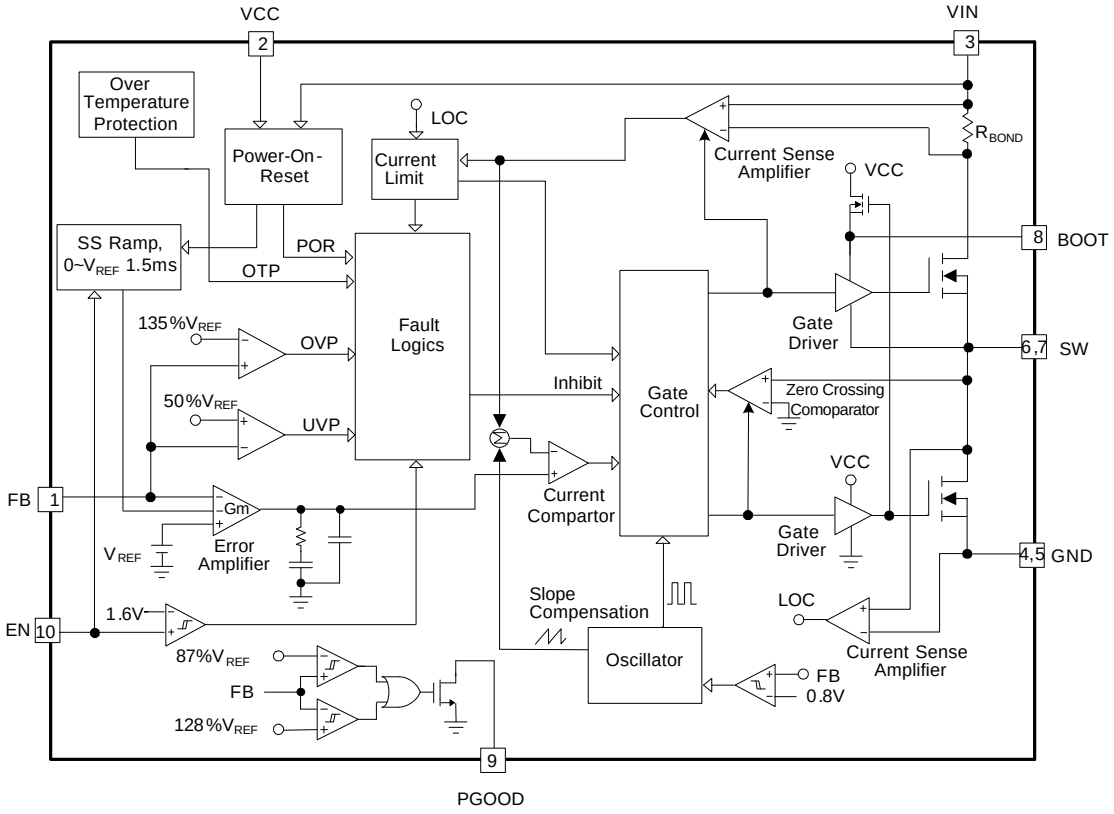
Unless otherwise specified, these specifications apply over $V_{IN}$=12V, $V_{CC}$=5V, $V_{EN}$=5V. Typical values are at $T_A$=25°C.

| Symbol | Parameter | Test Conditions | APW8835 | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| **BOOTSTRAP POWER** | | | | | | |
| | Bootstrap Switch Drop Voltage | $I_F$ = 10mA | - | | 0.2 | V |
| | BOOT Leakage Current | $V_{EN}$=0V, $V_{CC}$=5V, $V_{IN}$=$V_{SW}$=19V, $V_{BOOT}$=24V | - | - | 10 | μA |
| **CURRENT-MODE PWM CONVERTER** | | | | | | |
| gm | Error Amplifier Transconductance | | | 800 | | uA/V |
| | Error Amplifier DC Gain | | - | 80 | - | dB |
| $T_D$ | Dead Time | | | 20 | | ns |
| **PROTECTIONS** | | | | | | |
| | High Side MOSFET current-limit | | - | 5.3 | - | A |
| | Low Side Switch Current-Limit | | - | 1 | - | A |
| $T_{OTP}$ | Over-temperature Trip Point | | - | 150 | - | °C |
| | Over-temperature Hysteresis | | - | 20 | - | °C |
| | Over- Voltage Protection | | 130 | 135 | 140 | %$V_{REF}$ |
| | Under- Voltage Protection | | 45 | 50 | 55 | %$V_{REF}$ |
| **SOFT-START, ENABLE AND INPUT CURRENTS** | | | | | | |
| $T_{SS}$ | Soft-Start Time | | 0.8 | 1.5 | 2 | ms |
| | Enable High Level Voltage | VEN rising | 1.6 | - | - | V |
| | Enable Low Level Voltage | VEN falling | - | - | 0.4 | V |
| **POWER GOOD** | | | | | | |
| | PGOOD in from lower (PGOOD goes high) | $V_{OUT}$ rising | 87 | 90 | 93 | %$V_{OUT}$ |
| | PGOOD low hysteresis | $V_{OUT}$ falling | - | 5 | - | %$V_{OUT}$ |
| | PGOOD in from higher (PGOOD goes high) | $V_{OUT}$ falling | 122 | 125 | 128 | %$V_{OUT}$ |
| | PGOOD high hysteresis | $V_{OUT}$ rising | - | 5 | - | %$V_{OUT}$ |
| | PGOOD Pull Low Resistance | | - | 100 | - | Ω |

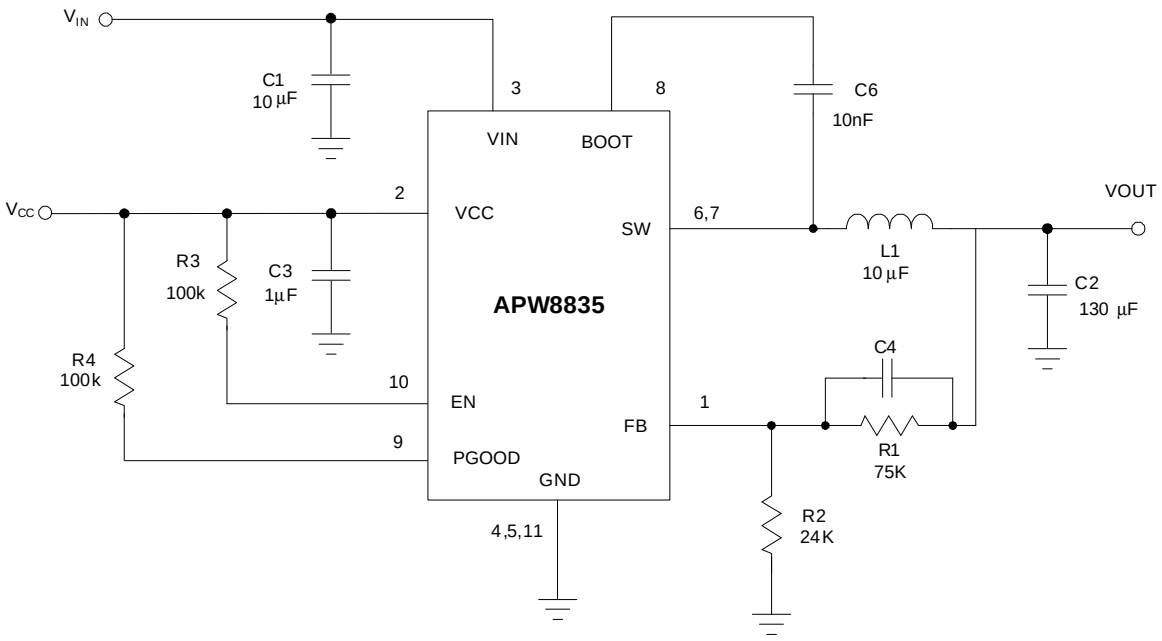
## Pin Description

| PIN | | FUNCTION |
|---|---|---|
| NO. | NAME | |
| 1 | FB | Output Feedback Input. The APW8835 senses the feedback voltage via FB and regulates the voltage at 0.8V. Connecting FB with a resistor-divider from the converter's output sets the output voltage. |
| 2 | VCC | Signal Input. The VCC supplies the control circuitry, gate driver. Connect a ceramic bypass capacitor from VCC to GND. |
| 3 | VIN | Power Input. The VIN supplies the step-down converter switches. Connect a ceramic bypass capacitor from VIN to GND. |
| 4 | GND | Ground. Power and signal ground. |
| 5 | GND | |
| 6 | SW | Power Switching Output. The SW is the junction of the high-side and low-side power MOSFET to supply power to the output LC filter. |
| 7 | SW | |
| 8 | BOOT | High-side Gate driver supply Voltage input. The BOOT supplies the voltage to drive the high-side N-channel MOSFET. |
| 9 | PGOOD | Power Good Output. This pin is an open-drain logic output that is pulled to the ground when the $V_{FB}$ voltage is out of window. This pin needs a resistor to pull high when PGOOD signal is used. |
| 10 | EN | Enable pin of the PWM converter. When the EN is above high logic level, the device is in operation mode. When the EN is below low logic level, the device is in shutdown mode. This pin can not be left open. |
| 11 | - | GND and Exposed pad. Connect the exposed pad to the system ground plane with large copper area for dissipating heat into the ambient air. |

## Block Diagram



## Typical Application Circuit



## Function Description

### Main Control Loop

The APW8835 is a constant frequency current mode switching regulator. During normal operation, the internal N-channel power MOSFET is turned on each cycle when the oscillator sets an internal RS latch and would be turned off when an internal current comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the COMP pin, which is the output of the error amplifier (EAMP). An external resistive divider connected between VOUT and ground allows the EAMP to receive an output feedback voltage VFB at FB pin. When the load current increases, it causes a slight decrease in VFB relative to the 0.8V reference, which in turn causes the COMP voltage to increase until the average inductor current matches the new load current.

### VIN and VCC Power-On-Reset (POR)

The APW8835 keeps monitoring the voltage on VIN and VCC pin to prevent wrong logic operations which may occur when VIN or VCC voltage is not high enough for the internal control circuitry to operate.

After the VIN, VCC and EN voltages exceed their respective voltage thresholds, the IC starts a start-up process and then ramps up the output voltage to the setting of output voltage.

### Soft-Start

The APW8835 provides the soft-start function to limit the inrush current. The soft-start time is fixed in 1.5ms.

### Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW8835 When the junction temperature exceeds $T_J$=+150°C, a thermal sensor turns off the N-channel power MOSFET, allowing the device to cool down. The thermal sensor allows the converter to start a start-up process and regulate the output voltage again after the junction temperature cools by 20°C. The OTP designed with a 20°C hysteresis lowers the average $T_J$ during continuous thermal overload conditions, increasing life time of the APW8835.

### Enable/Shutdown

Driving EN to ground places the APW8835 in shutdown. When in shutdown, the internal N-Channel power MOSFET turns off, all internal circuitry shuts down and the quiescent supply current reduces to 0.3µA. Connect a RC network from EN to GND to set a turn-on delay that can be used to sequence the output voltages of multiple devices.

### Current-Limit Protection

The APW8835 monitors the output current, flowing through the N-Channel power MOSFET, and limits the current peak at current-limit level to prevent loads and the IC from damages during overload, short-circuit and over-voltage conditions.

### Foldback Frequency

The foldback frequency is controlled by the FB voltage. When the FB pin voltage is under 80% of reference ($V_{REF}$), the frequency of the oscillator will be reduced to 110kHz. This lower frequency allows the inductor current to safely discharge, thereby preventing current runaway. The oscillator¡¦s frequency will switch to its designed rate when the feedback voltage on FB rises above the rising frequency foldback threshold (85% of $V_{REF}$, typical) again.

### Boostrap Capacitor

The APW8835 is an N-channel MOSFET step down converter. The MOSFET requires a gate voltage that is higher than input voltage, thus a boost capacitor should be connected between LX and BS pins to drive the gate of the N-channel MOSFET. Typical boostrap capacitor value is 10nF.

## Function Description (Cont.)

**Output Under-Voltage Protection (UVP)**

In the operational process, if a short-circuit occurs, the output voltage will drop quickly. Before the current-limit circuit responds, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the FB voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, the IC shuts down converter's output.

The under-voltage threshold is 50% of the nominal output voltage. The under-voltage comparator has a built-in 3ms noise filter to prevent the chips from wrong UVP shutdown being caused by noise. The APW8835 will be latched after under-voltage protection.

**Over-Voltage Protection (OVP)**

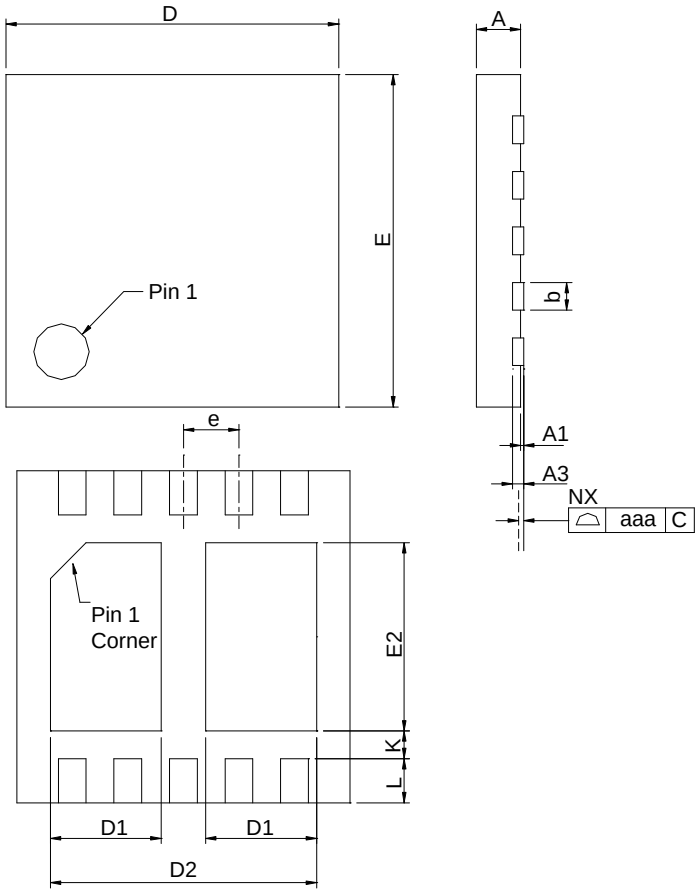
The over-voltage function monitors the output voltage by FB pin. When the FB voltage increases over 135% of the reference voltage due to the high-side MOSFET failure or for other reasons, the over-voltage protection comparator will force the low-side MOSFET gate driver high. This action actively pulls down the output voltage and eventually attempts to blow the internal bonding wires. The APW8835 will be latched after over-voltage protection.

**Power OK Indicator**

PGOOD is actively held low in shutdown and soft-start status.In the soft-start process, the PGOOD is an open-drain. When the soft-start is finished, the PGOOD is released. In normal operation, the PGOOD window is from 90% to 125% of the converter reference voltage. When the output voltage has to stay within this window, PGOOD signal will become high after 0.5ms internal delay. When the output voltage outruns 87% or 128% of the target voltage, PGOOD signal will be pulled low immediately. In order to prevent false PGOOD drop, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient.

## Package Information

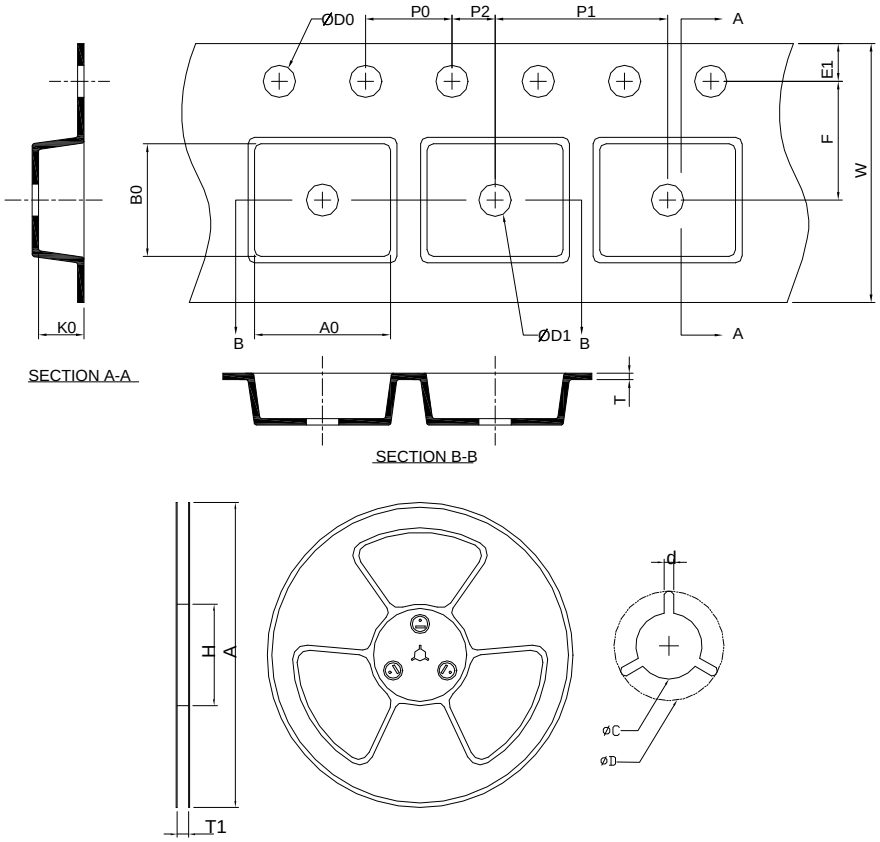
**TDFN3x3-10**




| SYMBOL | TDFN3x3-10C | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.70 | 0.80 | 0.028 | 0.031 |
| A1 | 0.00 | 0.05 | 0.000 | 0.002 |
| A3 | 0.11 REF | | 0.004 REF | |
| b | 0.18 | 0.30 | 0.007 | 0.012 |
| D | 2.90 | 3.10 | 0.114 | 0.122 |
| D1 | 0.92 | 1.13 | 0.036 | 0.044 |
| D2 | 2.20 | 2.40 | 0.087 | 0.094 |
| E | 2.90 | 3.10 | 0.114 | 0.122 |
| E2 | 1.40 | 1.60 | 0.055 | 0.063 |
| e | 0.50 BSC | | 0.020 BSC | |
| L | 0.30 | 0.50 | 0.012 | 0.020 |
| K | 0.20 | | 0.008 | |
| aaa | 0.08 | | 0.003 | |

Note : 1. Followed from JEDEC MO-229 VEED-5.

## Carrier Tape & Reel Dimensions




| Application | A | H | T1 | C | d | D | W | E1 | F |
|---|---|---|---|---|---|---|---|---|---|
| TDFN3x3-10 | 330.0±2.00 | 50 MIN. | 12.4+2.00 -0.00 | 13.0+0.50 -0.20 | 1.5 MIN. | 20.2 MIN. | 12.0±0.30 | 1.75±0.10 | 5.5±0.05 |
| | **P0** | **P1** | **P2** | **D0** | **D1** | **T** | **A0** | **B0** | **K0** |
| | 4.0±0.10 | 8.0±0.10 | 2.0±0.05 | 1.5+0.10 -0.00 | 1.5 MIN. | 0.6+0.00 -0.40 | 3.30±0.20 | 3.30±0.20 | 1.30±0.20 |

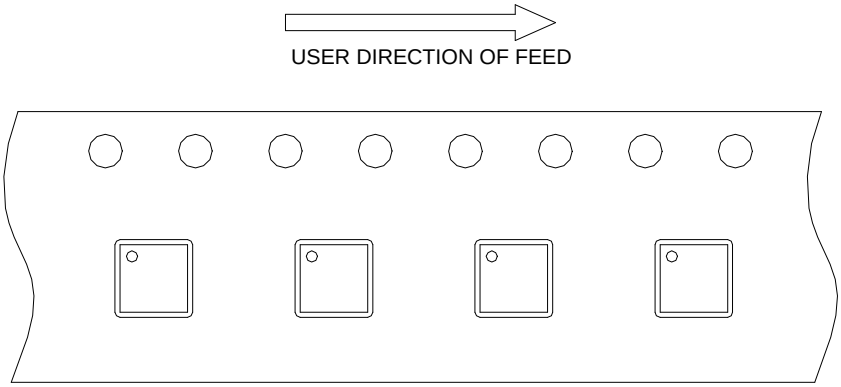
(mm)

## Devices Per Unit

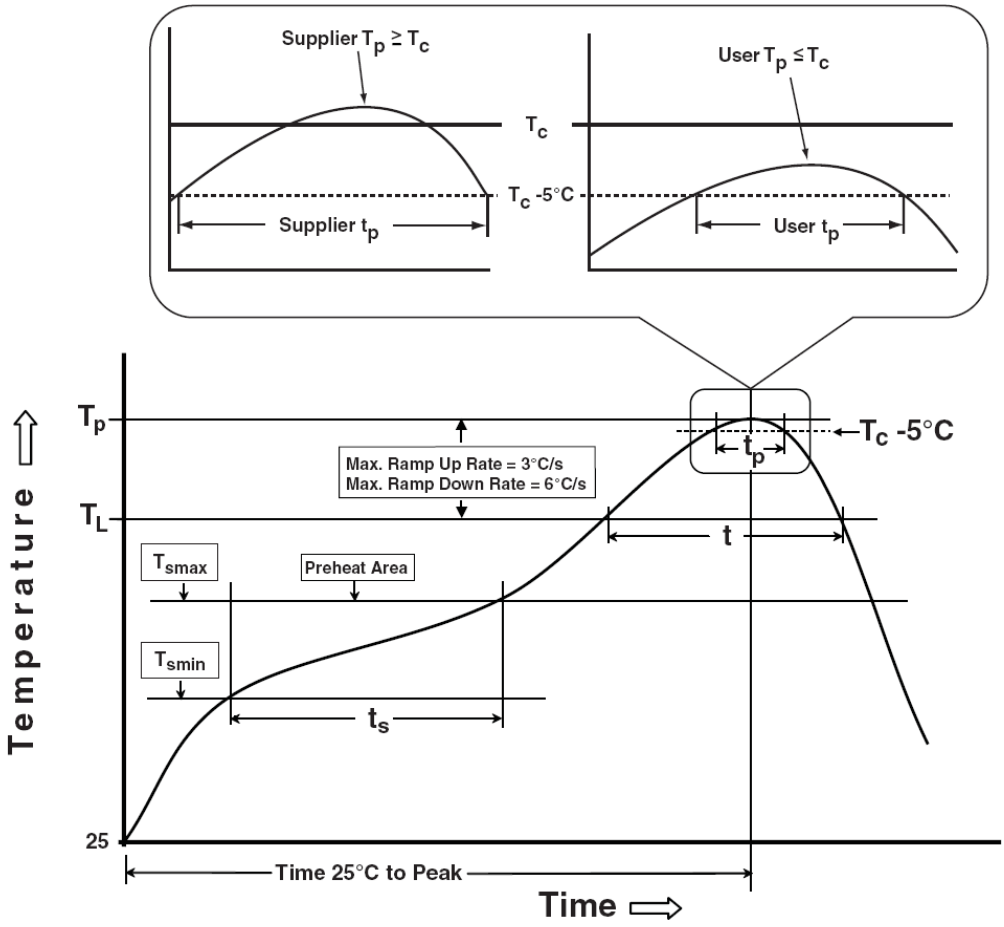
| Package Type | Unit | Quantity |
|---|---|---|
| **TDFN3x3-10** | Tape & Reel | 3000 |

## Taping Direction Information

**TDFN3x3-10**




## Classification Profile



## Classification Reflow Profiles

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|---|---|
| **Preheat & Soak**<br>Temperature min ($T_{smin}$)<br>Temperature max ($T_{smax}$)<br>Time ($T_{smin}$ to $T_{smax}$) ($t_s$) | 100 °C<br>150 °C<br>60-120 seconds | 150 °C<br>200 °C<br>60-120 seconds |
| Average ramp-up rate ($T_{smax}$ to $T_P$) | 3 °C/second max. | 3 °C/second max. |
| Liquidous temperature ($T_L$)<br>Time at liquidous ($t_L$) | 183 °C<br>60-150 seconds | 217 °C<br>60-150 seconds |
| Peak package body Temperature ($T_p$)* | See Classification Temp in table 1 | See Classification Temp in table 2 |
| Time ($t_P$)** within 5°C of the specified classification temperature ($T_c$) | 20** seconds | 30** seconds |
| Average ramp-down rate ($T_p$ to $T_{smax}$) | 6 °C/second max. | 6 °C/second max. |
| Time 25°C to peak temperature | 6 minutes max. | 8 minutes max. |
| * Tolerance for peak profile Temperature ($T_p$) is defined as a supplier minimum and a user maximum.<br>** Tolerance for time at peak profile temperature ($t_p$) is defined as a supplier minimum and a user maximum. | | |

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ ³350 |
|---|---|---|
| <2.5 mm | 235 °C | 220 °C |
| ≥2.5 mm | 220 °C | 220 °C |

Table 2. Pb-free Process – Classification Temperatures (Tc)

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ 350-2000 | Volume $mm^3$ >2000 |
|---|---|---|---|
| <1.6 mm | 260 °C | 260 °C | 260 °C |
| 1.6 mm – 2.5 mm | 260 °C | 250 °C | 245 °C |
| ≥2.5 mm | 250 °C | 245 °C | 245 °C |

## Reliability Test Program

| Test item | Method | Description |
|---|---|---|
| SOLDERABILITY | JESD-22, B102 | 5 Sec, 245°C |
| HOLT | JESD-22, A108 | 1000 Hrs, Bias @ $T_j$=125°C |
| PCT | JESD-22, A102 | 168 Hrs, 100%RH, 2atm, 121°C |
| TCT | JESD-22, A104 | 500 Cycles, -65°C~150°C |
| HBM | MIL-STD-883-3015.7 | VHBM≧2KV |
| MM | JESD-22, A115 | VMM≧200V |
| Latch-Up | JESD 78 | 10ms, $1_{tr}$≧100mA |

## Customer Service

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