SM803020

Flexible Ultra-Low Jitter Clock Synthesizer

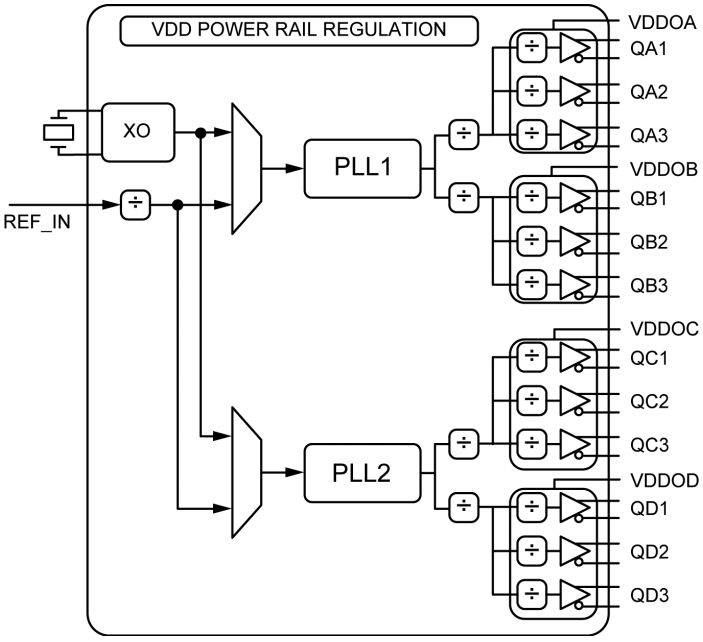
General Description

The SM803020 is a dual-PLL clock generator that achieves ultra-low, 74.2fs_rms output jitter at 156.25MHz output frequency. It accepts a crystal input or a reference input.

Each output channel is individually configurable to a differential PECL, LVDS, HCSL, or CMOS output logic level. PECL is selected by default, but can be overridden through SPI. It is packaged in a dual-row 84-pin 7mm x 7mm package.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Typical Application



Features

- Generates twelve 156.25MHz outputs
- Independently programmable output logic:
  - Output logic: LVPECL (default), LVDS, HCSL, LVCMOS
- 74.2fs jitter at 156.25MHz (1.875MHz to 20MHz)
- Selectable inputs require 39.0625MHz input frequency
  - XTAL (default)
  - Differential or single-ended reference clock (SPI selectable)
- 2.5V or 3.3V operating power supply
- Separate output power supplies:
  - Different banks can be at different levels
- Industrial temperature range (–40°C to +85°C)
- Green, RoHS, and PFOS compliant
- Available in 84-pin 7mm × 7mm QFN package

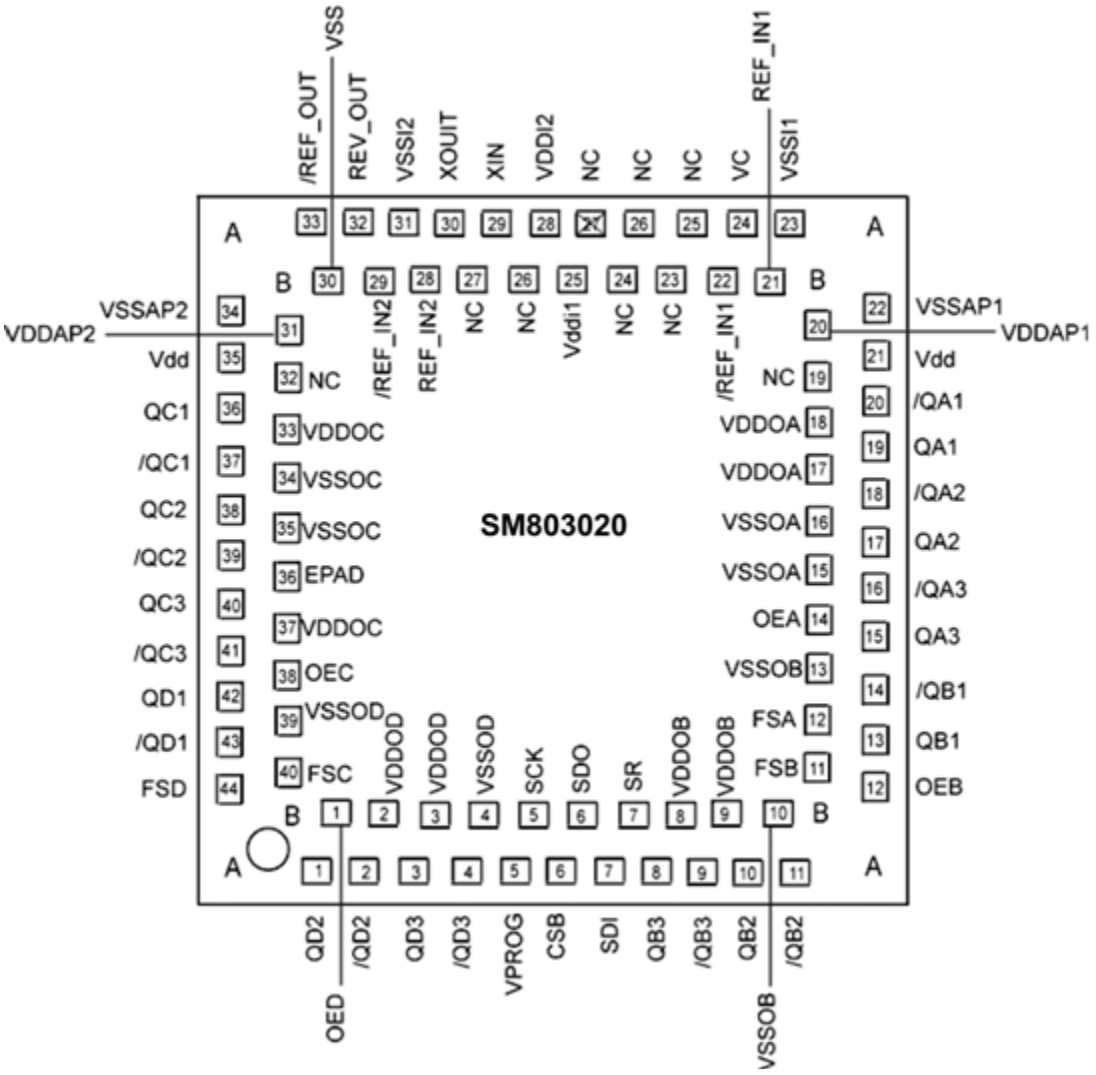
Applications

- 1/10/40/100 Gigabit Ethernet

Ordering Information

Part Number	Marking	Shipping	Ambient Temperature Range	Package
SM803020UMY	803020	Tray	–40°C to +85°C	84-Pin QFN
SM803020UMYR	803020	Tape and Reel	–40°C to +85°C	84-Pin QFN

Pin Configuration



84-Pin QFN 7mm x 7mm

hbwhelp@micrel.com or (408) 955-1690

Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
A19, A20 A17, A18 A15, A16 A13, A14 A10, A11 A8, A9 A36, A37 A38, A39 A40, A41 A42, A43 A1, A2 A3, A4	QA1, /QA1 QA2, /QA2 QA3, /QA3 QB1, /QB1 QB2, /QB2 QB3, /QB3 QC1, /QC1 QC2, /QC2 QC3, /QC3 QD1, /QD1 QD2, /QD2 QD3, /QD3	O, (DIF/SE)	LVPECL	Differential LVPECL (default), HCSL, or LVDS Clock Outputs or Phase-Adjustable Differential or Single-Ended CMOS Outputs
B12 B11 B40 A44	FSEL_A FSEL_B FSEL_C FSEL_D	I, (SE)	LVCMOS	Frequency Select, 75kΩ pull-up 1 = Primary Selection 0 = Secondary Selection
A21, A35	VDD	PWR		Power Supply
B18 B17	VDDOA1 VDDOA2 VDDOA3	PWR		Power Supply for Outputs QA1–3
B8 B9	VDDOB1 VDDOB2 VDDOB3	PWR		Power Supply for Outputs QB1–3
B33 B37	VDDOC1 VDDOC2 VDDOC3	PWR		Power Supply for Outputs QC1–3
B2 B3	VDDOD1 VDDOD2 VDDOD3	PWR		Power Supply for Outputs QD1–3
B20	VDDAP1	PWR		Power Supply for PLL1
B31	VDDAP2	PWR		Power Supply for PLL2
A27, B25	VDDI1	PWR	3.3V only	Power Supply for VCXO, Reference1, Feedback 1
A28	VDDI2	PWR		Power Supply for XO, Reference2, Feedback 2
B30 B36	VSS (Exposed Pad)	PWR		Core Power Supply Ground. The exposed pad must be connected to the VSS ground plane.
B15 B16	VSSOA1 VSSOA2 VSSOA3	PWR		Power Supply Ground for Outputs QA1–3
B10 B13	VSSOB1 VSSOB2 VSSOB3	PWR		Power Supply Ground for Outputs QB1–3

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
B34 B35	VSSOC1 VSSOC2 VSSOC3	PWR		Power Supply Ground for Outputs QC1–3
B4 B39	VSSOD1 VSSOD2 VSSOD3	PWR		Power Supply Ground for Outputs QD1–3
A34	VSSAP1	PWR		Power Supply Ground for PLL1
A22	VSSAP2	PWR		Power Supply Ground for PLL2
A23	VSSI1	PWR		Power Supply Ground for VCXO, Reference1, Feedback 1
A31	VSSI2	PWR		Power Supply Ground for XO, Reference2, Feedback 2
B14	OEA1/2/3	I, (SE)	LVCMOS	Output Enable, Outputs Q0–Q3 disable to tri-state, 0 = Disabled, 1 = Enabled, 75kΩ pull-up
A12	OEB1/2/3	I, (SE)	LVCMOS	Output Enable, Outputs Q4–Q7 disable to tri-state, 0 = Disabled, 1 = Enabled, 75kΩ pull-up
B38	OEC1/2/3	I, (SE)	LVCMOS	Output Enable, Outputs Q4–Q7 disable to tri-state, 0 = Disabled, 1 = Enabled, 75kΩ pull-up
B1	OED1/2/3	I, (SE)	LVCMOS	Output Enable, Outputs Q4–Q7 disable to tri-state, 0 = Disabled, 1 = Enabled, 75kΩ pull-up
A5, A6, A7, B5, B6, B7	TEST	-	-	Factory Test pins. Do not connect anything to these pins.
A32 A33	REFOUT_P, REFOUT_N	I, (Diff/SE)	LVPECL LVDS HCSL LVCMOS	Reference Clock Output
B21 B22	REF1_P, REF1_N	I, (Diff/SE)	LVPECL LVDS HCSL LVCMOS	Reference Clock Input 1
B28 B29	REF2_P, REF2_N	I, (Diff/SE)	LVPECL LVDS HCSL LVCMOS	Reference Clock Input2
B23 B24	FB1_P, FB1_N	I, (Diff/SE)	LVPECL LVDS HCSL LVCMOS	Feedback Clock Input1
B26 B27	FB2_P, FB2_N	I, (Diff/SE)	LVPECL LVDS HCSL LVCMOS	Feedback Clock Input2
A29	XTAL_IN	I, (SE)	12pF crystal	Crystal Reference Input, no load caps needed (See Figure 9.)
A30	XTAL_OUT	O, (SE)	12pF crystal	Crystal Reference Output, no load caps needed (See Figure 9.)

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
B19, B32	NC			
A25	VCXO_OUT	O, SE		VCXO output, 8 to 10pF, programmable
A26	VCXO_IN	I, SE		VCXO input, 8 to 10pF, programmable
A24	VC	I		Control voltage for VCXO, positive slope

Truth Tables

PLL_BYPASS	XTAL_SEL	OEA	OEB	OEC	OED	Input	Output
0	–	1	1	1	1	–	PLL
1	–	1	1	1	1	–	XTAL/REF_IN
–	0	1	1	1	1	REF_IN	–
–	1	1	1	1	1	XTAL	–
–	–	0	1	1	1	–	QA Tri-state
–	–	1	0	1	1	–	QB Tri-state
–	–	1	1	0	1	–	QC Tri-state
–	–	1	1	1	0	–	QD Tri-state

FSEL	Output Frequency (MHz)
1	Primary
0	Secondary

Output Logic Programming

Available output logic types are LVPECL (default), LVDS, HCSL and LVCMOS.

Each output can be programmed individually to any of the four logic types through SPI.

Unused outputs can be disabled to high impedance.

All logic types are differential except LVCMOS. LVCMOS signals are single ended coming out of the Qx pins. During LVCMOS operation the /Qx pins are disabled.

Absolute Maximum Ratings[2]

Supply Voltage (V_{DD}, V_{DDA}, V_{DDI}, V_{DDO}) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.5V to +4.6V
Lead Temperature (soldering, 20s) ..... 260°C
Storage Temperature (Ts) ..... –65°C to +150°C
ESD Machine Model 200V
ESD Human Body Model 2000V

Operating Ratings[3]

Supply Voltage (V_{DD}, V_{DDO}) ..... +2.375V to +3.465V
Ambient Operating Temperature (T_A) ..... –40°C to +85°C
Maximum Allowable Junction Temp ..... 125°C
Junction Thermal Resistance
84-pin QFN 7mm x 7mm θ_{JA} Still Air ..... 24°C/W

Electrical Characteristics

Typical values are T_A = 25°C, min/max across –40°C ≤ T_A ≤ +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}, V_{DDO}	Supply Voltage	2.5V Operation	2.375	2.5	2.625	V
		3.3V Operation	3.135	3.3	3.465	
V_{DDI_1}	Analog Supply Voltage	Note 3	3.135	3.3	3.465	V
V_{DDI_2}	Analog Supply Voltage	Note 3	2.375		3.465	V
V_{DDA}	PLL Core Voltage		2.375		3.465	V
I_{DDA}	PLL Core Current Consumption	Per active PLL			60	mA
I_{DD}	Current Consumption				8	mA
I_{DDI_1}	Input 1 Supply Current	XO Input[3]			0	mA
		Ref Input			2	mA
I_{DDI_2}	Input 2 Supply Current	XO Input[3]			4	mA
		Ref Input			2	mA

LVPECL DC Electrical Characteristics

V_{DDCore} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{DDO} – 2V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	50Ω to V_{DDO} – 2V	V_{DDO} –1.35	V_{DDO} – 1.01	V_{DDO} – 0.8	V
V_{OL}	Output Low Voltage	50Ω to V_{DDO} – 2V	V_{DDO} –2	V_{DDO} – 1.78	V_{DDO} –1.6	V
V_{SWING}	Peak-to-Peak Output Voltage	Figure 2	0.65	0.77	0.95	V

LVDS DC Electrical Characteristics

V_{DDCore} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 100Ω between Q and /Q.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OD}	Differential Output Voltage	Figure 2	245	350	454	mV
V_{CM}	Common Mode Voltage		1.125	1.2	1.375	V
V_{OH}	Output High Voltage		1.248	1.375	1.602	V
V_{OL}	Output Low Voltage		0.898	1.025	1.252	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this datasheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The datasheet limits are not guaranteed if the device exceeds the operating ratings.
3. Crystal input is powered from V_{DDI_2} analog supply voltage source.

HCSL DC Electrical Characteristics

V_{DDCore} = V_{DD} = V_{DD0} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{SS}.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage		600	700	850	mV
V_{OL}	Output Low Voltage		–150	0	27	mV
V_{CROSS}	Crossing Point Voltage			0.350		V

REF_IN DC Electrical Characteristics

V_{DD} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CMR}	Input Common Mode Voltage		0.3		V_{DD} – 0.3	V
V_{SWING}	Input Voltage Swing	Peak to Peak, each side of the Diff Input	0.2			V_{PP}

Crystal Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	12pF Load Typical	Fundamental, Parallel Resonant			
Frequency			39.0625		MHz
Equivalent Series Resistance (ESR)				60	Ω
Load Capacitance, C_L			12		pF
Shunt Capacitor, C0			2	4	pF
Correlation Drive Level			10	100	µW

AC Electrical Characteristics

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

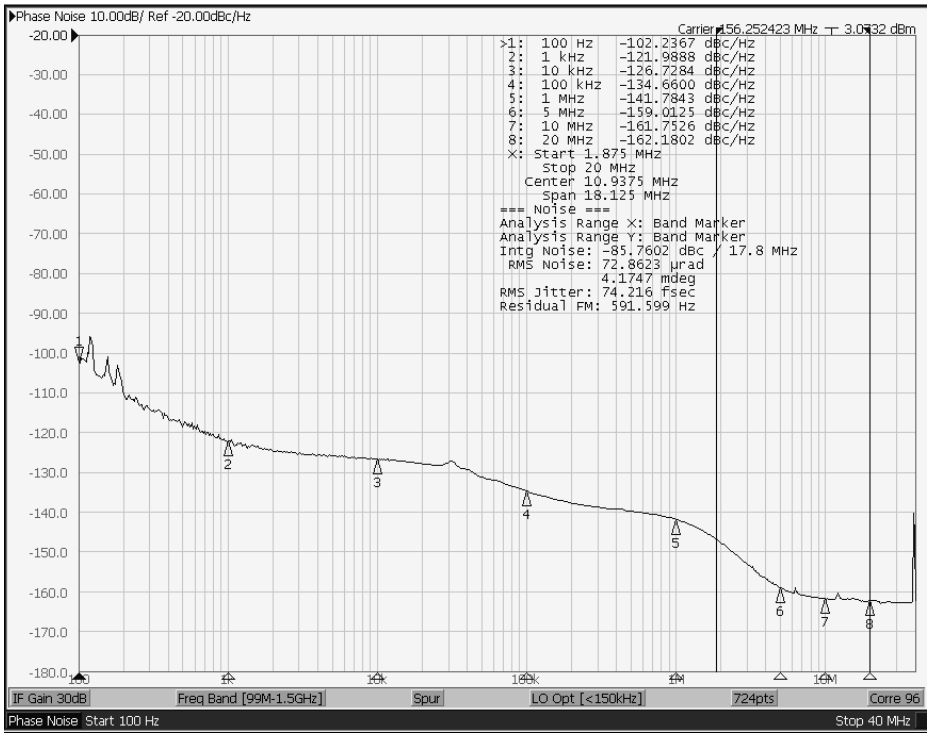
T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{IN}	Input Frequency			39.0625		MHz
F_{OUT}	Output Frequency	LVPECL, LVDS, HCSL, LVCMOS		156.25		MHz
T_R/T_F	Output Rise/Fall Time 20% – 80%	LVPECL output	85	135	350	ps
		LVDS output	85	140	300	ps
		HCSL output	175	340	700	ps
		LVCMOS output	100	200	400	ps
ODC	Output Duty Cycle		45	50	55	%
Tpd	Input to Output Propagation Delay	ZDB mode	–100		100	ps
		Synthesizer/Bypass mode		4		ns
T_{SKEW}	Output-to-Output Skew[4]	Note 5, same output bank			50	ps
T_{LOCK}	PLL Lock Time			5	20	ms
$T_{jit}(\varnothing)$	RMS Phase Jitter[6]	Integration range (12kHz to 20MHz)		180		fs

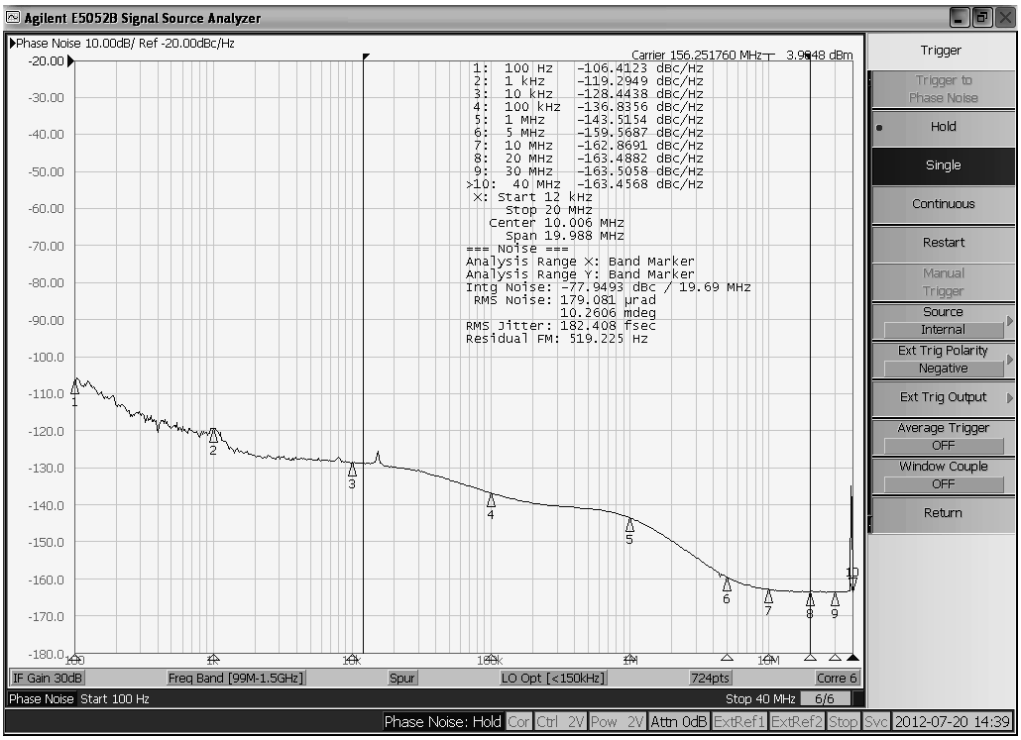
Notes:

4. Defined as skew between outputs at the same supply voltage and with equal load conditions; measured at the output differential crossing points.
5. Output-to-output skew is only defined for outputs in the same PLL bank [A:B, C:D] with the same output type setting.
6. All phase noise measurements were taken with an Agilent 5052B phase noise system.

Phase Noise Performance



156.25MHz, integration range 1.875MHz to 20MHz: 74.2fs rms



156.25MHz, integration range 12kHz to 20MHz: 182.4fs rms

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Application Information

Input Reference

When operating with a crystal input reference, do not apply a switching signal to a REF_IN.

Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal.

Crystal load capacitance is built inside the die so no external capacitance is needed. See the *Selecting a Quartz Crystal for the Clockworks Flex I Family of Precision Synthesizers* application note for more details.

Contact Micrel's HBW applications group if you need help selecting a suitable crystal for your application at: hbwhelp@micrel.com.

Power Supply Filtering Recommendations

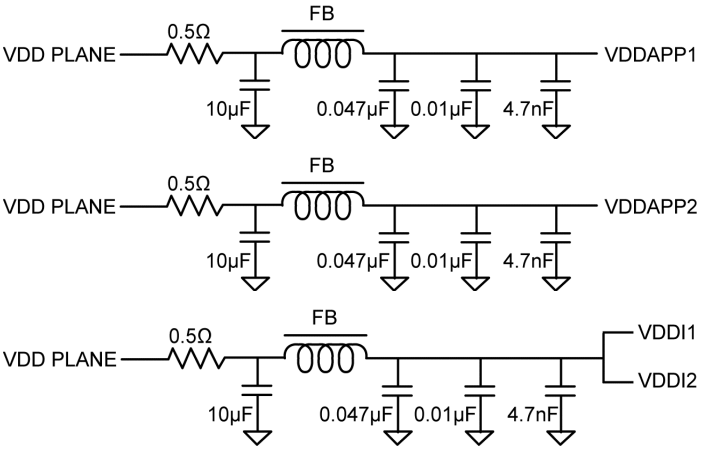

Figure 1. Recommended Power Supply Filtering

- Use the power supply filtering shown in Figure 1 for VDDAP1, VDDAP2, VDDI1 and VDDI2.
- Connect the VDDO and VDD pins directly to the VDD power plane.
- Connect all VSS pins directly to the ground power plane.

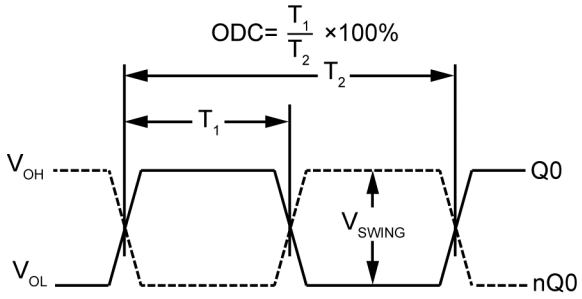

Figure 2. Duty Cycle Timing

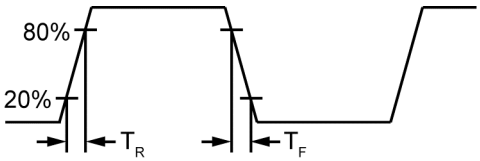

Figure 3. All Outputs Rise/Fall Time

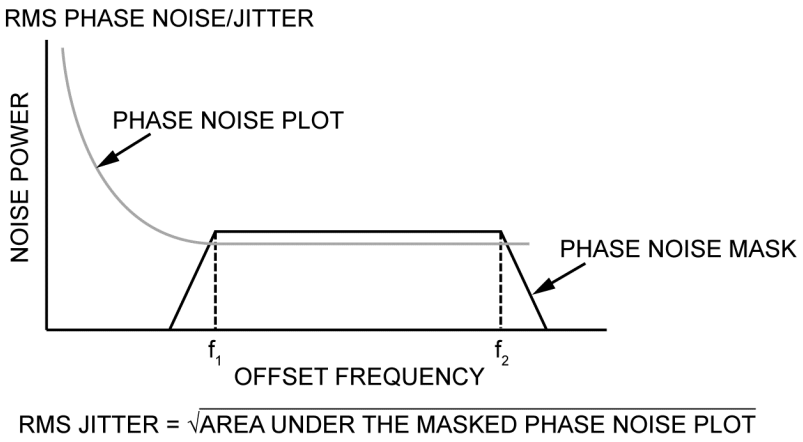

Figure 4. RMS Phase/Noise Jitter

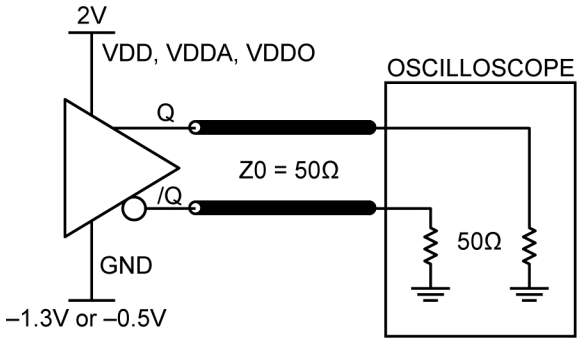

Figure 5. LVPECL Output Load and Test Circuit

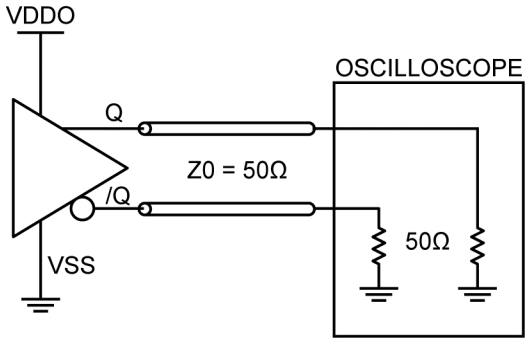

Figure 6. HCSL Output Load and Test Circuit

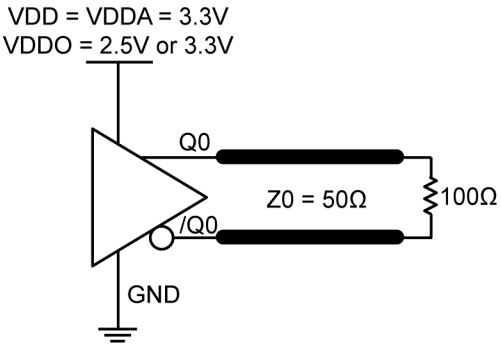

Figure 7. LVDS Output Load and Test Circuit

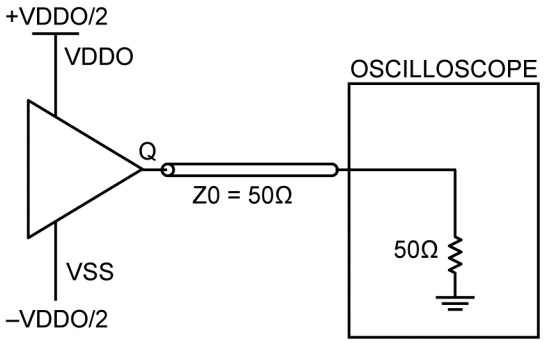

Figure 8. LVCMOS Output Load and Test Circuit

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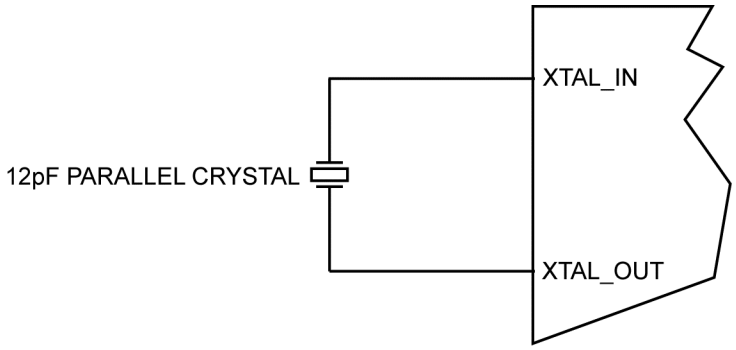
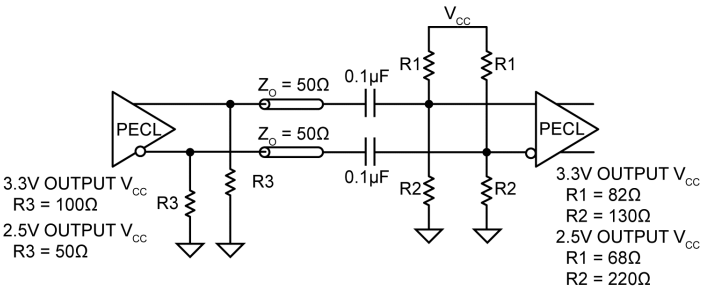


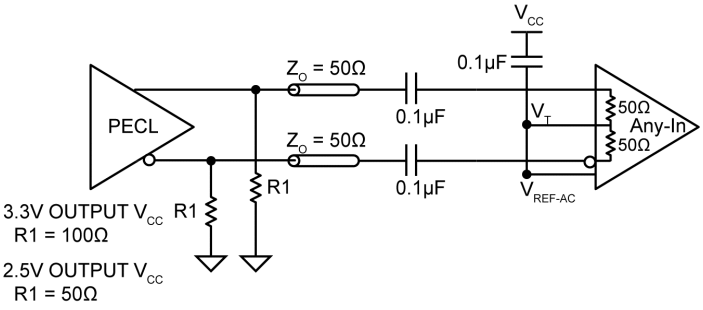
Figure 9. Crystal Input Interface

AC-Coupled Signal Interfacing

PECL

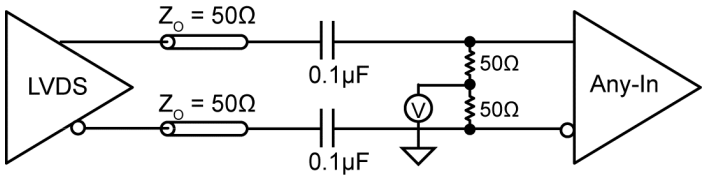


Thevenin Equivalent Conventional Termination

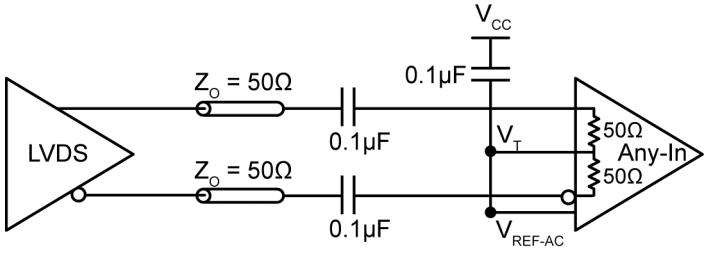


Micrel Any-In Internal Termination

LVDS



LVDS: V source = 1.25V



Micrel Any-In Internal Termination

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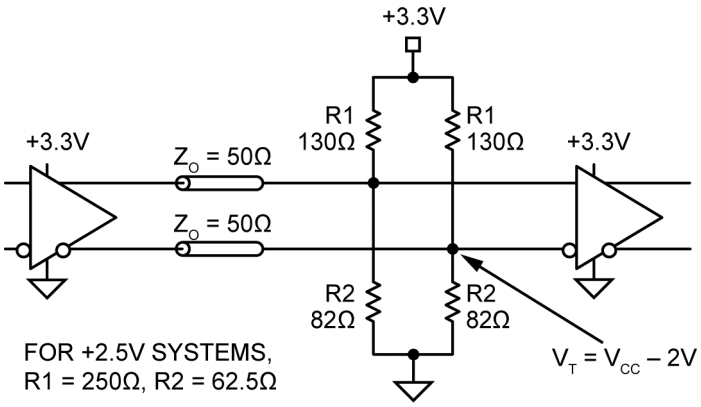
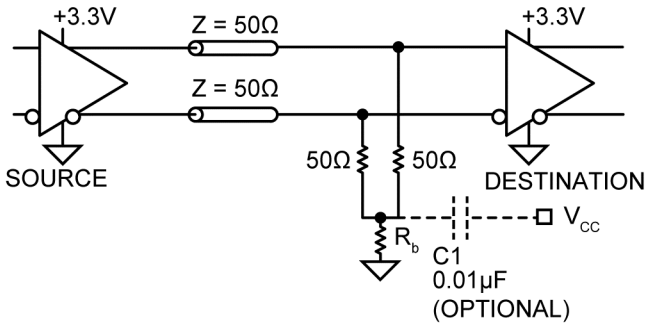
DC-Coupled Signal Interfacing

PECL



Parallel Termination (Thevenin Equivalent)

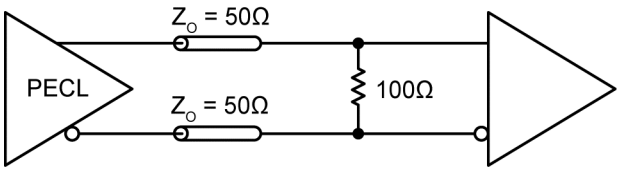


Notes:

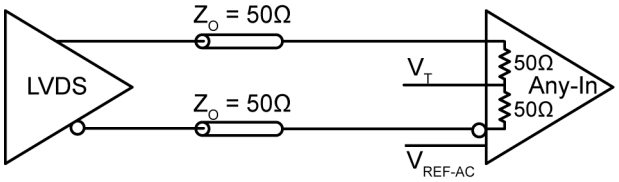
7. Power-saving alternative to Thevenin termination.
8. Place termination resistors as close to destination inputs as possible.
9. R_b resistor set the DC bias voltage, equal to V_T.
10. For 2.5V systems, R_b = 19Ω. For 3.3V systems, R_b = 50Ω.

Parallel Termination (3-Resistor)
"Y-Termination"

LVDS

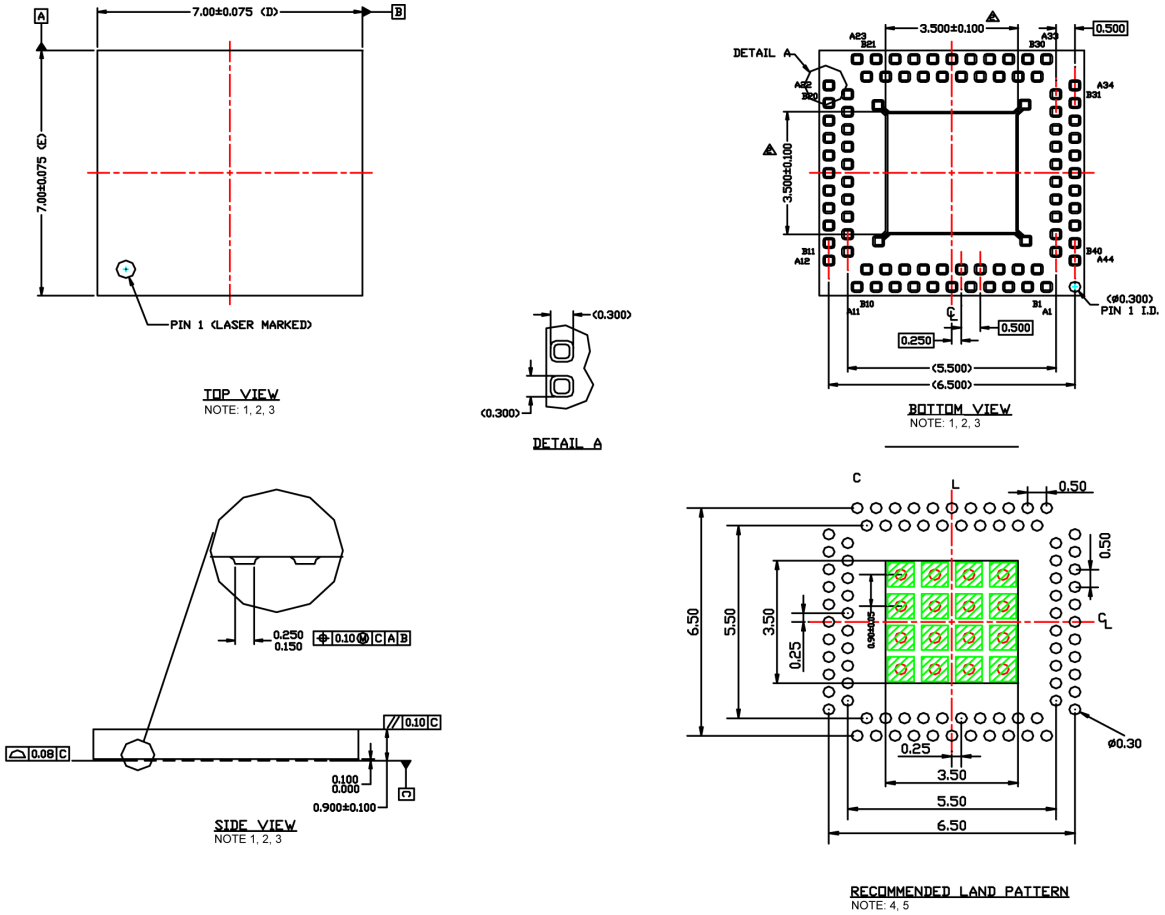


Conventional Method



Micrel Any-In Internal Termination

Package Information[11]



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAXIMUM THERMAL PERFORMANCE. PITCH IS 0.90mm.
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 0.70x0.70 mm, PITCH IS 0.90 mm.

84-Pin QFN 7mm x 7mm

Note:

11. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com