DATA SHEET

80C752/80C732

CMOS SINGLE-CHIP 8 BIT KEYBOARD CONTROLLER

FEATURES

- **4 K BYTES "QUICK-ROM" (80C752 only)**
- **256 BYTES RAM**
- **7 HIGH CURRENT I/O FULLY CUSTOMIZABLE (80C752 only)**
- **THREE 16-BIT TIMERS/COUNTERS**
- **INTERFACE FOR MECHANICAL AND RESISTIVE KEYBOARDS (82C752-M)**
- **INTERFACE FOR CAPACITIVE AND SWITCH CAP KEYBOARDS (80C752-C)**
- **COMPATIBLE WITH 80C52**
- **N-KEY ROLLOVER COMPATIBLE**
- **32 I/O LINES**
- **PROGRAMMABLE SERIAL PORT**
- **6 INTERRUPT SOURCES**
- **KEY PRESSED DETECTION**
- **FULLY STATIC DESIGN**
- **SAJI VI CMOS PROCESS**
- **32 K DATA MEMORY SPACE**
- **64 K PROGRAM MEMORY SPACE**
- **POWER CONTROL MODES**
- **IBMPC SOFTWARE ROUTINE (PCS52, PCK52)**

DESCRIPTION

MHS's 80C752/80C732 is a high performance 8-bit single-chip microcontroller designed for keyboard applications. It is derived from the 80C52/80C32 and bear all its internal features, (except the ROM size, the I/O structure and addressing : refer to MHS's 80C52/80C32 data-sheet).

The 80C752/80C732 allows the user to build powerful, cost effective, and flexible keyboard controllers for mechanical or capacitive keyboards using only this "single chip solution". This is achieved by :

- the on-chip analog interface for capacitive or mechanical matrix,
- the keypressed detection circuit,
- the 7 high current and fully customizable I/O of port 3 which allow the user to configure the circuit to fit a wide range of keyboards arrays and to directly interface with accesories like mouse, card reader, bar code reader, LCD display, etc.

The MHS 80C752/80C732 are manufactured using the SAJI VI CMOS PROCESS and supplied in DIL 40 pins (80C752 only) or PLCC44 pins packages.

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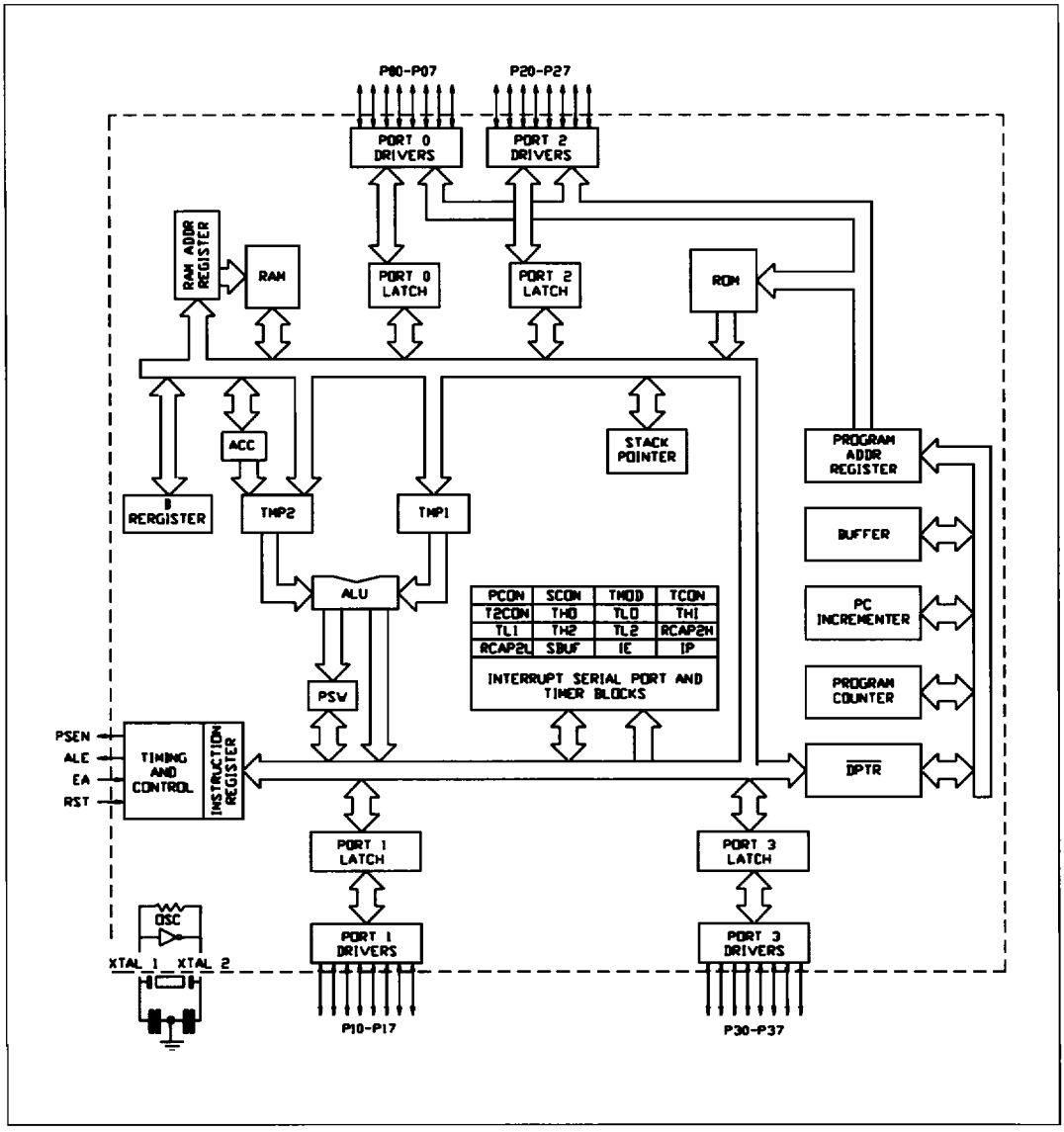
FUNCTIONAL BLOCK DIAGRAM



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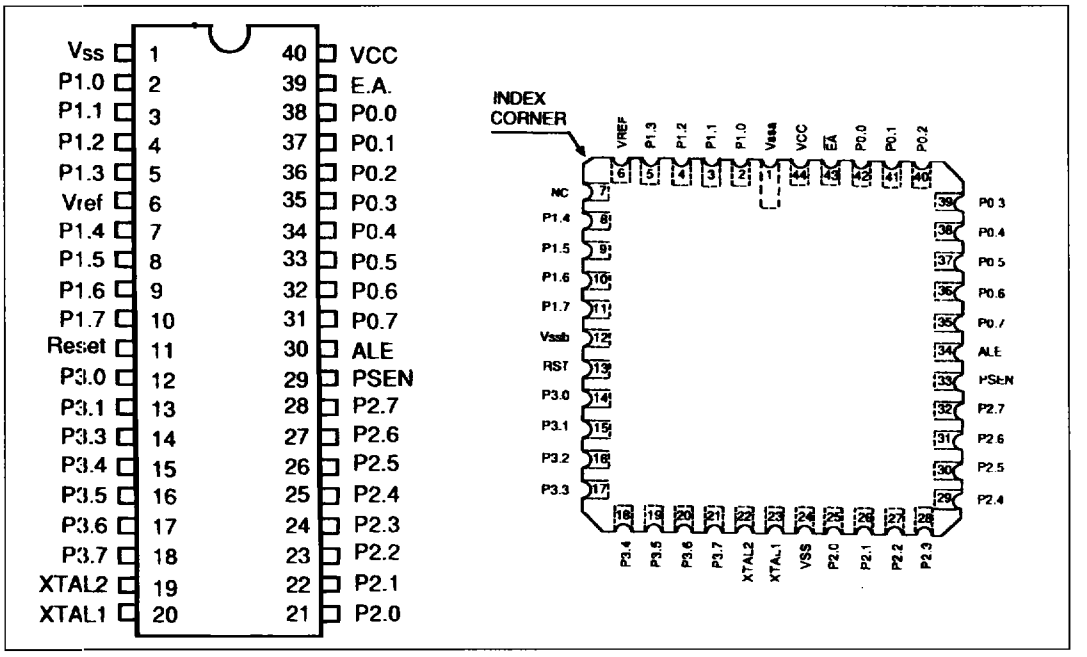
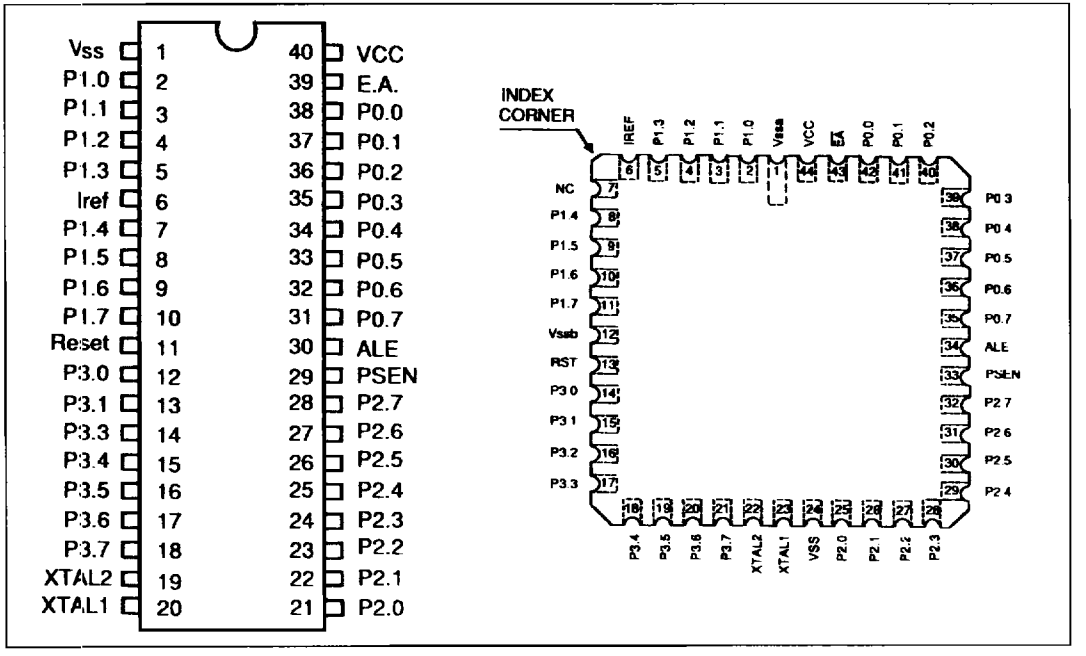
PIN CONFIGURATIONS 80C752-M/80C732-M



PIN CONFIGURATIONS 80C752-C/80C732-C



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PIN DEFINITIONS AND FUNCTIONS

SYMBOL	INPUT (I) OUTPUT (O)	FUNCTION
P3.0-P3.1 P3.2* P3.3-P3.7 P3.6	I/O O I/O I/O	Port3 is an 7 bit quasi-bidirectional port plus a 1-bit output port. For the masked version (80C752), the input level (TTL/CMOS) and the output structure (totempole/open-drain) of all the I/O can be individualy selected by mask during the processing. Port3 also contains the interrupt, timer, serial port, key detection and memory strobe pins : - P3.0 : RxD (serial input port) - P3.1 : TxD (serial output port) - P3.2 : INT0 (key detection), output only - P3.3 : INT1 (external interrupt) - P3.4 : T0 (timer 0 external input) - P3.5 : T1 (timer 1 external input) - P3.6 : WR (external data memory write strobe) - P3.7 : RD (external data memory read strobe)
Xtal1	I	Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.
Xtal2	O	Output of the inverting amplifier that forms the oscillator, and input to the internal clock generator. This pin should be floated when an external oscillator is used.
Vss		Ground (Ov).
P2.0 P2.7	I/O	Port2 is an 8 bit port. For the 80C732. Port2 emits the high-order address during code fetches and external memory accesses. For the 80C752, Port2 is an 8 bit port that can be used as a scanning output port. Port2 is also used for the high order address and the control signals during program verification.
$\overline{PSEN}$	O	The Program Store Enable output is a control signal that enables the external program memory fetch operations. It is activated every six oscillator periods except during to the bus during external data memory accesses. Remains high during internal program execution.
ALE	O	Provides address latch enable output used for latching the adress into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access at which time one ALE pulse is omitted.
$\overline{EA}$	I	When EA is held high, the CPU executes out of internal program memory (unless the program counter exceeds 4096). When EA is held low, the CPU executes only out of external program memory. EA must not be left floating. EA is internally connected to Vcc in the 40 pins DIL package.
P0.0-P0.7	I/O	Port0 is an 8 bit port. In the 80C732, Port0 is only the multiplexed low-order adress and data bus during accesses to external program or data memory. For the 80C752, Port0 is either an 8 bit output port, which can be used for scanning output, or the multiplexed address and data bus. depending on the state of GF0 flag bit (see 80C752' structure). It is also used during code program verification.
Vcc		Power supply (+ 5 V power supply).
Vss, Vssa, Vssb		Reference Ground.
RST	I	A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to Vcc.

PIN DEFINITIONS AND FUNCTIONS (continued)

SYMBOL	INPUT (I) OUTPUT (O)	FUNCTION
P1.0-P1.3 P1.4-P1.7	I/O I	Port1 is an 8 bit port. All bits can be programmed as analog inputs or quasibidirectional I/O, depending on the organization of the matrix. This programmability is possible only for the masked version (80C752). Default configuration is 8 bit analog input (80C732). P1-0 and P1.0, as quasibidirectional I/O can also serve Timer2 as follow : - P1.0 : T2 (external input to timer2) - P1.1 : T2EX (timer2 external trigger input)
Vref	I	Reference voltage for the mechanical interface or reference current for the capacitive interface : Vref set-up the value of the threshold of the resistive switch of the key for P1.0 to P1.7 of the 80C752-M or 80C732-M.
Iref	I	Reference current for the capacitive interface : Iref sets up the value of the threshold for the capacitive. Version : 80C752-C or 80C732-C.

DEVICE DESCRIPTION

INTRODUCTOIN

The 80C752 is a microcontroller designed to be used mainly in keyboards applications. The two different versions are :

- 80C752-M for mechanical keyboards
  - . direct contact
  - . resistive contact
- 80C752-C for capacitive keyboards
  - . switch capacitive
  - . capacitive

They can be provided in :

ROMless version : 80C732 with standard Input/Output port structure (see table 2 page 8),

MASKED ROM versions : 80C752 with customizable Input levels and Output port structure (see table 1 page 7)

80C752 OVERVIEW

This keyboard controller is derived from the MHS80C32 microcontroller and has the same instruction set than the 80C51 processor family. It has been designed for single-chip keyboard or control applications which use a keyboard. The structure of the I/O ports, the interrupt system and the I/O port addressing have been modified for those types of applications.

INPUT/OUTPUT PORTS

ORGANIZATION

The Input/Output ports have been modified and specialized to do different functions related to the keyboard control :

Port0, and Port2 pins are the scanning outputs, Port 1'pins are the return lines of the matrix, Port 3' pins are the high current I/O.

Standard configuration :

The 80C732 do not offers any options on the I/O configuration.

The standard configuration is shown in the table 2 page 8.

Custom configuration :

The 80C752 is also the masked version of the 80C732 which means that the ROM code is implemented on the 80C752 using a special mask. On this mask, MHS offers several options which allow the customer to personalize some I/O of Port1 and Port3 to eliminate the " glue logic " around the 80C752.

The first four I/O of Port1 (P1.0 to P1.3) can be individually selected as a quasi bi-directional port or as an input line from the matrix.

Each of the 7 high current I/O of Port3 can be entirely configured ; this means that the input level can be selected between CMOS or TTL and that the structure of the output stage can be selected between open-drain or quasi bi-directional.

The table 1 shows the characteristics of the I/O port of the 80C752.

STRUCTURE

The structure of each port of the 80C752/80C732 is quite different of the 80C52/80C32's. Let us consider first the I/O structure of the 80C752 (80C752-C and 80C752-M).

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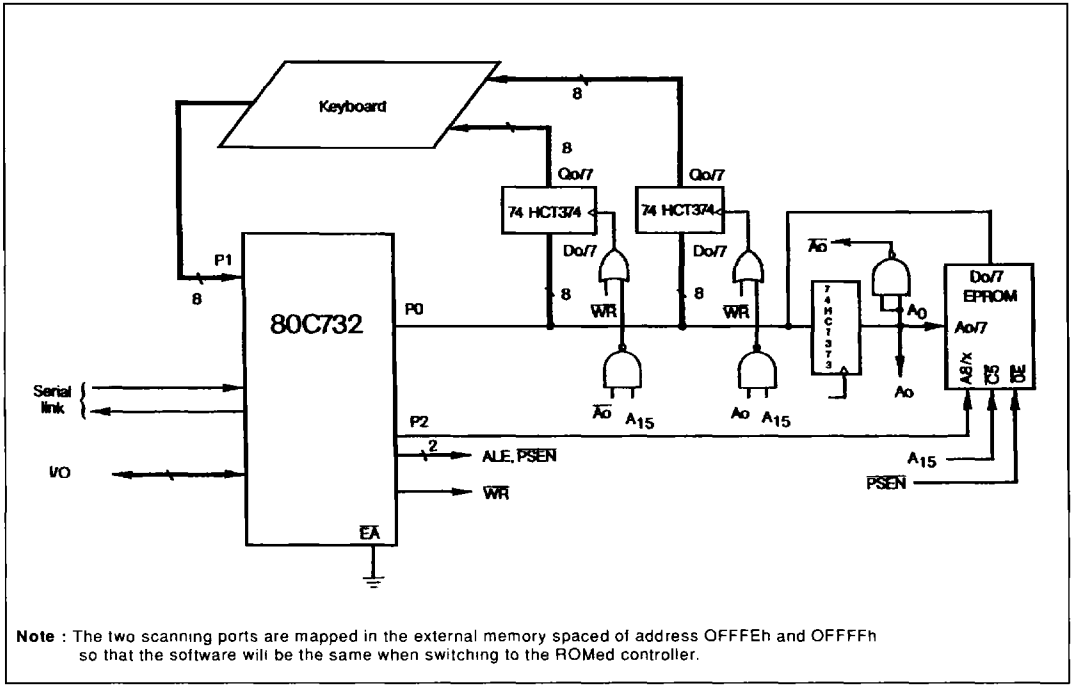
The 80C752 can operate in two modes : the Keyboard controller Mode and the General Purpose Microcontroller Mode. The selection between these two modes in done with GFO, general purpose flag 0 in PCON (*), power control register.

1) The Keyboard Controller Mode : in this mode, GFO is set
   - in ROMLESS version PORT0 is a standard 80C52 Address/Data PORT, and PORT 2 is and Address/SFR Standard PORT.
     When using external ROM, some dedicated glue is necessary to recreat I/O PORT 0 and 2 (see figure 1). To have a complete software compatibility between ROMESS version and ROM version configuration, these 2 new external PORT 0 and 2, must be mapped at Address : FFFFh and FFFEh respectively.
   - in ROM version PORT 0 and PORT 2 are dedicated for the keyboard scanning output lines.
   - When the Controller executes a MOVX instruction :
     - *no control signal si sent to PORT3 (this allows* the use of P3.6 and P3.7 as an I/O PORT)
     - no Address Data are sent on PORT 0 and PORT 2.

2) The General Purpose Microcontroller Mode :
   In this Mode GFO is reset, and all functions are working as a standard 80C52.
   * Note : For more information, see MHS 80C51 user's manual.



Note : The two scanning ports are mapped in the external memory spaced of address OFFFEh and OFFFFh so that the software will be the same when switching to the ROMed controller.

Figure 1 : Keyboard Controller Mode in ROMLESS Version.

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I/O	FUNCTION	STRUCTURE	OPTION
P0.0-P0.7	ADbus or scanning Out	# GF0 = 0 bidirectional ADbus # GF0 = 1 scanning output : output Port	Soft Soft
P1.0-P1.3 P1.4-P1.7	I/O port or scanning In scanning In	Quasi bi-directional I/O with TTL input level Input from resistive or capacitive matrix Input from resistive or capacitive matrix	Mask Mask
P2.0-P2.7	Scanning Out	Scanning output : output port only	
P3.0/RxD	High current I/O	CMOS or TTL input level Open-drain or quasi bi-directional I/O port - IOL = 10 mA @ 0.45 Volt	Mask Mask
P3.1/TxD	High current I/O	CMOS or TTL input level Open-drain or quasi bi-directional I/O port - IOL = 12 mA @ 0.45 Volt	Mask Mask
P3.2/INT0	Key-pressed output signal	Output activated (at 0) when a key is pressed in the scanned line.	
P3.3/INT1	High current I/O	CMOS or TTL input level Open-drain or quasi bi-directional I/O port - IOL = 10 mA @ 0.45 Volt	Mask Mask
P3.4/T0	High current I/O	CMOS or TTL input level Open-drain or quasi bi-directional I/O port - IOL = 3.2 mA @ 0.45 Volt can be used as an 17th scanning Out.	Mask Mask
P3.5/T1	High current I/O	CMOS or TTL input level Open-drain or quasi bi-directional I/O port - IOL = 10 mA @ 0.45 Volt	Mask Mask
P3.6/WR	High current I/O	CMOS or TTL input level Open-drain or quasi bi-directional I/O port - IOL = 10 mA @ 0.45 Volt No WR pulse in single-chip mode	Mask Mask
P3.7/RD	High current I/O	CMOS or TTL input level Open-drain or quasi bi-directional I/O port - IOL = 10 mA @ 0.45 Volt No RD pulse in single-chip mode	Mask Mask

Table 1 : 80C752 (-M or -C version).

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80C732's STRUCTURE

The 80C732 has no on-chip ROM ; as the 80C32, it uses Port0 and Port2 to fetch opcodes and to access external data memory (RAM or I/O port mapped in the external memory space). But, as the chip has no masked-ROM, no options are possible on Port1 and Port2.

Port1 operation is the same as 80C752's. Port3' I/O lines operate as Port3 of 80C32.

The table 2 shows the characteristics of the I/O port of the 80C732.

I/O	FUNCTION	STRUCTURE	OPTION
P0.0-P0.7	ADbus	Bidirectional ADbus	
P1.0-P1.3 P1.4-P1.7	scanning In	Input from resistive or capacitive matrix	
P2.0-P2.7	Add bus	A8-A15 adress bus	
P3.0/RxD	High current I/O	TTL input level quasi bi-directional I/O port - IOL = 10 mA @ 0.45 Volt	
P3.1/TxD	High current I/O	TTL input level quasi bi-directional I/O port - IOL = 12 mA @ 0.45 Volt	
P3.2/INT0	Key-pressed output signal	Output activated (at 0) when a key is pressed in the scanned line.	
P3.3/INT1	High current I/O	TTL input level quasi bi-directional I/O port - IOL = 10 mA @ 0.45 Volt	
P3.4/T0	High current I/O	TTL input level quasi bi-directional I/O port - IOL = 3.2 mA @ 0.45 Volt	
P3.5/T1	High current I/O	TTL input level quasi bi-directional I/O port - IOL = 10 mA @ 0.45 Volt	
P3.6/WR	High current I/O	TTL input level quasi bi-directional I/O port - IOL = 10 mA @ 0.45 Volt WR pulse during each WRITE instruction	
P3.7/RD	High current I/O	TTL input level quasi bi-directional I/O port - IOL = 10 mA @ 0.45 Volt RD pulse during each READ instruction	

Table 2 : 80C752 (-M or -C version).

MECHANICAL KEYBOARDS

80C752-M/80C732-M

The operation of the mechanical keyboards is based on the use of contacting switches. These switches can be elastomer-dome, mechanical, membrane and snap-dome ; they rely on basically the same hardware and software techniques.

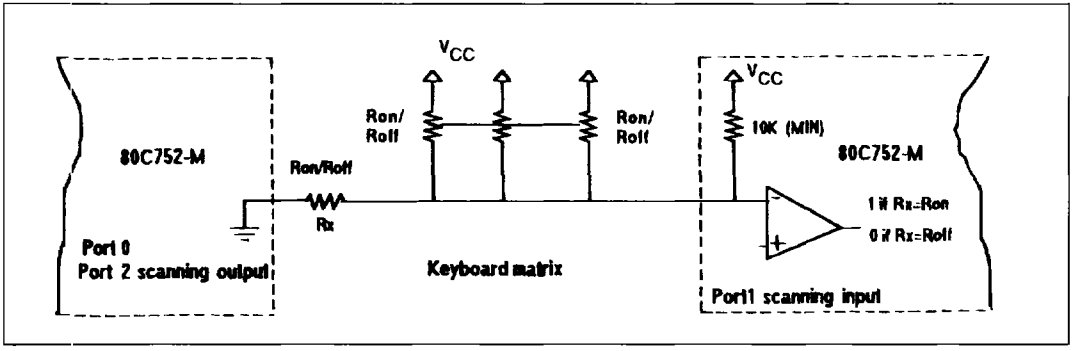
The 80C752-M and the 80C732-M are designed to directly interface these types of mechanical keyboards, whatever the types of the contacting switches.

THE ON-CHIP ANALOG INTERFACE

PRINCIPLE

The measurement is based on a voltage comparison between the selected threshold voltage and the voltage coming from the matrix :

The output voltage from the matrix may depend on the state of the non-scanned keys. The user must take this into account when selecting the threshold voltage.



SWITCH ROLLOVER TECHNIQUES

Depending on the keyboard's technology and its application, designers can use several rollover or validation schemes (defined as the number of keys that the keyboard circuit can process as closed in the correct sequence at the same time). The most common types of roll-over in use today are N-key lockout, two-key rollover, three-key rollover, and N-key rollover.

The 80C752-M and the 80C732-M allow all these different schemes. The number of roll-over is determined by the value of the ON-resistor and the presence of a blocking diode.

- without blocking diode.

If the ON-resistor is less than 2 kΩ, 16 keys can be pressed at the same time on a same column (16 Key Rollover). To avoid risk of phantom key only one column must be activated at the same time.

- with blocking diode.

Adding a blocking diode at each switch location eliminates phantom key closures and provides current protection with low ON-resistor switches. This technique also enables the use of the N-key rollover scheme, whatever the characteristics of the switch. The blocking diode is mandatory for keyboards with mechanical switches.

SCANNING TECHNIQUE

The scanning consists of resetting one of the drive lignes high and reading the state of the voltage comparators. Only one output at a given time can be active (low level) ; this means that between two different active states.

THRESHOLD SETTING

To accomodate different types of contacting switches, the user can adjust the threshold voltage of the 80C752-M/80C732-M by adjusting the input voltage on Vref pin.

KEY PRESSED DETECTION

The 80C752-M and the 80C732-M provide hardware detection of a pressed key. This information (state of the P3.2 pin) can be used as a flag (state read by software) or as an interrupt source, if INT0 is enabled. The state of P3.2 is updated after the start of every new scanning ; this is the reason why INT0 must be edge triggerred (bit IT0 in TCON must be set).

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DEVELOPMENT

The 80C752-M has been designed so that any program developed for the 80C732-M, with the two output scanning ports mapped at external memory addresses OFFFEh and OFFFFh, can be exactly the same for the 80C752-M. This is the reason why Port0 and Port2 of the 80C752 are mapped in the SFR space and in the external memory space.

EMULATION

For the software and/or hardware debugging, any 80C52 emulator can be used to emulate the 80C752-M, but the user has to add some external "glue logic" around the emulator probe to build the mechanical interface of the 80C752-M and the drivers integrated in Port3 pins. Hereafter is the schematic of the mechanical interface which must be added between the 8 outputs from the matrix and the 8 pins of Port1 of the emulator :

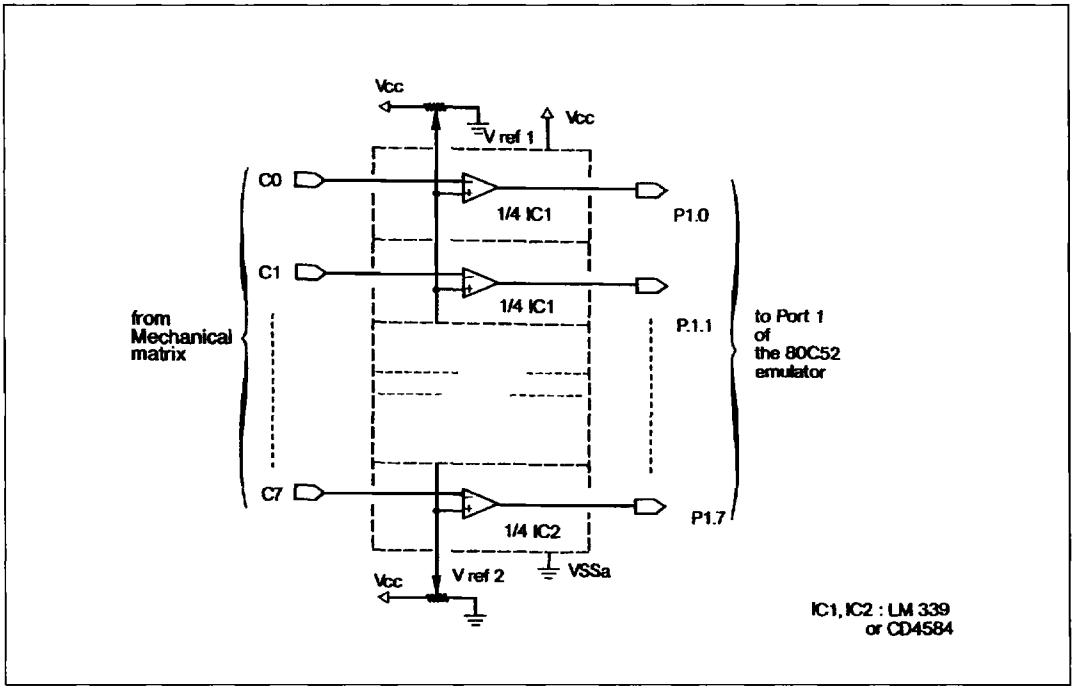

Figure 2 : Mechanical Interface Schematic.

80C732-M EMULATION

For 80C732-M emulation, the user has to provide one or two external ports, to be mapped in the external memory space for the scanning output port. It is recommended to map these ports at the addressed OFFFEh and OFFFFh because when going from ROMless to ROMed version, the software will remain the same. This is the complete emulation schematic :

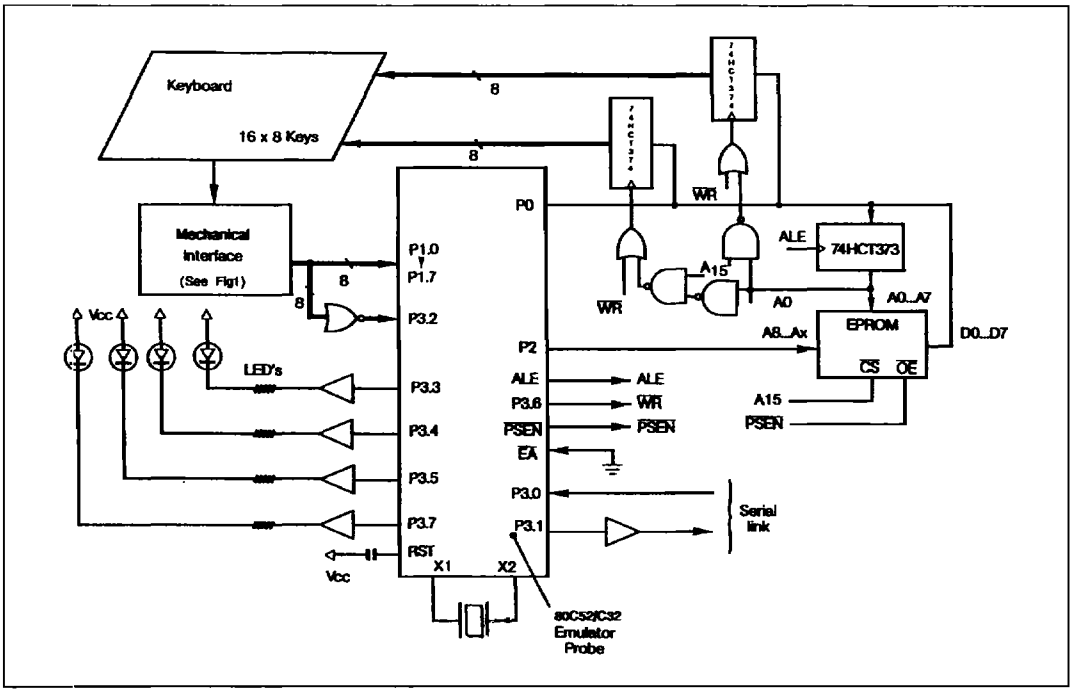

Figure 3 : 80C732-M Emulation Schematic.

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80C752-M EMULATION

For 80C752-M emulation, it is not useful to build the external output ports (and it is not recommended) because the SFR and bit addressing of the scanning ports (P0 and P2) is preferable when using the external memory addressing and also because this allows the use of P3.6 as an I/O.

The below figure shows the complete emulation schematic :

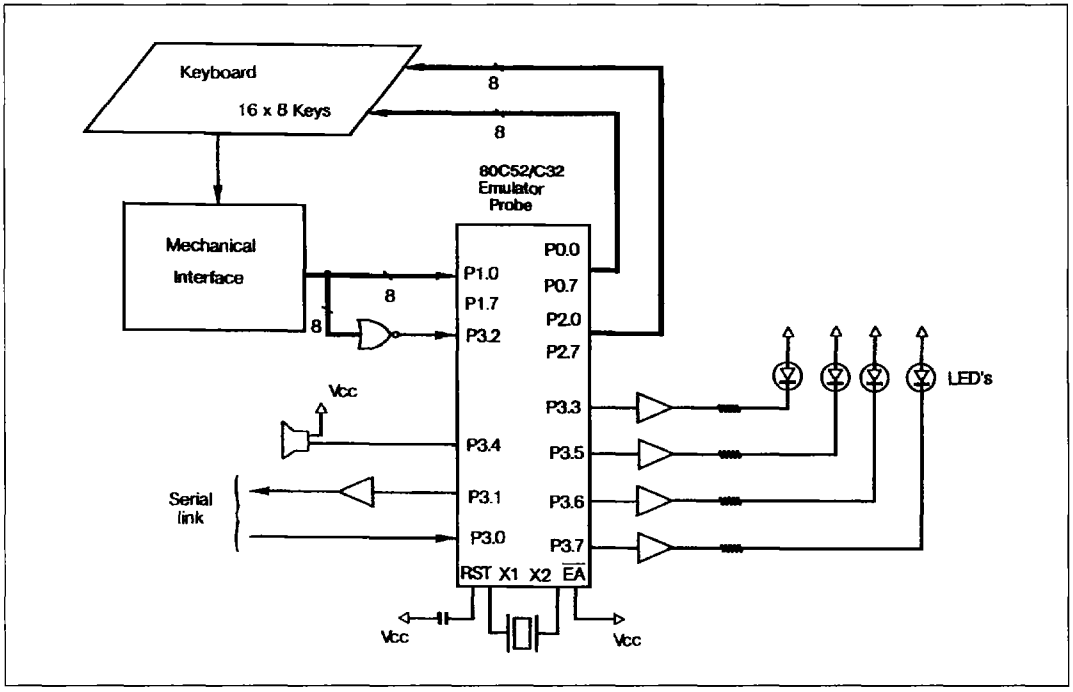

Figure 4 : 80C752-M Emulation Schematic.

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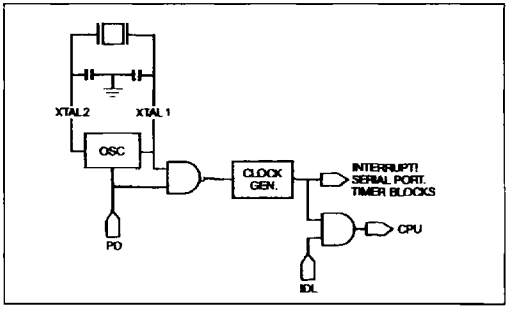
IDLE AND POWER-DOWN OPERATION

As shown in the below figure, the idle and power-down modes are the same than with 80C51 (see MHS 80C51 user's manual). As illustrated, Power-down operation stops the oscillator and idle mode operation allows the interrupt, serial port, and timer blocks to continue to function while the clock to the CPU is gated off.

During power-down, the analog interface is powered-off to minimize circuit power consumption. The only way to escape from power-down mode is to reset the CPU.

During idle, if any key is pressed, P3.2 will fall down and, if INT0 is enabled, the CPU will escape from idle mode.



CAPACITIVE KEYBOARDS

80C752-C/80C732-C

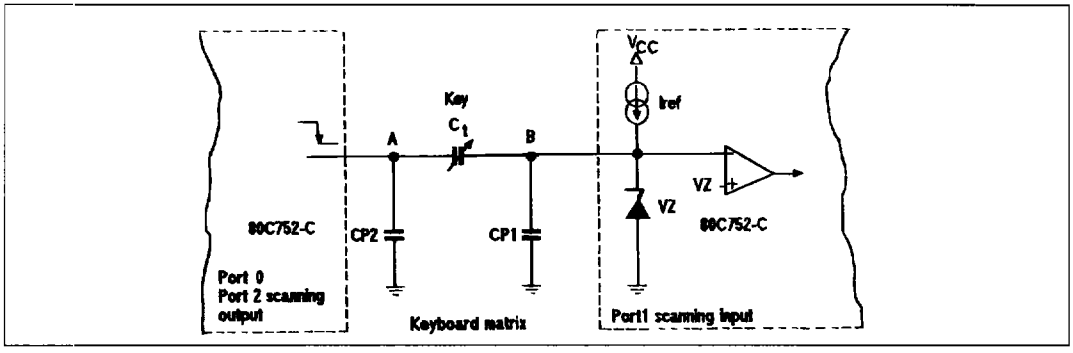
There are 2 types of capacitive keys : the full capacitive type and the switch-capacitor type.

The 80C752-C and the 80C732-C are designed to directly interface these two types of capacitive keyboards, independently of the state of each capacitive key.

THE ON-CHIP ANALOG INTERFACE

PRINCIPLE

The 80C752-C and the 80C732-C allow the N-Key rollever technique ; this means that they can detect a key independently of the state of the other keys and of the technology of the matrix (flexprint...).
The measurement is based on a constant current charge of the capacitor of the key :



At the falling edge of the scanning output, the voltage at node B goes down below the regulation voltage of the " zener ".

The voltage decreasing virtually disconnect the regulator and all the current from the current generator goes to the capacitors.

So, the capacitors are charged with a constant current. At the end of the process, the voltage value is the same as before the falling edge ; this means that Cp1 has no influence on the time to charge Ct the capacitor of the key :

$$t = Va \times Ct/Iref \Rightarrow Ct = (t \times Iref)/Va$$

The voltage driven technique on the node A eliminates the influence of Cp2.

Cp1 and Cp2 have no influence on Ct measurement ; this allows the 80C752-C and the 80C732-C to be used in design with N-key rollover technique. They can fit with a wide range of capacitive matrices because the on-chip hardware allows the selection of the capacitor threshold value.

SCANNING TECHNIQUE

The scanning must be done with a rolling zero on the scanning outputs (the other outputs remain high). Only one output at a given time can be active (low level) ; this means that between two different active states all scanning outputs must be desactivated.

THRESHOLD SETTING

The formula which determines the operation of the capacitive interface is :

Ct = (t x Iref)/Va

- Ct, is the capacitor threshold value,
- Va, which is the value of the voltage variation on the scanning output, Vcc - 0.5 V,
- t, determines the moment when the output of the comparator is strobed (0 if the capacitor is recharged, 1 if not recharged).

Iref, which is the value of the constant current driving Ct. It can be adjusted by an external resistor. This allows the 80C752-C and the 80C732-C to operate with different types of capacitive matrixes. Iref can be fixed with only one resistor ; the formula to select Iref is Iref = (Vcc – 1.5 V)/R, where R is the value of the external resistor.

KEY PRESSED DETECTION

The 80C752-C and the 80C732-C provide an internal hardware detection of pressed key. This signal is output on P3.2 and internally connected to INT0. This information (state of P3.2) can be used as a flag (state read by software) or as an interrupt source, if INT0 is enabled. This is the reason why INT0 must be edge triggered (bit IT0 in TCON must be set).

DEVELOPMENT

The 80C752-C has been designed so that any program developed for the ROMless, with the two output scanning ports mapped at external memory address 0FFFEH and 0FFFFh, can be exactly the same for the 80C752-C. This is the reason why Port0 and Port2 of the 80C752 are mapped in the SFR space and in the external memory space.

EMULATION

For software and/or hardware debugging, any 80C52 emulator can be used to emulate the 80C752-C, but the user has to add some external " glue logic " around the emulator probe to build the capacitive interface of the 80C752-C and the drivers integrated in port3 pins. Hereafter is the schematic diagram of the capacitive interface which mut be added between the 8 inputs from the matrix and the 8 pins of Port1 of the emulator :

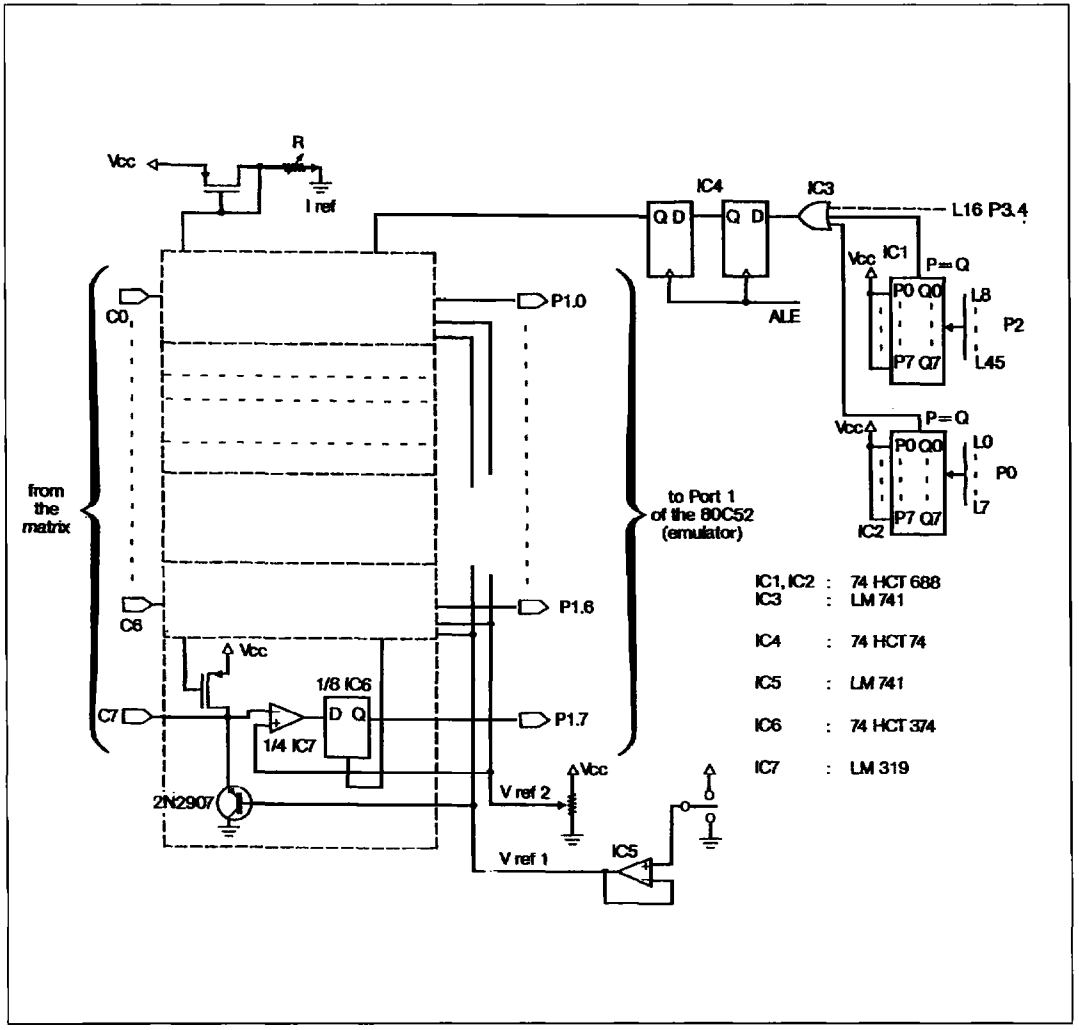


Figure 5 : Capacitive Interface Schematic.

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80C732-C EMULATION

For 80C732-C emulation, the user has to provide one or two external ports, to be mapped in the external memory space for the scanning output port. It is recommended to map these ports at the addresses 0FFFEh and 0FFFFh because when going from ROMless to ROMed version, the software will remain the same. Here is the complete emulation schematic :

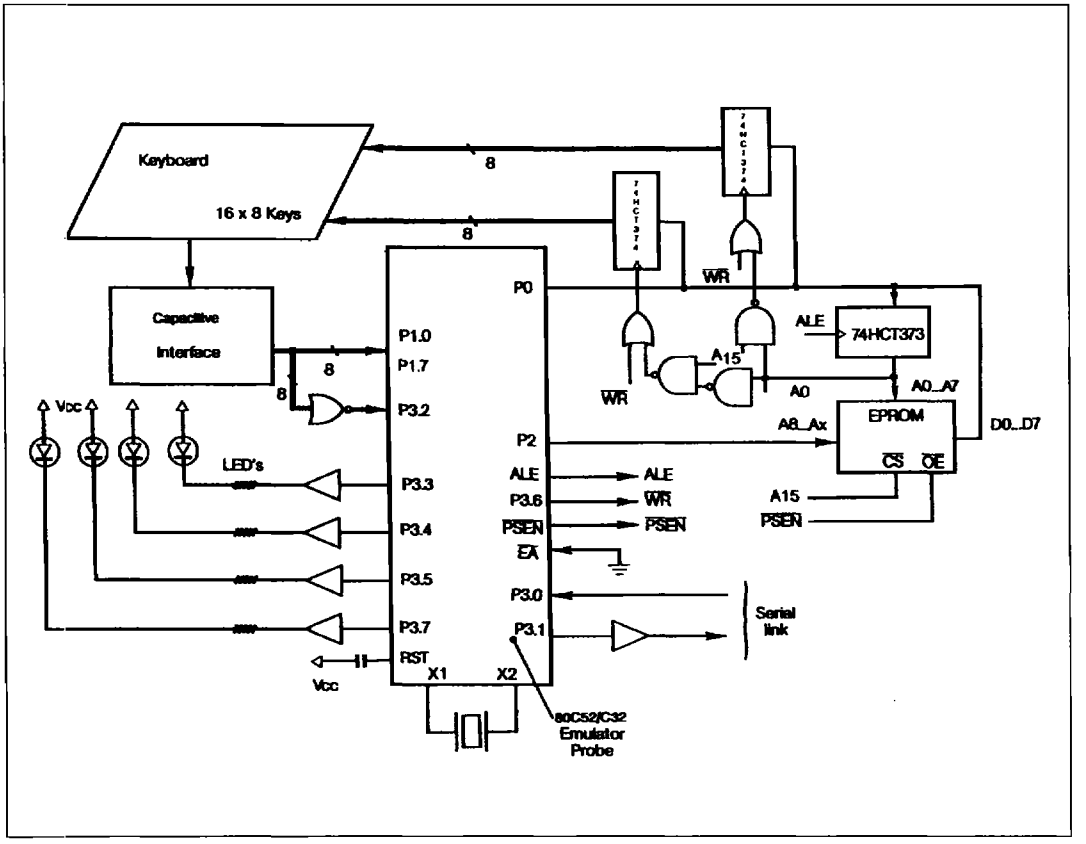

Figure 6 : 80C732-C Emulation Schematic.

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80C752-C EMULATION

For 80C752-C emulation, there is no need to build the external output ports. However it is not recommended since the SFR and bit addressing of the scanning ports (P0 and P2) is better than the external memory addressing and also because this allows the use of P3.6 (WR) as an I/O. The below figure shows the complete emulation schematic :

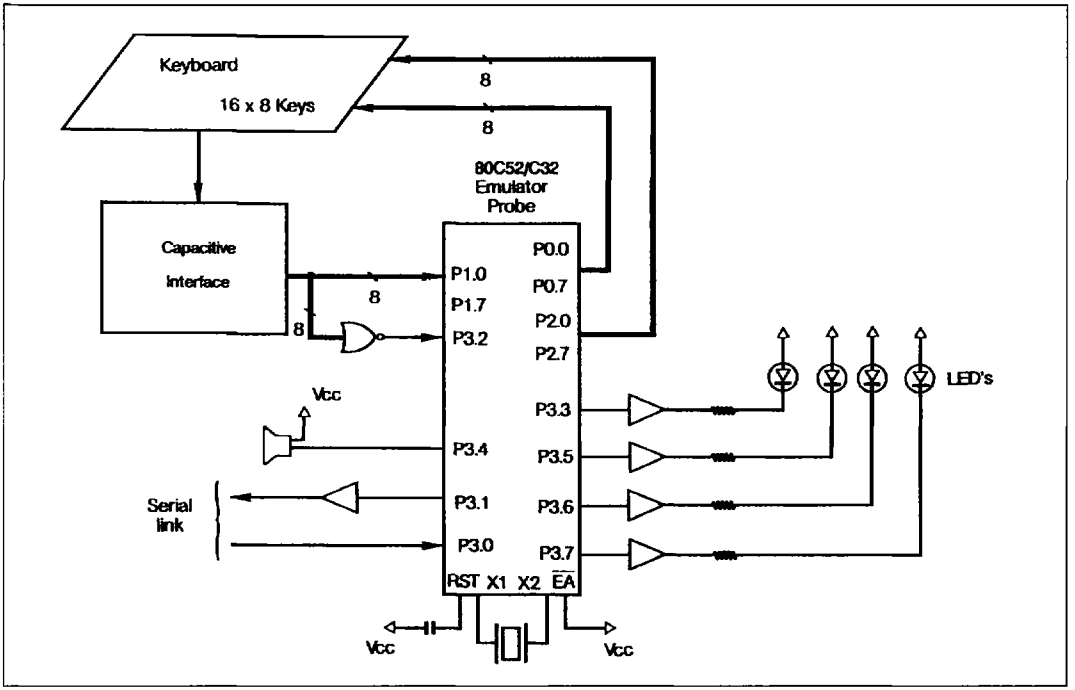

Figure 7 : 80C752-C Emulation Schematic.

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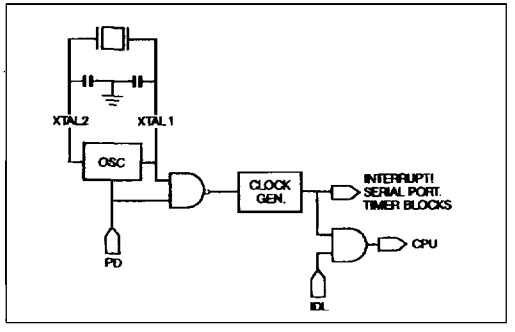
IDLE AND POWER-DOWN OPERATION

As shown in the figure below, the idle and power-down modes are the same as for 80C51 (see MHS 80C51 user's manual). As illustrated, Power-down operation stops the oscillator and Idle mode operation allows the interrupt, serial port, and timer blocks to continue to function while the clock to the CPU is gated off.

During power-down the capacitive interface is powered-off to minimize circuit power consumption. P3.2 remains in the same state until a new scanning value is sent ; if any key is pressed during Idle or Power-down, it will not change the state of P3.2 and the circuit will stay in the same mode.



SOFTWARE CONSIDERATIONS

The 80C752 has been built to simplify the design of keyboards and thus allowing the user to concentrate on the real problems such as keys organisation, type of matrix, design of the keys and the box of the keyboard...

As a result, only one software has to be written by the user. The same software can be used for :

- ROMless devices,
- ROMed devices,
- mechanical or resistive matrixes,
- capacitive matrixes.

Moreover MHS can also provide a masked version for IBM-PC (*) compatible keyboards, the PCK52, and the assembly source program of the PCK52, named PCS52.

1. MECHANICAL OR RESISTIVE MATRIXES. The scanning is based on the static level of each input : at any moment, the state of P3.2 and the data read in SFR Port1 indicate the real state of the scanned-keys.
2. CAPACITIVE MATRIXES. The scanning is based on the dynaic level of each input of the matrix : the capacitor measurement until (integrated in Port1) is retriggered at each new scan generation (i.e. after the falling edge of a scan line) and for some microsecond only.

So, the state of P3.2 and the data read in SFR Port1 do not indicate at every moment the state of the scanned-keys.

Design considerations :

The data in Port1, which should be normally strobed 3 µs after a new scan generation, are not strobed on this design.

The consequences are :

- P3.2 must not be used for software tests and for interrupt generation.
- The 3 µs delay must be done by software,
- During the active time of the scanning, all interrupts must be masked to ensure that the 3 µs software delay will be always the same.
- The data in SFR Port1 must be read immediatly after the 3 µs delay.

3. EXAMPLE : Hereafter is an example of a scanning routine which can be used for capacitive or resistive matrixes and for ROMed or ROMless devices.

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(*) IBM is a trademark of International Business Machine Corporation.

```
SCANNING_ROUTINE :                      ; ASSUME (R7, R6) CONTAINS THE
                                        ; SCANNING VALUE
            SETB    C
            MOV     A, R6
            RLC     A                   ; ROLLING 0 THROUGH (R7, R6)
            MOV     R6, A
            MOV     PSW.5, C            ; STORE CARRY FLAG IN GF1
            CJNE    A, #0FFH, SCAN_LOW
            MOV     C, PSW.5
            MOV     A, R7
            RLC     A
            MOV     R7, A
            CJNE    A, #0FFH, SCAN_HIGH
            MOV     R6, #0FEH
SCAN_LOW :
            MOV     A, R6
            MOV     DPTR, #0FFFFH
            CLR     IE.7                ; DISABLE ALL IT
            MOVX    @DPTR, A            ; SCAN : FALLING EDGE ON PO.X
            NOP
            NOP
            MOV     A, P1               ; 3 µS DELAY BETWEEN SCAN AND SENSE
            JMP     TEST_DETECT
SCAN_HIGH :
            MOV     A, R7
            MOV     DPTR, #0FFFEH
            CLR     IE.7                ; DISABLE ALL IT
            MOVX    @DPTR, A            ; SCAN : FALLING EDGE ON P2.X
            NOP
            NOP
            MOV     A, P1               ; 3 µS DELAY BETWEEN SCAN AND SENSE
TEST_DETECT :
            SETB    IE.7                ; RE-ENABLES ALL IT
            CPL     A
            JZ      NO_KEY
KEY-DETECTED :                          ; TEST FOR PUSHED KEYS
NO_KEY :                                ; TEST FOR RELEASED KEYS
            RET
```

PCK52

The PCK52 has been specially designed for IBM-PC keyboards. It is supplied in 2 versions :

- PCK52-M for mechanical or resistive matrix,
- PCK52-C for capacitive matrix.

It can be used in PC-XT or PC-AT applications, depending of the state of switch 1 (SW1).
The Key-mapping is shown in table 3. The number given in this table designates the keybutton position, conforming to the IBM nomenclature for keyboards.

	P1.0	P1.1	P1.2	P1.3	P1.4	P1.5	P1.6	P1.7
P0.0	0	0	0	0	0	0	0	0
P0.1	53	60	52	58	61	62	56	54
P0.2	47	46	45	44	51	50	49	48
P0.3	33	32	31	30	37	36	35	34
P0.4	19	18	17	16	23	22	21	20
P0.5	4	3	2	1	8	7	6	5
P0.6	0	0	0	SW1	0	0	0	0
P0.7	114	113	112	110	118	117	116	115
P2.0	0	0	0	0	0	0	0	0
P2.1	91	96	101	103	0	42	93	98
P2.2	41	40	39	38	83	64	57	0
P2.3	108	106	105	104	84	79	89	99
P2.4	90	95	100	102	86	85	92	97
P2.5	27	26	25	24	81	76	43	28
P2.6	12	11	10	9	80	75	15	13
P2.7	122	121	120	119	126	125	124	123

SW1 : ON : PC-XT, OFF : PC-AT3.

Table 3 : Key Mapping of PCK52.

PCK52 MASK OPTIONS :

Hereunder are described the Mask options of the actual version of PCK52 for Mechanical Keyboard : 80C752M.290.

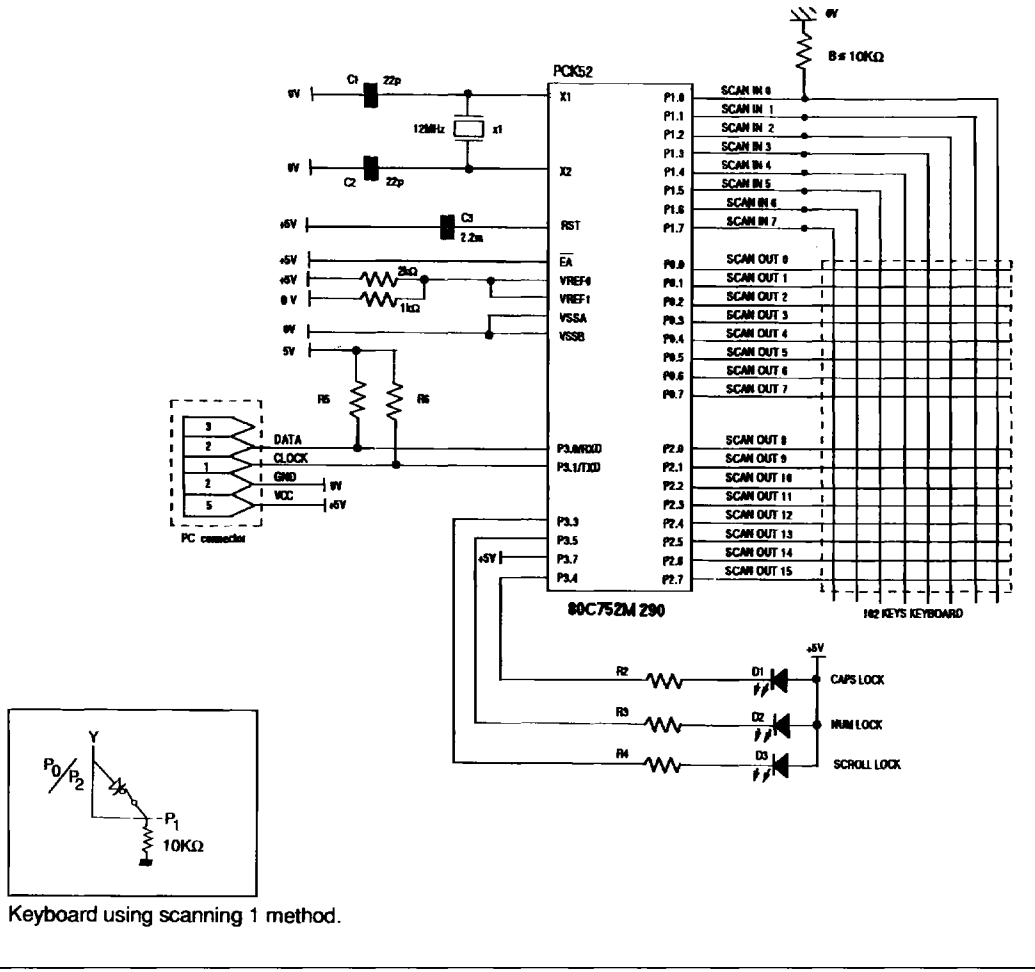
80C752-M 290 MASK OPTIONS

KEYBOARD MATRIX								
MECHANICAL				or	CAPACITIVE			
PORT 1 SELECTIONS	P1.0	P1.1	P1.2	P1.3	P1.4	P1.5	P1.6	P1.7
I/O port with TTL input	YES	YES	YES	YES	YES	YES	YES	YES

	INPUT SELECTION		OUTPUT SELECTION		
PORT 3 OPTIONS	TTL (51 type)	CMOS	C51 TYPE (*)	OPEN DRAIN	
P3.0/RXD	YES			YES	10 mA (max)
P3.1/TXD	YES			YES	12 mA (max)
P3.3/INT1	YES			YES	10 mA (max)
P3.4/T0		YES	YES		3.2 mA (max)
P3.5/T1		YES	YES		10 mA (max)
P3.6/WR		YES	YES		10 mA (max)
P3.7/RD		YES	YES		10 mA (max)

(*) : Quasi bi-directionnal high current @ 0.45 V.

The Hardware environment must be following :



Keyboard using scanning 1 method.

PCS52

The PSC52 is the assembly source of the PCK52 program.

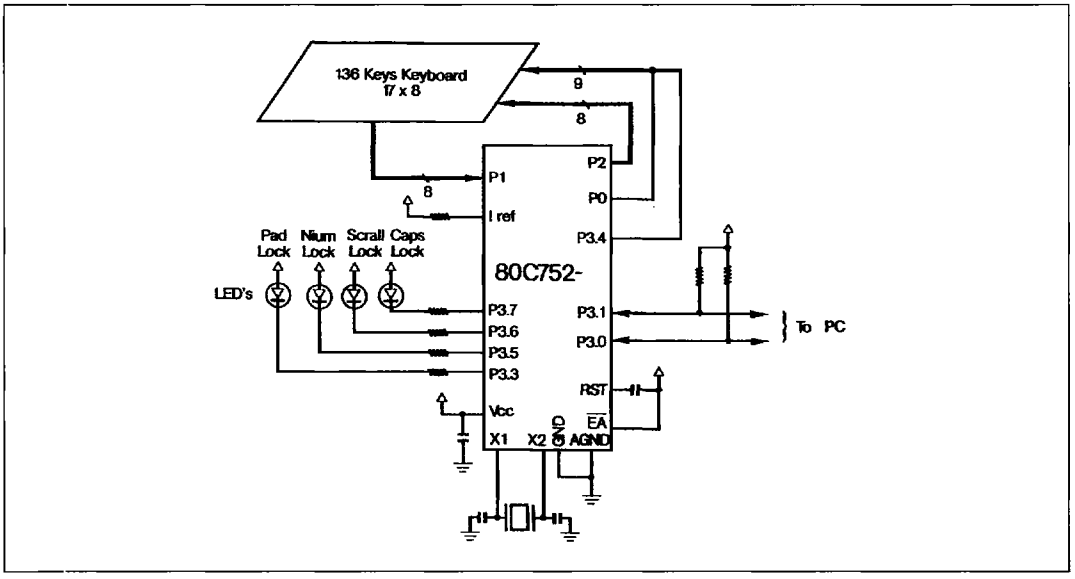
This software, fully documented, allows to change the main characteristics of a keyboard by modifing some parameters in the assembly is the source program :

- the key-mapping
- the 3 internal timings :
  - the debounce time,
  - the scanning rate,
  - the auto-repeat rate.
- the default type of the keys :
  - make/break,
  - typematic.
- the type of the scanning :
  - positive or negative.

This source file, in 8051 assembly code is provided in 1 floppy (5 or 3 inches) for MS-DOS compatible PC.

APPLICATION EXAMPLES

1. Keyboard controller for Personal Computer :



In this configuration, the 80C752-C can control keyboards with up to 136 keys.
The following options must be selected in order to drive the capacitive matrix and to comply with the DC specifications of the serial link with the PC :
Input levels :
P3.0 and P3.1 : TTL (0.8 V ; 2.4 V), selected by mask option.

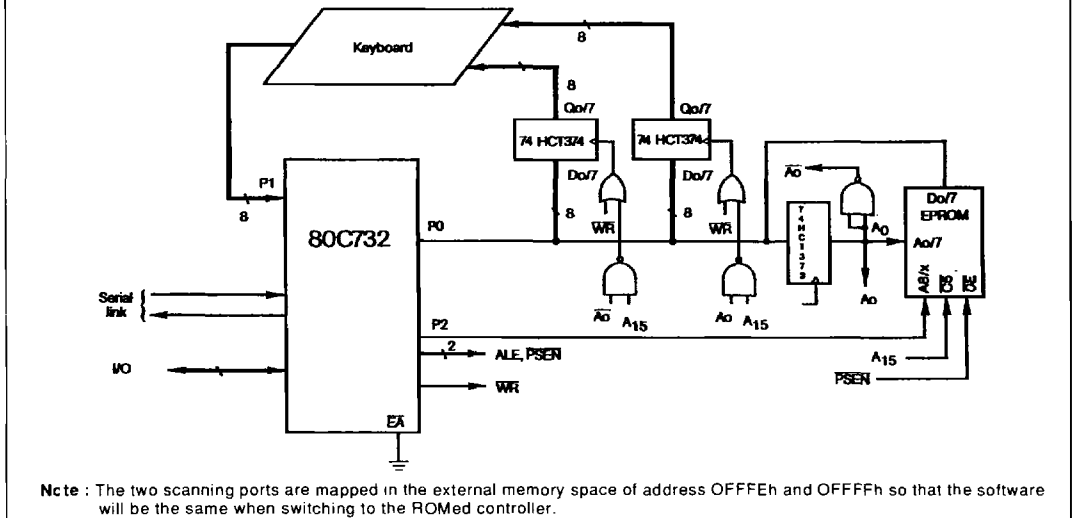
2. Keyboard controller with external EPROM :

Output structures :

P3.0, P3.1 : open drain, selected by mask option,

P3.4 : quasi bi-directional port, selected by mask option,

P3.3, P3.5, P3.7 : open drain, selected by mask option.



Note : The two scanning ports are mapped in the external memory space of address OFFFEh and OFFFFh so that the software will be the same when switching to the ROMed controller.

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ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias :
Commercial ..... – 0°C to 70°C
Storage Temperature ..... – 65°C to + 150°C
Voltage on V_{CC} to V_{SS} ..... – 0.5 to V_{CC} + 7 V
Voltage on any pin to V_{SS} ..... – 0.5 V to V_{CC} + 0.5 V
Power Dissipation ..... 200 mW

* NOTICE : Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC CHARACTERISTICS

TA = 0°C to + 70°C ; V_{SS} = 0 V ; V_{CC} = 5 V ± 10 %

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	– 0.5	0.2 V_{CC} – 0.1	V	
VIH	Input High Voltage (Except XTAL1 and RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
VIH1	Input High Voltage (RST and XTAL1)	0.7 V_{CC}	V_{CC} + 0.5	V	
VOL	Output Low Voltage (Ports 1, 2, 3)		0.45	V	IOL = 1.6 mA (note 2)
VOL1	Output Low Voltage Port 0, ALE, $\overline{PSEN}$, P3.4, Port 2		0.45	V	IOL = 3.2 mA (note 2)
VOL2	Output Low Voltage P3.3, P3.5, P3.6, P3.7		0.45	V	IOL = 10 mA (note 2)
VOL3	Output Low Voltage P3.0, P3.1		0.45	V	IOL = 12 mA (note 2)
VOH	Output High Voltage Ports 1, 2, 3	0.9 V_{CC}		V	IOH = – 10 µA
		0.75 V_{CC}		V	IOH = – 25 µA
		2.4		V	IOH = – 60 µA V_{CC} = 5 V ± 10 %
VOH1	Output High Voltage (Port 0 in External Bus Mode, ALE, $\overline{PSEN}$)	0.9 V_{CC}		V	IOH = – 40 µA
		0.75 V_{CC}		V	IOH = 150 µA
		2.4		V	IOH = – 400 µA V_{CC} = 5 V ± 10 %
IIL	Logical 0 Input Current Ports 1, 2, 3		– 50	µA	Vin = 0.45 V
ILI	Input Leakage Current (Port 0, $\overline{EA}$)		± 10	µA	0.45 < Vin < V_{CC}
ITL	Logical 1 to 0 Transition Current (Ports 1, 2, 3)		– 650	µA	Vin = 2.0 V
IPD	Power Supply Current (Power Down Mode)		100	µA	V_{CC} = 2.0 V to 5.5 V (note 1)
RRST	RST Pulldown Resistor	50	150	kΩ	
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz TA = 25°C
VREF	Reference Voltage	1.0	V_{CC} – 1.0	V	80C752-M/80C732-M
RVREF	Source Impedance of VREF	1.0		MΩ	80C752-M/80C732-M
IRef	Current reference for current minors	10	500	µA	80C752-C/80C732-C

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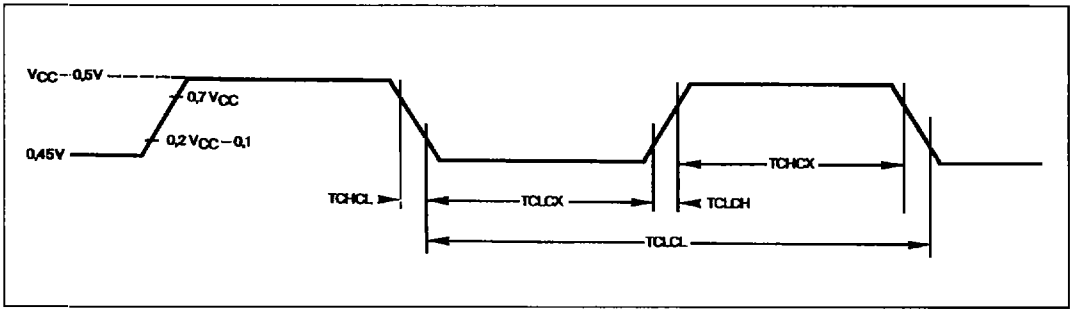

Figure : Clock Signal Waveform for ICC Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

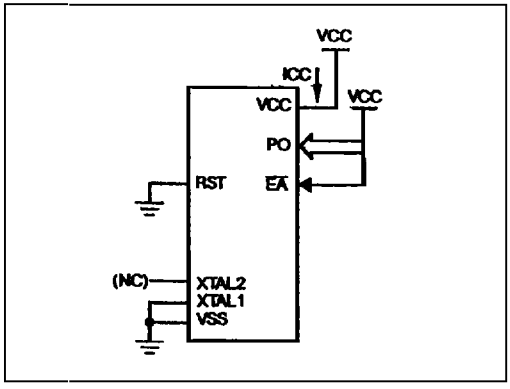

Figure : ICC Test Condition, Power Down Mode.
All other pins are Disconnected.

Note : 1. ICC is measured with all output pins disconnected ; XTAL1 driven with TCLCH, TCHCL = 5 ns, VIL = VS + 5 V, VIH = VCC − .5 V ; XTAL2 N.C. ; EA = RST = Port 0 = VCC. ICC would be slightly higher if a crystal oscillator used.

Idle ICC is measured with all output pins disconnected ; XTAL1 driven with TCLCH, TCHCL = 5 ns, VIL = VSS + .5 V, VIH = VCC − .5 V ; XTAL2 N.C. ; Port 0 = VCC ; EA = RST = VSS.

Power down ICC is measured with all output pins disconnected ; EA = PORT 0 = VCC ; XTAL2 N.C. ; RST = VSS.

Note : 2. Capacitance loading on Ports 0 and 2 may cause spurious noise, pulses to be superimposed on the VOLS of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transistions during bus operations. In the worst cases (capacitive loading 100 pF), the noise pulse on the ALE line may exceed 0.45 V with maxi VOL peak 0.6 V. A Schmitt Trigger use is not necessary.

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EXTERNAL CLOCK DRIVE CHARACTERISTICS (XTAL1)

SYMBOL	PARAMETER	VARIABLE CLOCK FREQ = 0 to 12 MHz		UNIT
		MIN.	MAX.	
1/TCLCL	Oscillator Frequency	83		ns
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

AC PARAMETERS

TA + 0°C to 70°C ; VSS = 0 V ; VCC = 5 V ± 10 % (commercial)
(load capacitance for Port 0, ALE ; and $\overline{PSEN}$ = 100 pf ; load capacitance for all other outputs = 80 pf).

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

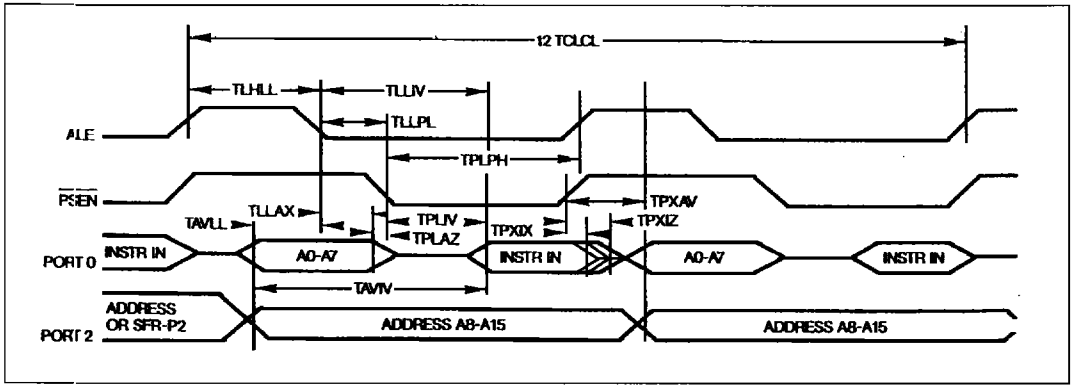
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
TLHLL	ALE Pulse Width	2TCLCL-40		ns
TAVLL	Address Valid to ALE	TCLCL-55		ns
TLLAX	Address Hold After ALE	TCLCL-35		ns
TLLIV	ALE to Valid Instr in		4TCLCL-110	ns
TLLPL	ALE to $\overline{PSEN}$	TCLCL-40		ns
TPLPH	$\overline{PSEN}$ Pulse Width	3TCLCL-45		ns
TPLIV	$\overline{PSEN}$ to Valid Instr in		3TCLCL-105	ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		ns
TPXIZ	Input Instr Float After $\overline{PSEN}$		TCLCL-25	ns
TPXAV	$\overline{PSEN}$ to Address Valid	TCLCL-8		ns
TAVIV	Address to Valid Instr in		5TCLCL-105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10	ns

EXTERNAL DATA MEMORY CHARACTERISTICS

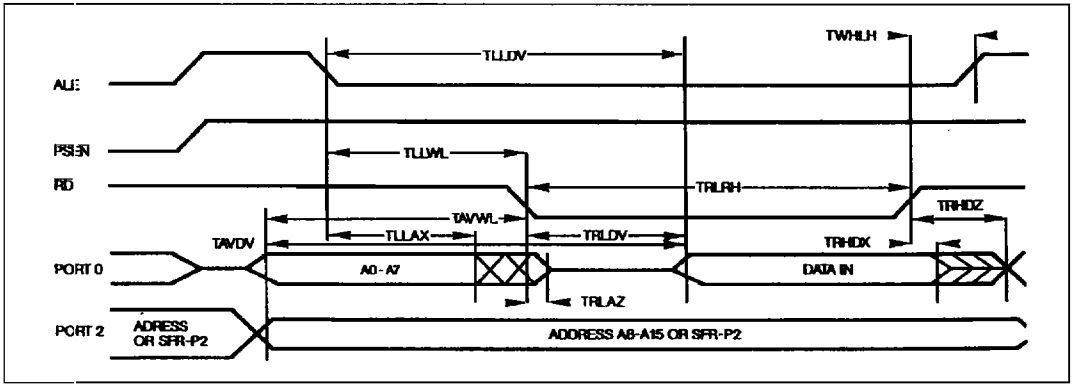
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
TRLRH	$\overline{RD}$ Pulse Width	6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	6TCLCL-100		ns
TLLAX	Data Address Hold After ALE	TCLCL-35		ns
TRLDV	$\overline{RD}$ to Valid Data in		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		ns
TRHDZ	Data Float After $\overline{RD}$		2TCLCL-70	ns
TLLDV	ALE to Valid Data in		8TCLCL-150	ns
TAVDV	Address to Valid Data in		9TCLCL-165	ns
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	3TCLCL-50	3TCLCL+50	ns
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	4TCLCL-130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	TCLCL-60		ns
TQVWH	Data Setup to $\overline{WR}$ High	7TCLCL-150		ns
TWHQX	Data Hold After $\overline{WR}$	TCLCL-50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	TCLCL-40	TCLCL+40	ns

AC TIMING DIAGRAMS

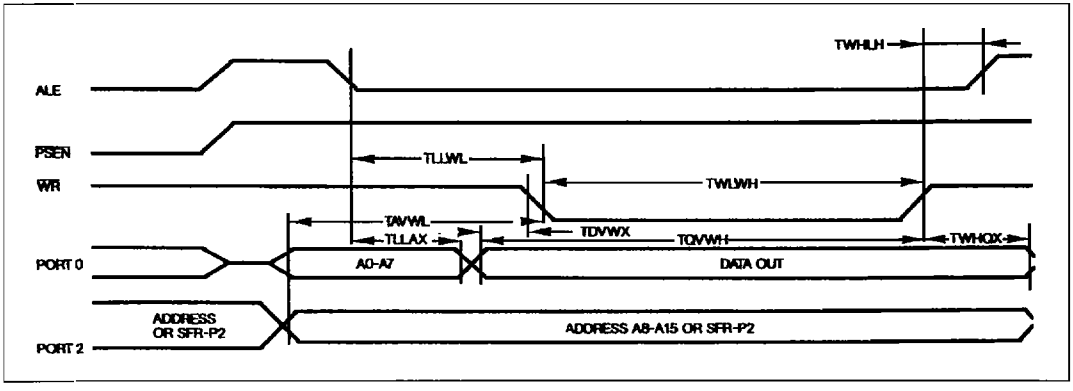
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE



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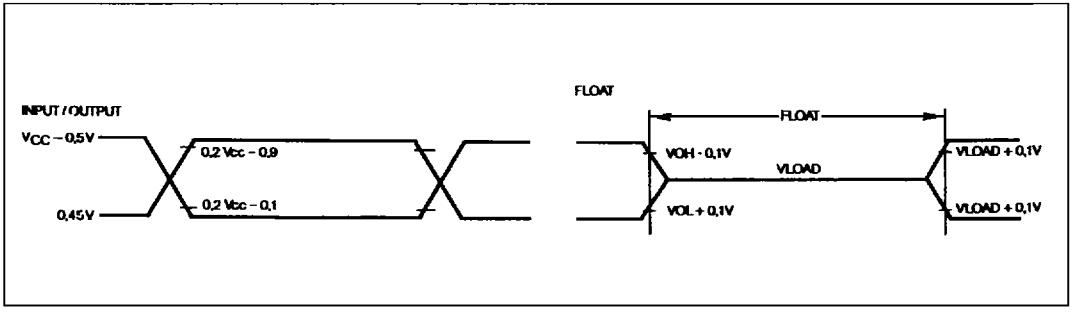
AC TESTING INPUT/OUTPUT, FLOAT WAVEFORMS

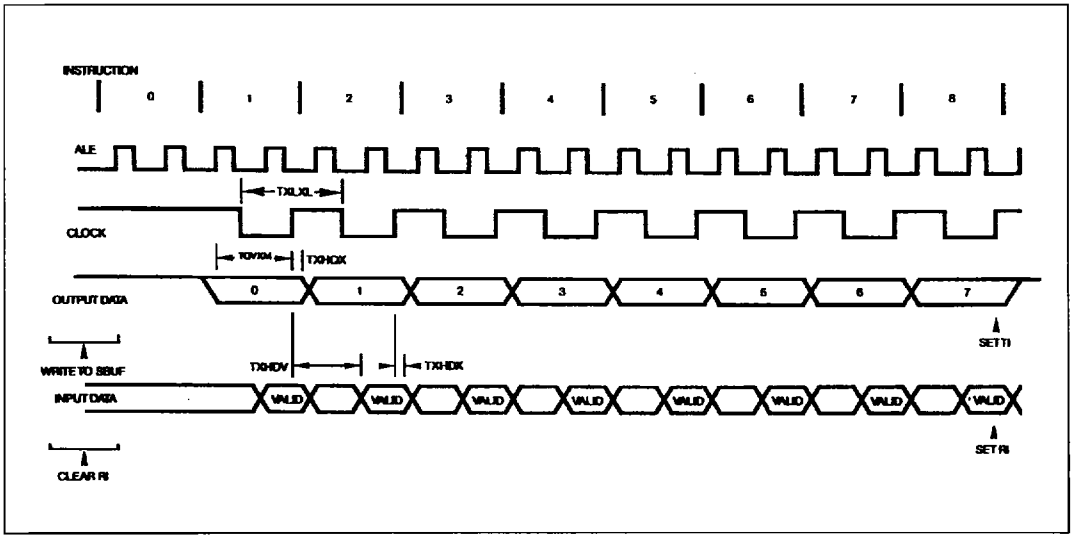


AC inputs during testing are driven at V_{CC} – 0.5 for a logic " 1 " and 0.45 V for a logic " 0 ". Timing measurements are made at VIH min for a logic " 1 " and VIL max for a logic "0".For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded VOH/VOL level occurs. Iol/IoH ≥± 20 Ma.

SERIAL PORT TIMING - SHIFT REGISTER MODE

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
TXLXL	Serial Port Clock Cycle Time	12TCLCL		µs
TQVXH	Output Data Setup to Clock Rising Edge	10TCLCL-133		ns
TXHQX	Output Data Hold after Clock Rising Edge	2TCLCL-117		ns
TXHDX	Input Data Hold after Clock Rising Edge	0		ns
TXHDV	Clock Rising Edge to Input Data Valid		10TCLCL-133	ns

SHIFT REGISTER TIMING WAVEFORMS



EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a " T " (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

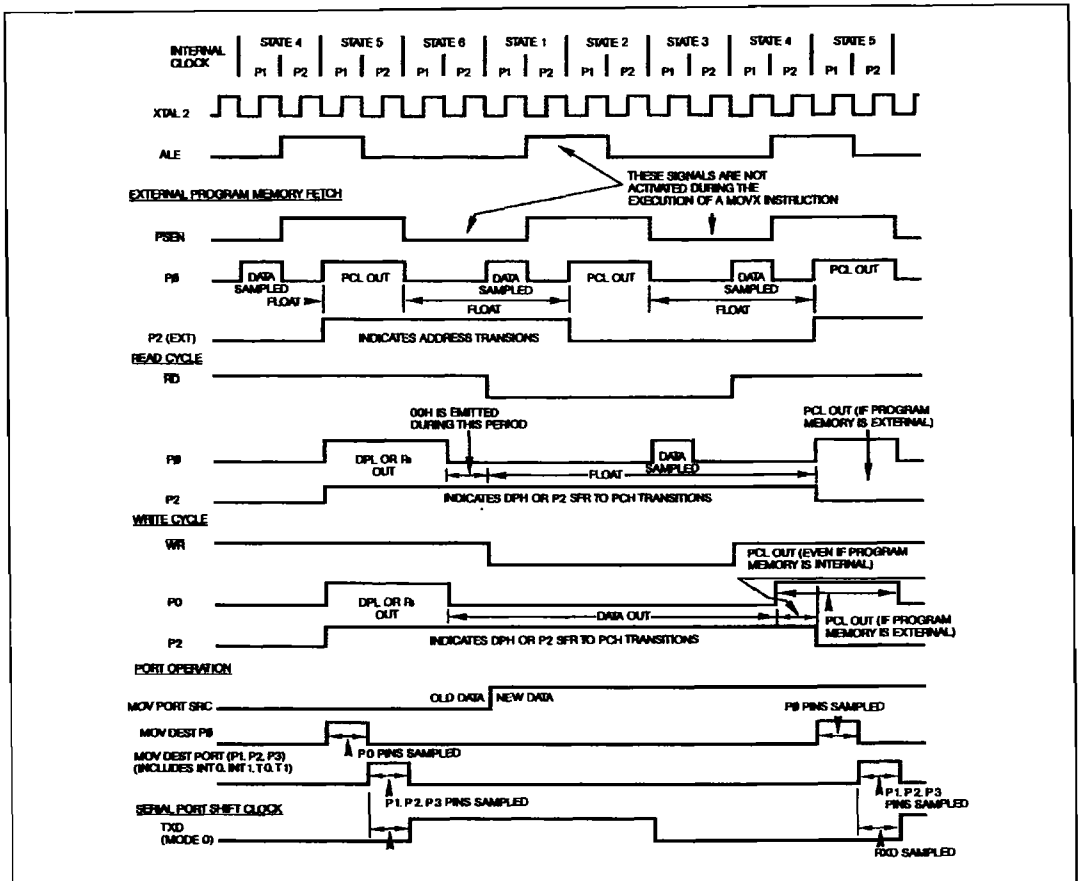
EXAMPLE :

TAVLL = Time for Address Valid to ALE low.

TLLPL = Time for ALE low to $\overline{PSEN}$ low.

A : Address	Q : Output data
C : Clock	R : READ Signal
D : Input Data	T : Time
H : Logic Level HIGH	V : Valid
I : Instruction (program memory contents)	W : WRITE Signal
L : Logic Level LOW, or ALE	X : No Longer a Valid Logic Level
P : PSEN	Z : Float

CLOCK WAVEFORMS



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins however ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component. Typically though (TA = 25°C, fully loaded) RD and WR propagation delays are approximately 50 ns. The other signal are typically 85 ns. Propagation delays are incorporated in the AC specifications.

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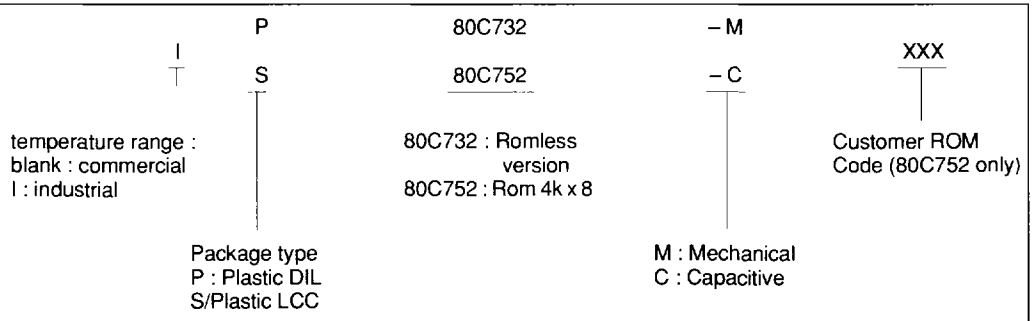
ORDERING INFORMATION



PCK52

* Commercial version in PDIL(P) or PLCC(S) package of PCK52 (Personal Computer Keyboard Controller containing Software PCS52).

PCS52 : (assembly source code only)

* Personal Computer Software dedicated for : IBM PC keyboard.

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