iC-NQI

13-bit Sin/D CONVERTER WITH CALIBRATION

preliminary

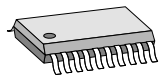
FEATURES

- Resolution of up to 8192 angle steps per sine/cosine period
- Binary and decimal resolution settings, e.g. 500, 512, 1000, 1024; programmable angle hysteresis
- Conversion time of just 250 ns including amplifier settling
- Count-safe vector follower principle, real-time system with a 70 MHz sampling rate
- Direct sensor connection; selectable input gain
- Front-end signal conditioning features offset (8 bits), amplitude ratio (5 bits) and phase (6 bits) calibration
- Input frequency of up to 250 kHz
- Incremental A QUAD B outputs with a selectable minimum transition distance (e.g. 0.25 µs for 1 MHz at A)
- Index signal processing adjustable in position and width
- Serial output of absolute angle data at clock rates of up to 10 MHz
- Error monitoring: frequency, amplitude, configuration (CRC)
- Multiturn counting up to 24 bits
- Device setup from serial EEPROM or 2-wire interface
- ESD protection and TTL-/CMOS-compatible outputs

APPLICATIONS

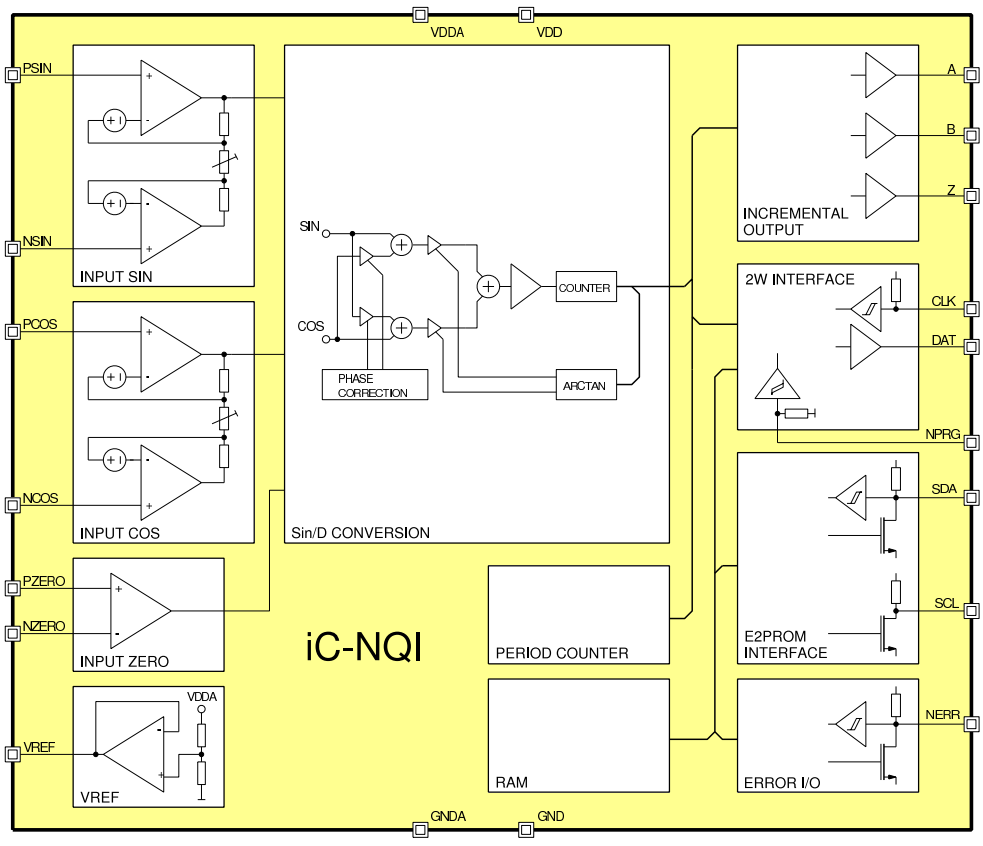
- Interpolator IC for position data acquisition from analog sine/cosine sensors
- Optical linear/rotary encoders
- MR sensor systems

PACKAGES



TSSOP20

BLOCK DIAGRAM



DESCRIPTION

iC-NQI is a monolithic A/D converter which, by applying a count-safe vector follower principle, converts sine/cosine sensor signals with a selectable resolution and hysteresis into angle position data.

The front-end amplifiers are configured as instrumentation amplifiers, permitting sensor bridges to be directly connected without the need for external resistors. Various programmable D/A converters are available for the conditioning of sine/cosine sensor signals with regard to offset, amplitude ratio and phase errors. Front-end gain can be set in stages graded to suit all common differential sensor signals from approximately 20 mVpp to 1.5 Vpp, and also single-end sensor signals from 40 mVpp to 3 Vpp respectively.

Two serial interfaces have been included to permit configuration of the device: I^2C for the connection of an EEPROM and a 2-wire interface for configuration from a microcontroller. A low signal at pin NPRG is required to release the 2-wire interface for programming, whereas a high signal at pin NPRG preselects the serial output of measurement data.

For measurement data output, the fast synchronous-serial 2-wire interface can follow an SSI protocol at clock rates of up to 4 Mbit/s, or a BiSS unidirectional protocol featuring error messages and a CRC-protected transmission at clock rates of up to 10 Mbit/s. A configurable period counter can supplement the measurement data by a multiturn count of up to 24 bits.

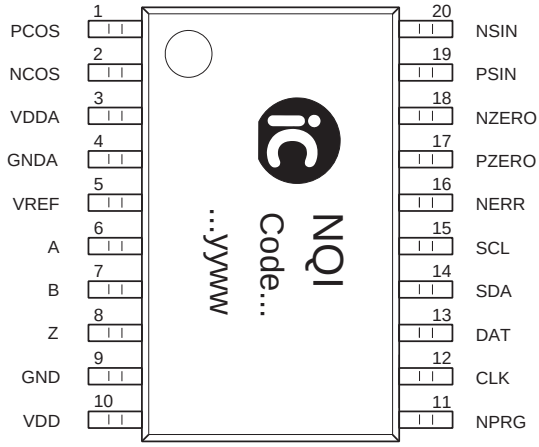
At the same time any changes in output data are converted into incremental A QUAD B encoder signals. Here, the minimum transition distance can be adapted to suit the system on hand (limitations due to counter input frequency, cable length, EMI). A synchronized index signal is generated and output to Z if enabled by the PZERO and NZERO inputs.

If the EEPROM is detected following a power-down reset, the CRC-protected chip setup is read in automatically.

CONTENTS

PACKAGES TSSOP20 (according to JEDEC Standard)

PIN CONFIGURATION
TSSOP20 4.4 mm, lead pitch 0.65 mm



PIN FUNCTIONS

No.	Name	Function
1	PCOS	Input Cosine +
2	NCOS	Input Cosine -
3	VDDA	+5 V Supply Voltage (analog)
4	GNDA	Ground (analog)
5	VREF	Reference Voltage Output
6	A	Incremental Output A Analog signal COS+ (TMA mode) PWM signal for Offset Sine (Calib.)
7	B	Incremental Output B Analog signal COS- (TMA mode) PWM signal for Offset Cosine (Calib.)
8	Z	Output Index Z PWM signal for Phase/Ratio (Calib.)
9	GND	Ground
10	VDD	+5 V Supply Voltage (digital)
11	NPRG	Programming Enable Input (active low)
12	CLK	2W Interface, clock line
13	DAT	2W Interface, data output
14	SDA	EEPROM interface, data line Analog signal SIN+ (TMA mode)
15	SCL	EEPROM interface, clock line Analog signal SIN- (TMA mode)
16	NERR	Error Input/Output, active low
17	PZERO	Input Zero Signal +
18	NZERO	Input Zero Signal -
19	PSIN	Input Sine +
20	NSIN	Input Sine -

External connections linking VDDA to VDD and GND to GNDA are required.

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDDA	Voltage at VDDA		-0.3	6	V
G002	VDD	Voltage at VDD		-0.3	6	V
G003	Vpin()	Voltage at PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF, NERR, SCL, SDA, CLK, DAT, NPRG, A, B, Z	V() < VDDA + 0.3 V V() < VDD + 0.3 V	-0.3	6	V
G004	Imx(VDDA)	Current in VDDA		-50	50	mA
G005	Imx(GNDA)	Current in GNDA		-50	50	mA
G006	Imx(VDD)	Current in VDD		-50	50	mA
G007	Imx(GND)	Current in GND		-50	50	mA
G008	Imx()	Current in PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF, NERR, SCL, SDA, CLK, DAT, NPRG, A, B, Z		-10	10	mA
G009	Ilu()	Pulse Current in all pins (Latch-up Strength)	according to Jedec Standard No. 78; Ta = 25 °C, pulse duration 10 ms, VDDA = $VDDA_{max}$, VDD = VDD_{max}, Vlu() = (-0.5...+1.5) x $Vpin()_{max}$	-100	100	mA
G010	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G011	Tj	Junction Temperature		-40	150	°C
G012	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Operating Conditions: VDDA = VDD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	 TSSOP20 ET -40/125	-25 -40		85 125	°C °C

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA = VDD = 5 V ±10 %, Tj = -40 ... 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDDA, VDD	Permissible Supply Voltage		4.5		5.5	V
002	I(VDDA)	Supply Current in VDDA	fin() = 200 kHz; A, B, Z open			15	mA
003	I(VDD)	Supply Current in VDD	fin() = 200 kHz; A, B, Z open			20	mA
004	Von	Turn-on Threshold VDDA, VDD		3.2		4.4	V
005	Vhys	Turn-on Threshold Hysteresis		200			mV
006	Vc()hi	Clamp Voltage hi at PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF	Vc()hi = V() - VDDA; I() = 1 mA, other pins open	0.3		1.6	V
007	Vc()lo	Clamp Voltage lo at PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, VREF, NERR, SCL, SDA, CLK, DAT, NPRG, A, B, Z	I() = -1 mA, other pins open	-1.6		-0.3	V
008	Vc()hi	Clamp Voltage hi at NERR, SCL, SDA, CLK, DAT, NPRG, A, B, Z	Vc()hi = V() - VDD; I() = 1 mA, other pins open	0.3		1.6	V
Input Amplifiers PSIN, NSIN, PCOS, NCOS							
101	Vin()sig	Permissible Input Voltage Range		0.6		VDDA − 1.1	V
102	Vos()	Input Offset Voltage	Vin() and G() in accordance with table GAIN; G ≥ 20 G < 20	 -10 -15		 10 15	 mV mV
103	TCos	Input Offset Voltage Temperature Drift	see 102		±10		µV/K
104	Iin()	Input Current	V() = 0 V ... VDDA	-50		50	nA
105	GA	Gain Accuracy	G() in accordance with table GAIN	95		102	%
106	GArel	Gain SIN/COS Ratio Accuracy	G() in accordance with table GAIN	97		103	%
107	fhc	Cut-off Frequency	G = 80 G = 2.667	230 650			kHz kHz
108	SR	Slew Rate	G = 80 G = 2.667	4 9			V/µs V/µs
Sin/D Conversion: Accuracy							
201	AAabs	Absolute Angle Accuracy without calibration	referred to 360° input signal, G = 2.667, Vin = 1.5 Vpp, HYS = 0	-1.0		1.0	DEG
202	AAabs	Absolute Angle Accuracy after calibration	referred to 360° input signal, HYS = 0, internal signal amplitude of 2 ... 4 Vpp	-0.5	±0.35	+0.5	DEG
203	AArel	Relative Angle Accuracy	referred to output signal period of A/B, G = 2.667, Vin = 1.5 Vpp, SELRES = 1024, FCTR = 0x0004 ... 0x00FF, fin < fin_{max} (see table 14)	-10		10	%
Reference Voltage VREF							
801	VREF	Reference Voltage	I(VREF) = -1 mA ... +1 mA	48		52	% VDDA
Oscillator							
A01	fosc()	Oscillator Frequency	presented at SCL with subdivision of 2048; VDDA = VDD = 5 V ±10 % VDDA = VDD = 5 V	 52 60	 72	 90 83	 MHz MHz
A02	TCosc	Oscillator Frequency Temperature Drift	VDDA = VDD = 5 V		-0.1		%/K
A03	VCosc	Oscillator Frequency Power Supply Dependance			+10.6		%/V

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDDA = VDD = 5 V ±10 %, Tj = -40 ... 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Zero Comparator							
B01	Vos()	Input Offset Voltage	V() = Vcm()	-20		20	mV
B02	Iin()	Input Current	V() = 0 V ... VDDA	-50		50	nA
B03	Vcm()	Common-Mode Input Voltage Range		1.4		VDDA-1.5	V
B04	Vdm()	Differential Input Voltage Range		0		VDDA	V
Incremental Outputs A, B, Z and 2W Interface Output DAT							
D01	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(); I() = -4 mA			0.4	V
D02	Vs()lo	Saturation Voltage lo	I() = 4 mA			0.4	V
D03	tr()	Rise Time	CL() = 50 pF			60	ns
D04	tf()	Fall Time	CL() = 50 pF			60	ns
D05	RL()	Permissible Load at A, B	TMA = 1 (calibration mode)	1			MΩ
2W Interface: Clock Input CLK, Programming Enable NPRG							
E01	Vt()hi	Threshold Voltage hi				2	V
E02	Vt()lo	Threshold Voltage lo		0.8			V
E03	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	300			mV
E04	Ipu(CLK)	Pull-up Current in CLK	V() = 0 ... VDD - 1 V	-240	-120	-25	µA
E05	Ipd(NPRG)	Pull-down Current in NPRG	V() = 1 ... VDD	20	120	300	µA
E06	fclk(CLK)	Permissible Clock Frequency at CLK	SSI protocol BiSS B/C or C unidir. protocols Register communication (NPRG = lo)			4 10 0.25	MHz MHz MHz
E07	tp(CLK-DAT)	Propagation Delay: CLK edge vs. DAT output	RL(DAT) ≥ 1 kΩ (see Fig. 4)	10		50	ns
E08	tbusy()	Processing Time		0	0	0	
E09	tbusy()r	Processing Time Register Communication (start bit delay)	NPRG = lo; with read access to EEPROM			2	ms
E10	tidle()	Interface Blocking Time	NPRG = lo; powering up with no EEPROM		1	1.5	ms
EEPROM Interface, Control Logic: Inputs SDA, NERR							
F01	Vt()hi	Threshold Voltage hi				2	V
F02	Vt()lo	Threshold Voltage lo		0.8			V
F03	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	300			mV
F04	tbusy()cfg	Duration of Startup Configuration	error free EEPROM access		5	7	ms
EEPROM Interface, Control Logic: Outputs SDA, SCL, NERR							
G01	f()	Write/Read Clock at SCL			20	100	kHz
G02	Vs()lo	Saturation Voltage lo	I() = 4 mA			0.45	V
G03	Ipu()	Pull-up Current	V() = 0 ... VDD - 1 V	-600	-300	-75	µA
G04	ft()	Fall Time	CL() = 50 pF			60	ns
G05	tmin()lo	Error Signal Indication Time at NERR (lo signal)	CLK = hi (keine Datenausgabe), amplitude or frequeny error	10			ms
G06	Tpwm()	Error Signal PWM Cycle Duration at NERR	fosc() subdivided 2^{22}		60.7		ms
G07	RL()	Permissible Load at SDA, SCL	TMA = 1 (calibration mode)	1			MΩ

CHARACTERISTICS: Diagrams

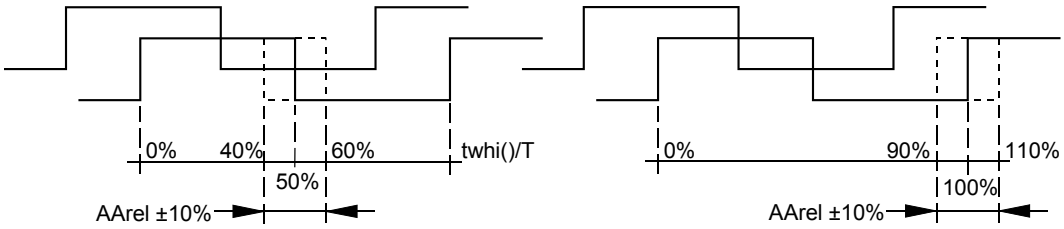


Figure 1: Definition of relative angle error.

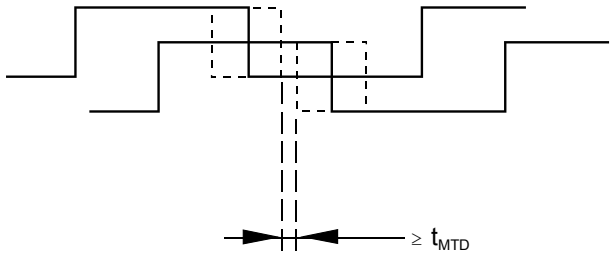


Figure 2: Definition of minimum transition distance.

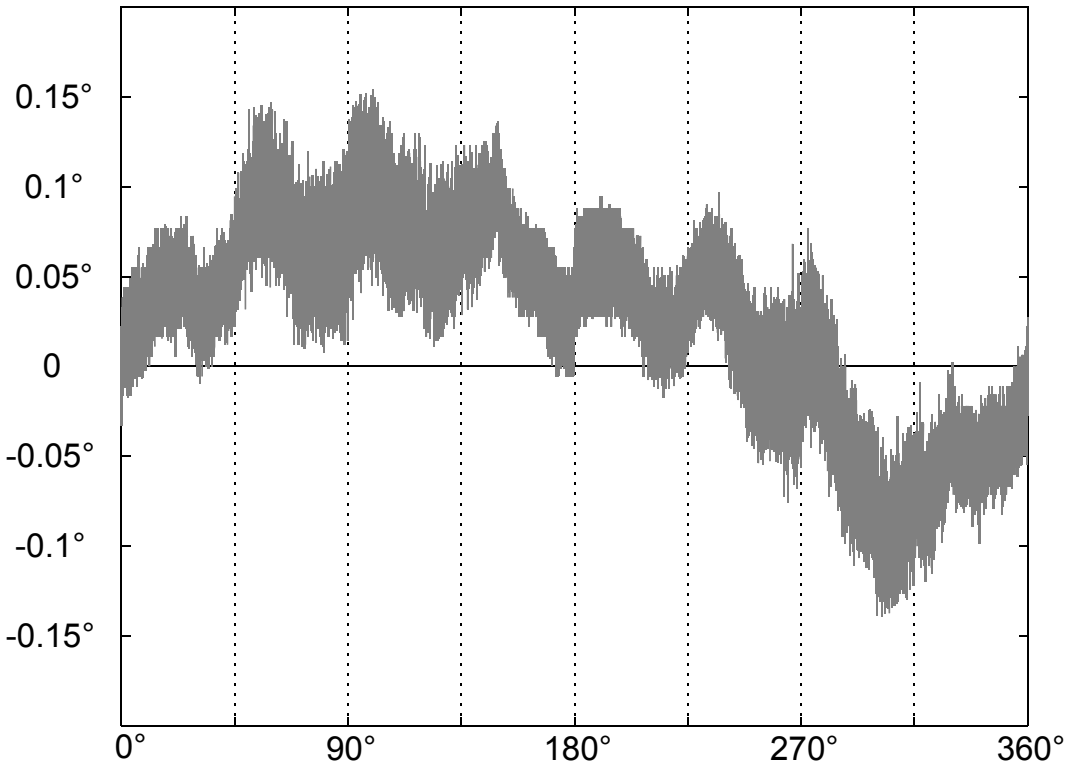


Figure 3: Typical residual absolute angle error after calibration.

OPERATING REQUIREMENTS: 2W Interface

Operating Conditions: VDD = 5 V ±10 %, Ta = -25 ... 85 °C; input levels lo = 0 ... 0.45 V, hi = 2.4 V ... VDD

Item No.	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
Serial Data Output: SSI (Pin NPRG = hi, SELSSI = 1)							
I001	T_{CLK}	Permissible Clock Period	CFGTOS = 0x01	4	250	2x t_{tos}	ns
I002	t_{CLKh}	Clock Signal Hi Level Duration		4	25	t_{tos}	ns
I003	t_{CLKl}	Clock Signal Lo Level Duration		4	25	t_{tos}	ns
Serial Data Output: BiSS B, BiSS C unidir. (Pin NPRG = hi, SELSSI = 0, BiSSMOD = 0 resp. 1)							
I004	T_{CLK}	Permissible Clock Period	CFGTOS selected in accordance with table 31	5, 6	100	2x t_{tos}	ns
I005	t_{CLKh}	Clock Signal Hi Level Duration		5, 6	25	t_{tos}	ns
I006	t_{CLKl}	Clock Signal Lo Level Duration		5, 6	25	t_{tos}	ns
Bidirectional Register Communication (pin NPRG = lo)							
I007	T_{CLK}	Permissible Clock Period	CFGTOR selected in accordance with table 31	7	4		µs
I008	t_{CLKh}	Clock Signal Hi Level Duration		7		t_{tor}	ns
I009	t_{CLKh}	Clock Signal Hi Level Duration	read out of register data	7	30	70	% TCLK
I010	t_{CLKl}	Clock Signal Lo Level Duration		7		indefinite	
I011	t_{CLK0h}	"Logic 0" Hi Level Duration		7	10	30	% TCLK
I012	t_{CLK1h}	"Logic 1" Hi Level Duration		7	70	90	% TCLK

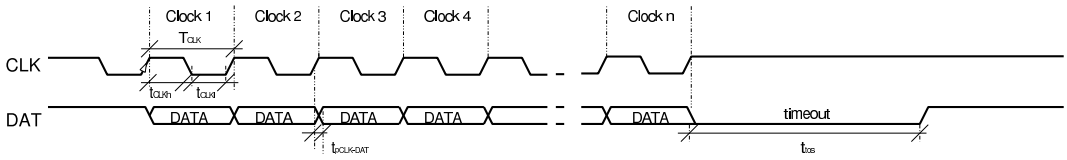


Figure 4: Serial SSI data output (NPRG = hi).

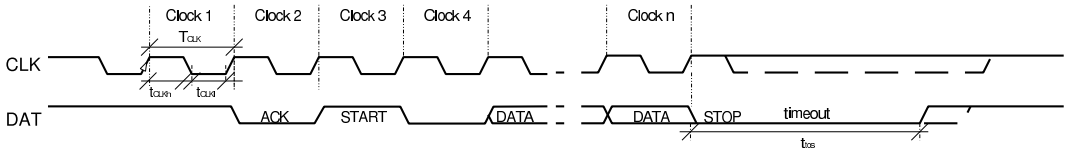


Figure 5: Serial BiSS B data output (NPRG = hi).

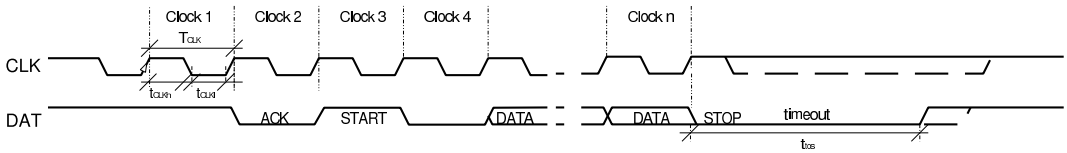


Figure 6: Serial BiSS C unidir. data output (NPRG = hi).

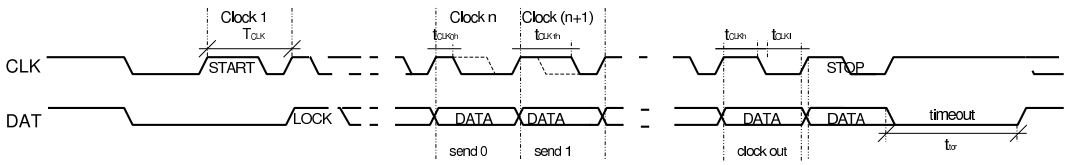


Figure 7: Bidirectional register communication (NPRG = lo).

PARAMETER and REGISTER

OVERVIEW

Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	BiSSMOD	M2S(1:0)		SELRES(4:0)				
0x01	HYS(2:0)			ZPOS(4:0)				
0x02	ENRESDEL	SELSSI	ROT	CBZ	CFGABZ(1:0)		CFGZ(1:0)	
0x03	CFGSSI(1:0)		CFGAB(1:0)		RPL(1:0)		AERR	FERR
0x04	FCTR(7:0)							
0x05		FCTR(14:8)						
0x06	CFGTOR(1:0)		CFGTOS(1:0)		TMODE(2:0)			TMA
0x07	Reserved address / internal use (programming to zero recommended)							
0x08	GAIN(3:0)				RATIO(3:0)			
0x09	SINOFFS(7:0)							
0x0A	COSOFFS(7:0)							
0x0B	PHASE(5:0)						REFOFFS	RATIO(4)
0x0C						SELAMPL	AMPL(1:0)	
0x0D								
0x0E								
0x0F	CRC(7:0) check sum over address 0-14 with CRC polynomial: "100100111" (read out of EEPROM)							
	EEPROM							
0x10 - 0x1F	0x00 - 0xF	EEPROM register section for device configuration						
0x20 - 0x77	0x10 - 0x67	Free EEPROM registers						
0x78 - 0x7F	0x68 - 0x6F	EEPROM: BiSS Identifier, ROM: Device ID iC-NQI V3: 4E 51 56 33 {ADR0} 00 69 43						
As no access protections are selected all registers are accessible by read and write operations (see RPL).								

Table 5: Register layout

SIGNAL CONDITIONING

Input stages SIN and COS are configured as instrumentation amplifiers. The amplifier gain must be selected in accordance with the sensor signal level and programmed to register GAIN according to the following table. Half of the supply voltage is output to VREF as center voltage to help DC level adaptation.

GAIN	Adr 0x08, Bit 7:4				
		Sine/Cosine input signal levels Vin()			
		Amplitude		Average value (DC)	
Code	Amplification	Differential	Single-ended	Differential	Single-ended
0x0F	80.000	up to 50 mVpp	up to 100 mVpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.2 V
0x0E	66.667	up to 60 mVpp	up to 120 mVpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.2 V
0x0D	53.333	up to 75 mVpp	up to 0.15 Vpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.2 V
0x0C	40.000	up to 0.1 Vpp	up to 0.2 Vpp	1.2 V ... VDDA - 1.2 V	1.3 V ... VDDA - 1.3 V
0x0B	33.333	up to 0.12 Vpp	up to 0.24 Vpp	1.2 V ... VDDA - 1.2 V	1.3 V ... VDDA - 1.3 V
0x0A	28.571	up to 0.14 Vpp	up to 0.28 Vpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.3 V
0x09	26.667	up to 0.15 Vpp	up to 0.3 Vpp	1.2 V ... VDDA - 1.2 V	1.3 V ... VDDA - 1.3 V
0x08	20.000	up to 0.2 Vpp	up to 0.4 Vpp	0.7 V ... VDDA - 1.2 V	0.8 V ... VDDA - 1.3 V
0x07	14.287	up to 0.28 Vpp	up to 0.56 Vpp	1.2 V ... VDDA - 1.3 V	1.4 V ... VDDA - 1.4 V
0x06	10.000	up to 0.4 Vpp	up to 0.8 Vpp	1.2 V ... VDDA - 1.3 V	1.4 V ... VDDA - 1.5 V
0x05	8.000	up to 0.5 Vpp	up to 1 Vpp	0.8 V ... VDDA - 1.4 V	1.0 V ... VDDA - 1.6 V
0x04	6.667	up to 0.6 Vpp	up to 1.2 Vpp	0.8 V ... VDDA - 1.4 V	1.1 V ... VDDA - 1.7 V
0x03	5.333	up to 0.75 Vpp	up to 1.5 Vpp	0.9 V ... VDDA - 1.5 V	1.3 V ... VDDA - 1.9 V
0x02	4.000	up to 1 Vpp	up to 2 Vpp	1.2 V ... VDDA - 1.6 V	1.7 V ... VDDA - 2.1 V
0x01	3.333	up to 1.2 Vpp	up to 2.4 Vpp	1.2 V ... VDDA - 1.7 V	1.8 V ... VDDA - 2.3 V
0x00	2.667	up to 1.5 Vpp	up to 3 Vpp	1.3 V ... VDDA - 1.8 V	2.0 V ... VDDA - 2.6 V

Table 6: Gain select

SINOFFS	Adr 0x09, Bit 7:0	
COSOFFS	Adr 0x0A, Bit 7:0	
Code	Output offset	Input offset
0x00	0 V	0 V
0x01	-7.8125 mV	-7.8125* mV / GAIN
...	...	...
0x7F	-0.9922 V	-0.9922 V / GAIN
0x80	0 V	0 V
0x81	+7,8125 mV	+7.8125 mV / GAIN
...	...	...
0xFF	+0.9922 V	+0.9922 V / GAIN
Notes	*) With REFOFFS = 0x00 und VDDA = 5 V.	

Table 7: Offset calibration sine/cosine

REFOFFS	Adr 0x0B, Bit 1
Code	Reference voltage
0x00	Depending on VDDA (example of application: MR sensors)
0x01	Not depending on VDDA (example of application: Sin/Cos encoders)

Table 8: Offset calibration reference

RATIO	Adr 0x0B, Bit 0, Adr 0x08, Bit 3:0		
Code	COS / SIN	Code	COS / SIN
0x00	1.0000	0x10	1.0000
0x01	1.0067	0x11	0.9933
...	...	...	...
0x0F	1.1	0x1F	0.9000

Table 9: Amplitude Calibration

PHASE	Adr 0x0B, Bit 7:2		
Code	Phase shift	Code	Phase shift
0x00	90°	0x20	90°
0x01	90.703125°	0x21	89.296875°
...	...	...	...
0x12	102.65625°	0x32	77.34375°
...	102.65625°	...	77.34375°
0x1F	102.65625°	0x3F	77.34375°

Table 10: Phase calibration

CONVERTER FUNCTIONS

SELRES	Adr 0x00, Bit 4:0	
Code	Binary resolutions	Examples of permissible input frequencies fin_{max} (FCTR 0x0004, 0x4304)
0x00	-	
0x01	-	
0x02	-	
0x03	8192	158 Hz, 635 Hz
0x04	4096	317 Hz, 1.27 kHz
0x05	2048	634 Hz, 2.54 kHz
0x06	1024	1.27 kHz, 5.1 kHz
0x07	512	2.54 kHz, 10.2 kHz
0x08	256	5.1 kHz, 20.3 kHz
0x09	128	10.2 kHz, 40.6 kHz
0x0A	64	20.3 kHz, 81.3 kHz
0x0B	32	40.6 kHz, 162.5 kHz
0x0C	16	81.3 kHz (max. 250 kHz @ 0x4202)
0x0D	8	162 kHz (max. 250 kHz @ 0x4102)
0x0E	-	
0x0F	-	

Table 11: Binary resolutions

SELRES	Adr 0x00, Bit 4:0	
Code	Decimal resolutions	Examples of permissible input frequencies fin_{max} (FCTR 0x0004, 0x4304)
0x10	2000	650 Hz, 2.6 kHz
0x11	1600	812 Hz, 3.3 kHz
0x12	1000	1.3 kHz, 5.2 kHz
0x13	800	1.6 kHz, 6.5 kHz
0x14	500	2.6 kHz, 10.4 kHz
0x15	400	3.2 kHz, 13 kHz
0x16	250 *1	5.2 kHz, 20.8 kHz
0x17	125 *1,2	5.2 kHz, 20.8 kHz
0x18	320	4.1 kHz, 16.3 kHz
0x19	160 *2	4.1 kHz, 16.3 kHz
0x1A	80 *4	4.1 kHz, 16.3 kHz
0x1B	40 *8	4.1 kHz, 16.3 kHz
0x1C	200	6.5 kHz, 26 kHz
0x1D	100 *2	6.5 kHz, 26 kHz
0x1E	50 *1,4	6.5 kHz, 26 kHz
0x1F	25 *1,8	6.5 kHz, 26 kHz
Notes	*1 Not useful with increment A quad B output. *2,4,8 The internal converter resolution is higher by factor 2, 4 or 8.	

Table 12: Decimal resolutions

HYS	Adr 0x01, Bit 7:5		
Code	Hysteresis in degree	Hysteresis in LSB	Absolute error*
0x00	0°		
0x01	0.0879°	1 LSB @ 12 bit	0.044°
0x02	0.1758°	1/2 LSB @ 10 bit	0.088°
0x03	0.3516°	1 LSB @ 10 bit	0.176°
0x04	0.7031°	1/2 LSB @ 8 bit	0.352°
0x05	1.4063°	1 LSB @ 8 bit	0.703°
0x06	5.625°		2.813°
0x07	45°	only recommended for calibration	22.5°
Notes	*) The absolute error is equivalent to one half the angle hysteresis		

Table 13: Hysteresis

MAXIMUM CONVERTER FREQUENCY

The converter frequency automatically adjusts to the value necessary for the input frequency and resolution. This value ranges from zero to a maximum dependent on the oscillator frequency which can be set using register FCTR.

Serial data output
For serial data output the possible maximum converter frequency can be adjusted to suit the maximum input frequency; an automatic converter resolution step-down feature can be enabled via the FCTR register. Should the input frequency exceed the frequency limit of the selected converter resolution, the LSB is kept stable and not resolved any further; the interpolation resolution halves.

If the next frequency limit is overshot, the LSB and the LSB+1 are kept stable and so on. When the input frequency again sinks below this frequency limit, the fine resolution automatically returns.

Maximum Converter Frequency For Serial Data Output

	Resolution Requirements			Protocol		Max. Input Frequency	Restrictions at high input frequencies	Examples* fin_{max} [kHz] at resol.		
FCTR	**Min. Res.**	**bin**	**dec**	**BiSS**	**SSI**	**fin_{max}**		**8192**	**1024**	**200**
0x0004		X	X	X	X	fosc()min / 40 / Resolution	–	0.16	1.27	6.5
0x4102	≥ 8	X	X	X	X	fosc()min / 24 / Resolution	Rel. angle error 2x increased	0.26	2.1	10.8
0x4202	≥ 16	X	X	X	X	2 x fosc()min / 24 / Res.	Rel. angle error 4x increased	0.53	4.2	21.6
0x4303	≥ 32	X	X	X	X	4 x fosc()min / 32 / Res.	Rel. angle error 8x increased	0.78	6.2	32.0
0x4602	≥ 32	X	-	X	X	4 x fosc()min / 24 / Res.	Resolution lowered by factor of 2	1.1	8.5	-
0x4A02	≥ 64	X	-	X	X	8 x fosc()min / 24 / Res.	Res. lowered by factor of 2-4	2.1	16.9	-
0x4E02	≥ 128	X	-	X	X	16 x fosc()min / 24 / Res.	Res. lowered by factor of 2-8	4.2	33.8	-
0x5202	≥ 256	X	-	X	X	32 x fosc()min / 24 / Res.	Res. lowered by factor of 2-16	8.5	67.7	-
0x5602	≥ 512	X	-	X	X	64 x fosc()min / 24 / Res.	Res. lowered by factor of 2-32	16.9	135	-
0x5A02	≥ 1024	X	-	X	X	128 x fosc()min / 24 / Res.	Res. lowered by factor of 2-64	33.8	250	-
0x5E02	≥ 2048	X	-	X	X	256 x fosc()min / 24 / Res.	Res. lowered by factor of 2-128	67.7	-	-
0x6202	4096	X	-	X	X	512 x fosc()min / 24 / Res.	Res. lowered by factor of 2-256	135	-	-
Notes	*) Calculated with fosc()min taken from Electrical Characteristics item A01.									

Table 14: Possible maximum converter frequency for serial data output.

Incremental output to A, B and Z
There are two criteria which must be considered when setting the maximum possible converter frequency via the FCTR register:

1. The maximum input frequency
2. System limitations, e.g. due to slow counters or cable transmission

When facing system limitations it is useful to preselect a minimum transition distance for the output signals. A digital zero-delay glitch filter then takes care of a temporal edge-to-edge separation, guaranteeing spike-free output signals after an ESD impact to the sensor, for instance.

A serial data output is simultaneously possible at any time. However, for the transfer of angle data to the output register the incremental output is halted for one period of the clock signal applied to pin CLK.

1. Maximum Converter Frequency Defined By The Maximum Input Frequency								
	Output Frequency fout @ fin_{max}	Resolution Requirem.		Maximum Input Frequency	Restrictions at high input frequencies	Examples* fin_{max} [kHz] at resol.		
FCTR	**A, B**	**bin**	**dec**	**fin_{max}**		**8192**	**1024**	**200**
0x0004	325 kHz	X	X	fosc()min / 40 / Resolution	None	0.16	1.27	6.5
0x4102	542 kHz	X	X	fosc()min / 24 / Resolution	Relative angle error 2x increased	0.26	2.1	10.8
0x4202	1.08 MHz	X	X	2 x fosc()min / 24 / Res.	Relative angle error 4x increased	0.53	4.2	21.6
0x4303	1.6 MHz	X	X	4 x fosc()min / 32 / Res.	Relative angle error 8x increased	0.78	6.2	32.0
Notes	*) Calculated with fosc()min taken from Electrical Characteristics item A01.							

Table 15: Possible maximum converter frequency for incremental A/B/Z output, defined by the maximum input frequency

2. Maximum Converter Frequency Defined By The Minimum Transition Distance						
	Output Frequency fout @ t_{MTD}	Resolution Requirem.		Minimum Transition Distance at A, B	Restrictions at high input frequencies	Example* t_{MTD} [µsec]
FCTR	**A, B**	**bin**	**dec**	**t_{MTD}**		
0x00FF	10 kHz	X	X	2048 / fosc()max	None	22.8
0x00FE	10.05 kHz	X	X	2040 / fosc()max	None	22.7
0x00FD	10.09 kHz	X	X	2032 / fosc()max	None	22.6
...	...	...	...	...	...	...
0x0006	366 kHz	X	X	56 / fosc()max	None	0.62
0x0005	427 kHz	X	X	48 / fosc()max	None	0.53
0x0004	512 kHz	X	X	40 / fosc()max	None	0.44
0x4102	854 kHz	X	X	24 / fosc()max	Relative angle error 2x increased	0.27
0x4202	1.7 MHz	X	X	12 / fosc()max	Relative angle error 4x increased	0.13
0x4303	2.8 MHz	X	X	8 / fosc()max	Relative angle error 8x increased	0.09
Notes	*) Calculated with fosc()max taken from El.Char. item A01; the min. transition distance refers to output A vs. output B without reversing the sense of rotation.					

Table 16: Possible maximum converter frequency for incremental A/B/Z output, defined by the minimum transition distance

INCREMENTAL SIGNALS

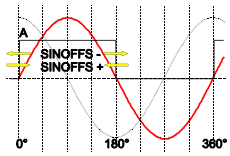
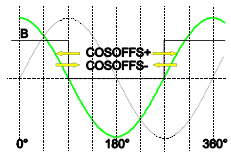
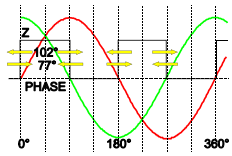
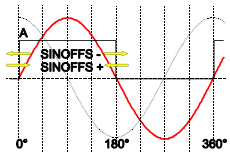
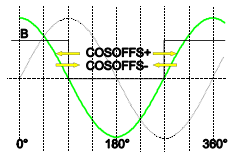
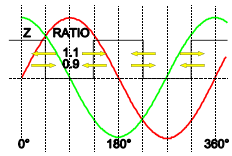
CFGABZ	Adr 0x02, Bit 3:2			
Code	Mode	A	B	Z
0x00	Normal	A	B	Z
0x01	Control signals for external period counters	CA	CB	CZ
0x02	Calibration mode **Offset+Phase** The following settings are required additionally: SELRES = 0x0D ZPOS = 0x00 HYS = 0x07 ROT = 0x00 CFGAB = 0x00 AERR = 0x00	 Figure 8: Offset SIN*	 Figure 9: Offs. COS*	 Figure 10: Phase*
0x03	Calibration mode **Offset+Amplitude** The following settings are required additionally: SELRES = 0x0D ZPOS = 0x00 HYS = 0x07 ROT = 0x00 CFGAB = 0x00 AERR = 0x00	 Figure 11: Offset SIN*	 Figure 12: Offs. COS*	 Figure 13: Amplit.*
Notes	*) Trimmed accurately when duty cycle is 50 %; Recommended trimming order (after selecting GAIN): Offset, Phase, Amplitude Ratio, Offset;			

Table 17: Outputs A, B, Z

ROT	Adr 0x02, Bit 5
Code	Code direction
0x00	Ascending order, B then A
0x01	Descending order, A then B

Table 18: Code direction

CBZ	Adr 0x02, Bit 4
Code	Clear by zero
0x00	Disabled
0x01	Enabled

Table 19: Reset enable for period counter

ENRESDEL	Adr 0x02, Bit 7	
Code	Output*	Function
0x00	immediately	An external counter displays the absolute angle following power on.
0x01	after 5 ms	An external counter only displays changes vs. the initial power-on condition (moving halted to reapply power is precondition.)
Notes	*) Output delay after device configuration and internal reset.	

Table 20: Output turn-on delay A, B, Z

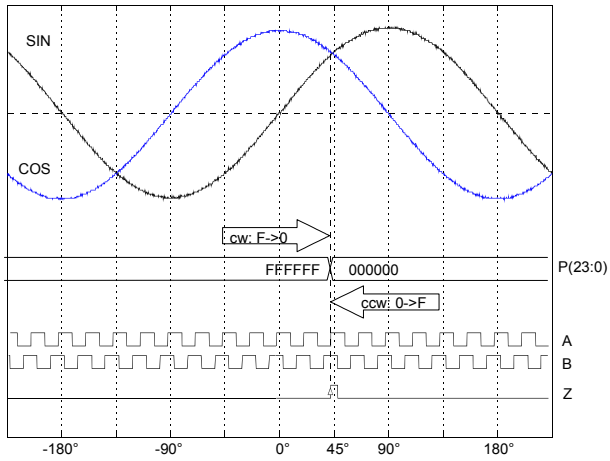


Figure 14: Clear by zero function of the period counter when enabled by CBZ = 1. Example for resolution 64 (SELRES = 0x0A), zero signal at 45° (ZPOS = 0x04, CFGAB = 0x00) and the direction of rotation not inverted (ROT = 0x00, COS leads SIN).

ZPOS	Adr 0x01, Bit 4:0
Code	Position
0x00	0°
0x08	90°
0x10	180°
0x18	270°
0x01	11.25° (1 x 11.25°)
...	...
0x1F	348.75° (31 x 11.25°)
Notes	The zero signal is only output if released by the input pins (for instance with PZERO = 5 V, NZERO = VREF).

Table 21: Zero signal position

CFGZ	Adr 0x02, Bit 1:0
Code	Length
0x00	90°
0x01	180°
0x02.. 03	Synchronization

Table 22: Zero signal length

CFGAB	Adr 0x03, Bit 5:4
Code	Z = 1 for
0x00	B = 1, A = 1
0x01	B = 0, A = 1
0x02	B = 1, A = 0
0x03	B = 0, A = 0

Table 23: Zero signal logic

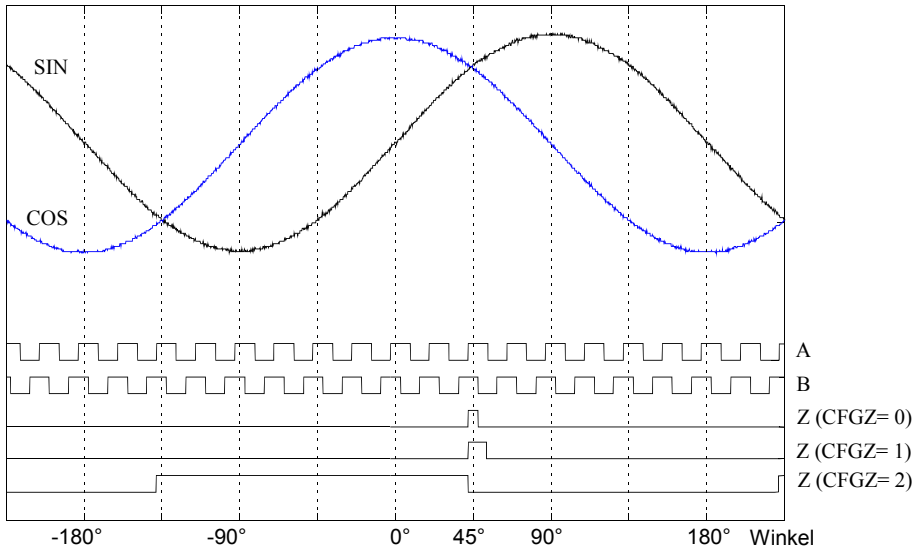


Figure 15: Incremental output signals for various length of the zero signal.
Example for resolution 64 (SELRES = 0x0A), a zero signal position of 45° (ZPOS = 0x04, CFGAB = 0x00) and no reversal of the rotational sense (ROT = 0x00, COS leads SIN).

SIGNAL MONITORING and ERROR MESSAGES

SELAMPL Adr 0x0C, Bit 2 **AMPL** Adr 0x0C, Bit 1:0		
Max (|Sin| , |Cos|) for SELAMPL = 0		
Code	Voltage threshold V_{th}	Output amplitude*
0x00	0.60 x VDDA	1.4 V_{pp}
0x01	0.64 x VDDA	2.0 V_{pp}
0x02	0.68 x VDDA	2.6 V_{pp}
0x03	0.72 x VDDA	3.1 V_{pp}
Sin^2 + Cos^2 for SELAMPL = 1		
Code	$V_{thmin} \leftrightarrow V_{thmax}$	Output amplitude*
0x04	0.48 ↔ 0.68 x VDDA	2.4 V_{pp} ↔ 3.4 V_{pp}
0x05	0.56 ↔ 0.76 x VDDA	2.8 V_{pp} ↔ 3.8 V_{pp}
0x06	0.64 ↔ 0.84 x VDDA	3.2 V_{pp} ↔ 4.2 V_{pp}
0x07	0.72 ↔ 0.92 x VDDA	3.6 V_{pp} ↔ 4.6 V_{pp}
Notes	*) Entries are calculated with VDDA = 5 V.	

Table 24: Signal amplitude monitoring

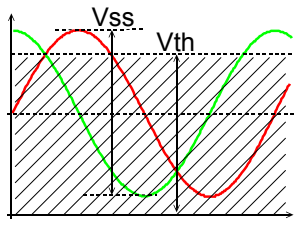


Figure 16: Signal monitoring of minimum amplitude.

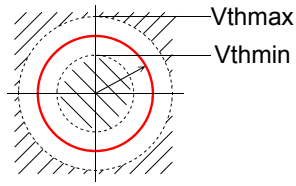


Figure 17: Sin^2 + Cos^2 signal monitoring.

AERR	Adr 0x03, Bit 1
Code	Amplitude error message
0x00	disabled
0x01	enabled

Table 25: Amplitude error

FERR	Adr 0x03, Bit 0
Code	Excessive frequency error message
0x00	disabled
0x01	enabled
Note	Input frequency monitoring is operational for resolutions ≥ 16

Table 26: Frequency error

Configuration error	
-	Messaging always released

Table 27: Configuration error

Error keys		
Failure mode	Pin NERR	Error bits E1, E0 with BiSS and SSI
No error	HI	11
Amplitude error	LO/HI = 75 % (AERR = 0: HI)	01 (11)
Frequency error	LO/HI = 50 % (FERR = 0: HI)	10 (11)
Configuration	LO	00
Undervoltage	LO	00
System error	NERR = low caused by an external error signal	00

Table 28: Error keys

Each phase in the configuration process is signaled by NERR = low; the signal is only reset following a successful CRC (cyclic redundancy check).

If the data transfer from the EEPROM is faulty and the CRC unsuccessful, then the configuration phase is automatically repeated. The process aborts following a third unsuccessful attempt and the error message output remains set to low.

To enable the successful diagnosis of faults other types of error are signaled at NERR using a PWM code as given in the key on the left.

Two error bits are provided for error messaging via the serial 2-wire interface; these bits can decode four different types of error. If NERR is held at low by an external source, such as an error message from the system, for example, this can also be verified via the serial 2-wire interface.

Error events are stored for the serial data output and deleted afterwards. Errors at NERR are displayed for a minimum of ca. 10 ms, as far as no serial data readout causes a deletion.

If an error in amplitude occurs the conversion process is terminated and the incremental output signals halted. An error in amplitude rules out the possibility of an error in frequency.

TEST FUNCTIONS

TMODE	Adr 0x06, Bit 3:1	
Code	Signal at Z	Description
0x00	Z	no test mode
0x01	A xor B	Output A EXOR B
0x02	ENCLK	iC-Haus device test
0x03	NLOCK	iC-Haus device test
0x04	CLK	iC-Haus device test
0x05	DIVC	iC-Haus device test
0x06	PZERO - NZERO	iC-Haus device test
0x07	TP	iC-Haus device test
Condition	CFGABZ = 0x00	

Table 29: Test mode

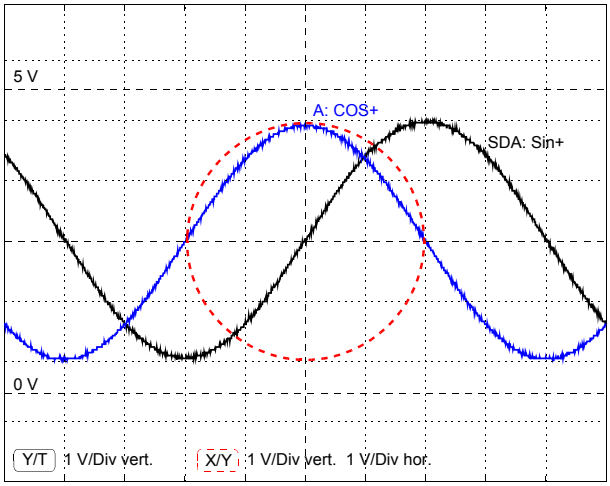


Figure 18: Calibrated signals during analog test mode.

TMA	Adr 0x06, Bit 0			
Code	**Pin A**	**Pin B**	**Pin SDA**	**Pin SCL**
0x00	A	B	SDA	SCL
0x01	COS+	COS-	SIN+	SIN-
Notes	To permit the verification of GAIN and OFFSET settings, the input amplifier outputs are available at the pins. To operate the converter a signal of 4 Vpp is the ideal here and should not be exceeded. Pin loads above 1 MΩ are adviceable for accurate measurements. EEPROM access is not possible during mode TMA.			

Table 30: Analog test mode

Parameter GAIN ideally adjusts the signal levels to ca. 4 Vpp and should not be touched afterwards.

Both scope display modes are feasible for OFFS (positive values) or RATIO adjustments; regarding the adjustment of PHASE the X/Y mode may be preferred.

For OFFS adjustment towards negative values the test signals COS- (pin B) and SIN- (pin SCL) are relevant.

SERIAL 2-WIRE INTERFACE

Depending on the programming enable at pin NPRG the serial 2-wire interface supports either a fast cyclic data output of the angle position and period counter data (for NPRG = 1), or bidirectional register communication for device programming, with write and read access to RAM and EEPROM registers (for NPRG = 0).

Two timeouts are used that prescribe a default minimum clock frequency of f(CLK)min for the master: sensor mode timeout Ttos and register mode timeout Ttor.

For data to be transferred to the interface conversion is halted for one CLK pulse from *Latch*. This time must be taken into consideration with low clock frequencies when calculating the maximum permissible input frequency.

As long as the configuration error is active, the longest respective timeouts are set regardless of CFGTOS or CFGTOR.

CFGTOS	Adr 0x06, Bit 5:4		
Code	Timeout t_{tos} data output	Ref. clock counts	f(CLK) min*
0x00	typ. 128 µs	256-259	11 kHz
0x01	typ. 16 µs	32-35	88 kHz
0x02	typ. 4 µs	8-11	352 kHz
0x03	typ. 1 µs	2-5	1.41 MHz
CFGTOR	Adr 0x06, Bit 7:6		
Code	Timeout t_{tor} programming	Ref. clock counts	f(CLK) min*
0x00	typ. 1 ms	2049-2060	1.4 kHz
0x01	typ. 256 µs	513-514	5.5 kHz
0x02	typ. 32 µs	67-68	42 kHz
0x03	not permitted	–	–
Notes	A ref. clock count is equal to $\frac{32}{fosc}$ (see El. Char. A01). The permissible max. clock frequency is specified by item E06.		

Table 31: 2-wire interface timeout

Serial data output

The position data provided by iC-NQI can contain the following data values: period counter (P), angle data (S), two error bits (E1, E0), and 5 or 6 CRC bits.

Signal names	
Name	Description
P(23:0)	Period counter (0, 8, 12 or 24 bit)
S(12:0)	Angle data (3 to 13 bit)
E1	Error bit (amplitude error)
E0	Error bit (frequency error)
(0)	Zero bit(s)
CRC(5:0)	CRC bits, inverted output, 5 or 6 bits
	Polynomial $x^5 + x^2 + x^0$ (0x25, resp. 100101)
	Polynomial $x^6 + x^1 + x^0$ (0x43, resp. 1000011) with period counter output of 12 or 24 bit

Table 32: Signal names

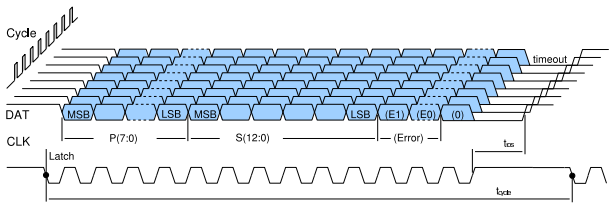


Figure 19: Output with SSI protocol (error bits optional)

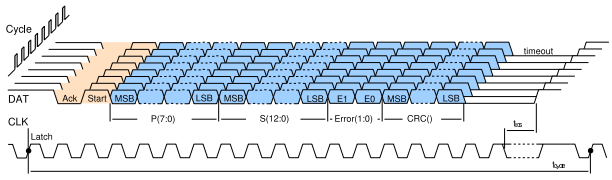


Figure 20: Output with BiSS B protocol

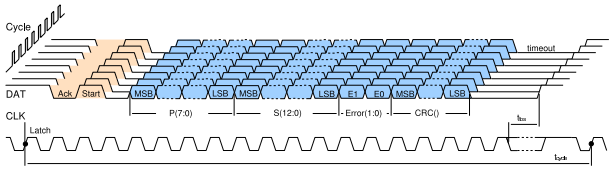


Figure 21: Output with BiSS C unidirectional protocol

Four parameters are relevant when setting the output protocol and data content; SELSSI and BiSSMOD select the protocol version, and M2S and CFGSSI define the optional data content.

SELSSI	Adr 0x02, Bit 6
Code	Description
0x00	Data output BiSS compatible
0x01	Data output with SSI protocol (in binary format, MSB first)

Table 33: Protocol version

BiSSMOD	Adr 0x00, Bit 7
Code	Description
0x00	Data output BiSS B or SSI
0x01	Data output BiSS C unidirectional

Table 34: Protocol version

M2S	Adr 0x00, Bit 6:5		
Code	Data length	CRC poly.	Zero bit
0x00	-	0x25	yes
0x01	P(7:0)	0x25	yes
0x02	P(11:0)	0x43	yes
0x03	P(23:0)	0x43	no

Table 35: Period counter output

CFGSSI	Adr 0x03, Bit 7:6	
Code	Additional bits	Ring register operation
0x00	E1, E0, zero bit	no
0x01	none	no
0x02	E1, E0, zero bit	yes
0x03	none	yes

Table 36: Output options for SSI protocol

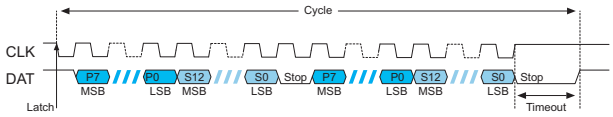


Figure 22: Ring operation with SSI protocol.

Examples of data output with SSI protocol

SSI Output Formats																							
13-bit SSI																							
Res	**Mode**	**Error**	**CRC**	**T1**	**T2**	**T3**	**T4... T10**	**T11**	**T12**	**T13**	**T14**	**T15**	**T16**	**T17**	**T18**	**T19**	**T20**	**T21**	**T22**	**T23**	**T24**	**T25**
10 bit	SSI	X	-	S9	S8	S7	S6 ... S0	E1	E0	0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
			Example							0	0	0	0	0	0	0	0	0	0	0	0	0
13 bit	SSI *1	-	-	S12	S11	S10	S9 ... S3	S2	S1	S0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
			Example								0	0	0	0	0	0	0	0	0	0	0	0
	SSI-R *2	-	-	S12	S11	S10	S9 ... S3	S2	S1	S0	Stop	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2
			Example								0											
25-bit SSI																							
13 bit	SSI	X	-	S12	S11	S10	S9 ... S3	S2	S1	S0	E1	E0	0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
			Example										0	0	0	0	0	0	0	0	0	0
8 + 13 bit *3	SSI	X	-	P7	P6	P5	P4 ... P0, S12, S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	E1	E0	0	Stop
			Example																		0	0
			Configuration	NPRG = 0, SELSSI = 1, M2S = 0x00, CFGSSI = 0x00, unless otherwise noted. *1 CFGSSI = 0x01; *2 CFGSSI = 0x03; *3 M2S = 0x01																			
			Caption	SSI = SSI protocol SSI-R = SSI ring operation																			

Table 37: SSI output formats

Bidirektional register communication
The bidirectional programming mode for write and read access to RAM and EEPROM registers is active for pin NPRG = 0. Data is transmitted coded as a PWM which makes a simple transfer of clock pulse and data to the master clock line possible. A duty cycle of 75 % represents a logic one, a duty cycle of 25 % a logic zero.

The addressing sequence consists of a start bit (’1’), the device address (slave ID ’000’), the register address (7 bits), a write/read bit WNR (’1’ for write, ’0’ for read), a 4-bit CRC, and a stop bit (’0’). The generator polynomial for the 4-bit CRC is 0x13 (or ’10011’); the CRC bits are transmitted in inversion.

Register communication: read
The master carries out the addressing sequence with the WNR bit at ’0’ and subsequently supplies at least 14 clock pulses. iC-NQI responds with a start bit (’1’), the addressed register byte (Data(7...0)), a 4-bit CRC (NCRC(3...0)), and a stop bit (’0’). The generator polynomial for the 4-bit CRC is also 0x13 (or ’10011’) and the CRC bits are again transmitted in inversion.

When reading out the internal registers iC-NQI does not require any processing time and responds immediately with the addressed register data. When reading the external EEPROM registers, output of the start bit is delayed until data is available from the EEPROM. During this wait period the master must continue the clock output.

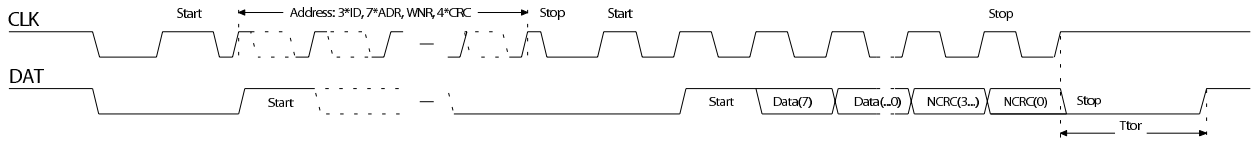


Figure 23: Register communication: read

Register communication: write
To write data to a register the master carries out the addressing sequence with the WNR bit set to ’1’. After the second start bit the master transmits the data to be written which iC-NQI returns bit by bit one clock pulse later for verification. The 8 bits of write data are anticipated by a 4-bit CRC (as before) and also returned by iC-NQI, this time not coded as a PWM, however.

If access to the addressed register is protected, neither the start bit nor data are returned (the master ends the clock output after ca. 20 ms).

Data is transferred to EEPROM registers in the background and can be verified by a read access once transmission has finished.

Write access to address 0 triggers an internal reset. This enables the period counter to be set to zero and the configuration error deleted; the EEPROM is not read out again.

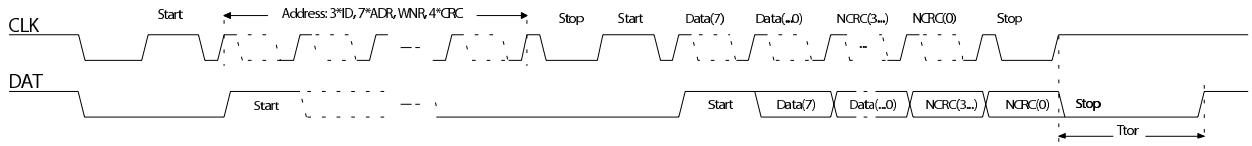


Figure 24: Register communication: write

As long as the configuration error is active, iC-NQI uses the longest respective timeouts regardless of CFGTOS or CFGTOR and ignores possible protective settings from RPL. When programming for the first time, the following addressing sequence is thus recommended: first addresses 1 to 12 and then address 0.

RPL	Adr 0x03, Bit 3:2		
RPL	Configuration Addr 0-31	User Addr 32-119	BiSS Identifier Addr 120-127
0x00	Read / Write	Read / Write	Read / Write
0x01	Read	Read / Write	Read
0x02	-	Read / Write	Read
0x03	-	Read	Read

Table 38: Register protection settings

EEPROM INTERFACE

Serial EEPROM components permitting operation from 3.3 V to 5 V can be connected (such as 24C02, for example). When the device is switched on the memory area of bytes 0 to 15 is mapped onto iC-NQI's registers.

For register communication with the EEPROM an address offset of 16 bytes must be taken into account; addresses 16-127 are destined for the EEPROM bytes of addresses 0-111.

If no EEPROM is connected, iC-NQI does not respond to addresses 16-119; reading addresses 120-127 transmits the device ID.

APPLICATION HINTS

Principle Input Circuits

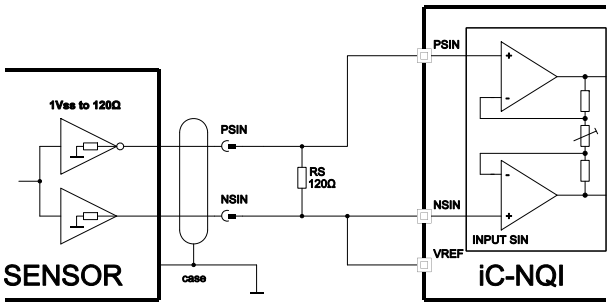


Figure 25: Input circuit for voltage signals of 1 Vpp with no ground reference. When grounds are not separated the connection NSIN to VREF must be omitted.

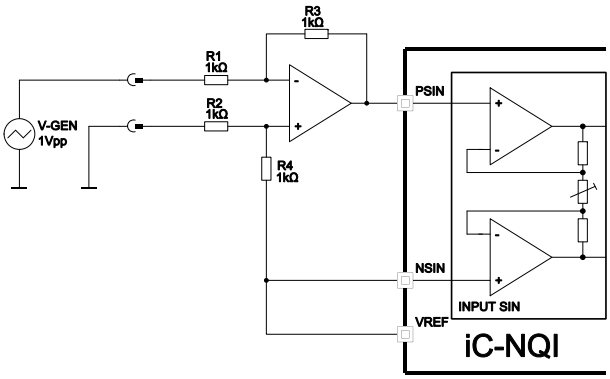


Figure 27: Input circuit for single-side voltage or current source signals with ground reference (adaptation via resistors R3, R4).

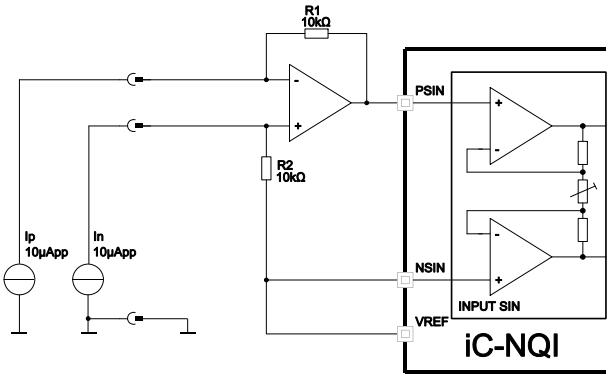


Figure 29: Input circuit for differential current sink sensor outputs, eg. using Opto Encoder iC-WG.

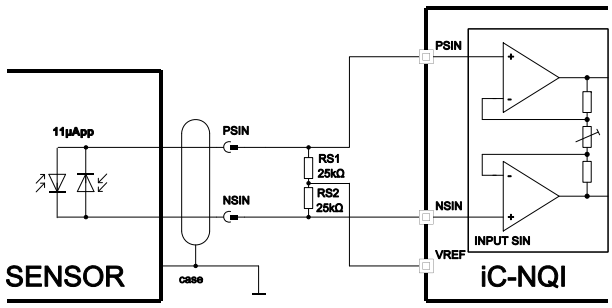


Figure 26: Input circuit for current signals of 11 µA.

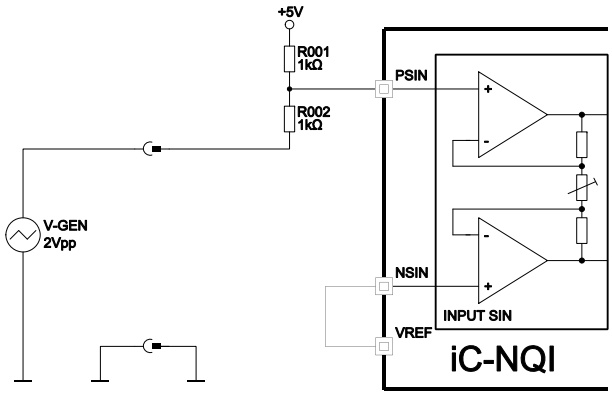


Figure 28: Simplified input wiring for single-side voltage signals with ground reference.

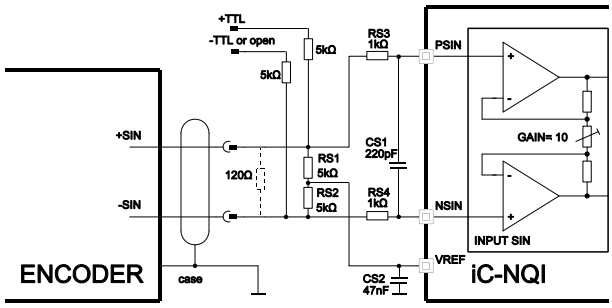


Figure 30: Combined input circuit for 11 µA, 1 Vpp (with 120 Ω termination) or TTL encoder signals. RS3/4 and CS1 serve as protection against ESD and transients.

Basic Circuits

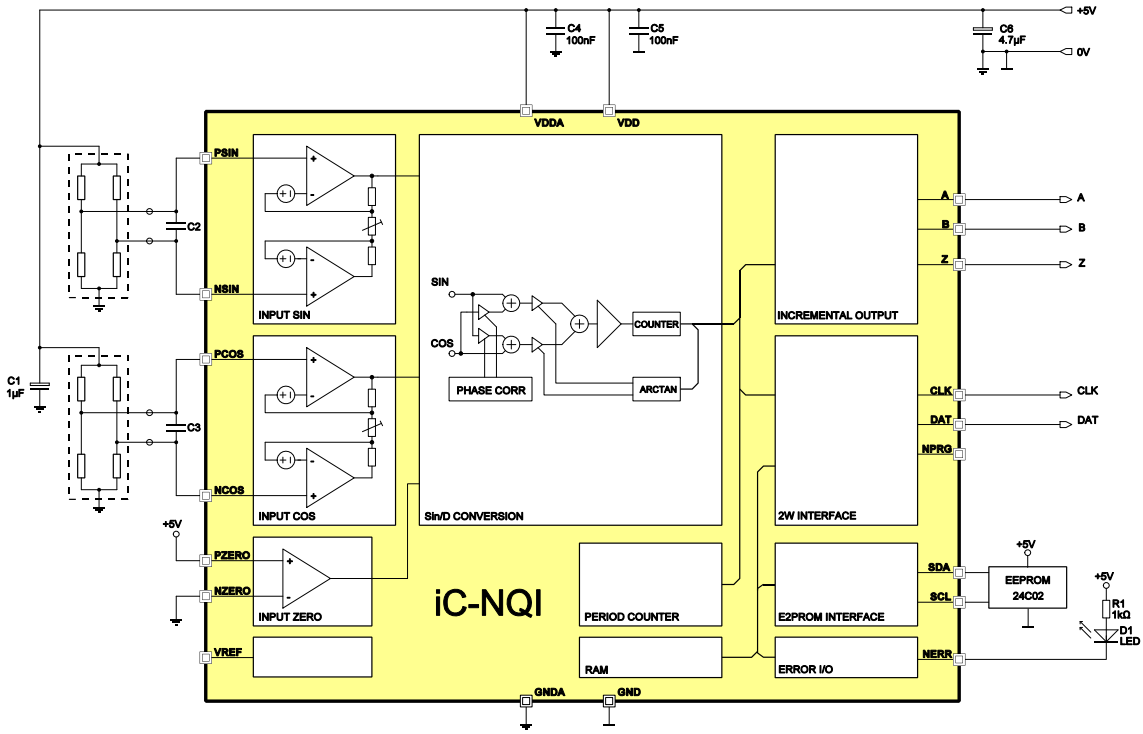


Figure 31: Circuit for evaluation of magneto-resistor bridge sensors with inremental output.

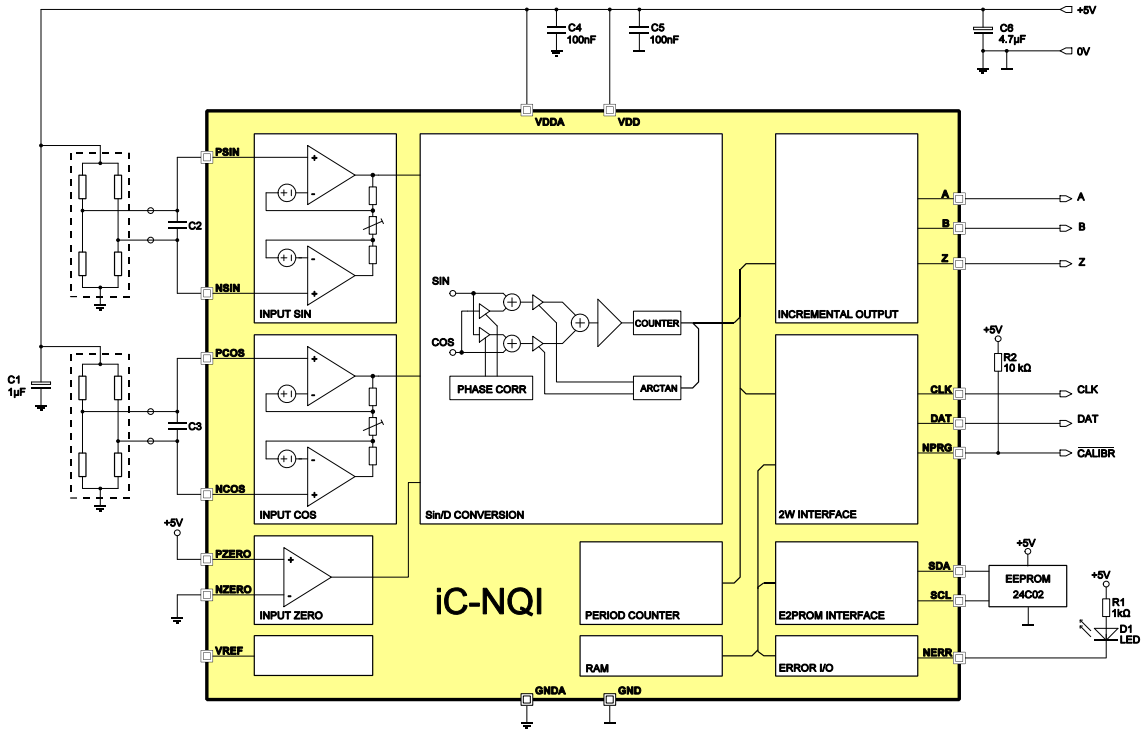


Figure 32: Circuit for evaluation of magneto-resistor bridge sensors with serial data output.

EVALUATION BOARD

The iC-NQI device is equipped with an evaluation board for test purposes; descriptions are available separately.

DESIGN REVIEW: Notes On Chip Functions

iC-NQI V3		
No.	Function, Parameter/Code	Description and Application Hints
1	**SELRES** Illegal setting: 0x0E for resolution 4	A minimal resolution of 8 is required for the frequency monitoring function and period counting as well. Thus, a binary resolution of 4 is not permitted when using the period counter and the serial interface for data output with the BiSS or SSI protocol. A resolution of 4 may be used for solely incremental applications with A/B/Z output, what then requires the deactivation of the frequency monitoring function (by FERR set to 0x00).

Table 39: Notes on chip functions regarding iC-NQI chip release V3

ORDERING INFORMATION

Type	Package	Order Designation
iC-NQI	TSSOP20 4.4 mm	iC-NQI TSSOP20 iC-NQI TSSOP20 ET -40/125
Evaluation Board		iC-NQI EVAL NQ7D

For technical support, information about prices and terms of delivery please contact:

iC-Haus GmbH
Am Kuemmerling 18
D-55294 Bodenheim
GERMANY

Tel.: +49 (61 35) 92 92-0
Fax: +49 (61 35) 92 92-192
Web: http://www.ichaus.com
E-Mail: sales@ichaus.com

Appointed local distributors: http://www.ichaus.com/sales_partners