H0548
Serial Input
Dot Matrix LCD Driver

HUGHES AIRCRAFT COMPANY
SEMICONDUCTOR DIVISION
Industrial Electronics Group

DESCRIPTION

Hughes 0548 is a CMOS/LSI circuit which drives rectangular matrix LCD displays under microcomputer control. The display itself may be a standard x-y array or a custom array that geometrically is not regular at all. Applications include games, bar graphs, and various custom patterns.

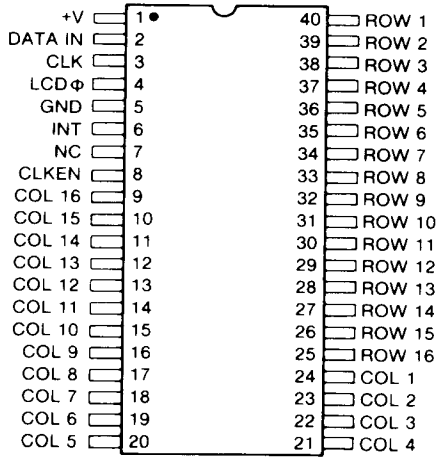
The 0548 is organized as 16 rows and 16 columns. It will drive an LCD display of up to 16 x 16 directly and can be cascaded for larger displays with additional 0548's or other Hughes LCD drivers. Data is input serially to maximize the number of output pins and minimize the number of control pins. This circuit drives (using a multiplexed scheme) the display with proper voltage level AC waveforms, but does not handle refresh or character encoding. This results in lower parts cost and greater design flexibility, but puts more burden on the microcomputer. The 0548 can be used with an 0539 to drive a display that has up to 16 rows and an arbitrary number of columns.

The 0548 is available in a 40 lead hermetic dual-in-line ceramic package (D suffix), plastic package (P suffix), cerdip (Y suffix) or leadless chip carrier (L suffix). Devices in chip form (H suffix) are available upon request.

FEATURES

- Direct drive of matrix LCDs
- Cascadable for larger displays
- On chip oscillator
- CMOS construction for:
  - Wide supply voltage range
  - Low power operation
  - High noise immunity
  - Wide temperature range
- CMOS, NMOS, and T^2L compatible inputs
- Requires only 3 control lines
- Flexible organization allows arbitrary display patterns
- Interrupt Output to request data from microcomputer

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

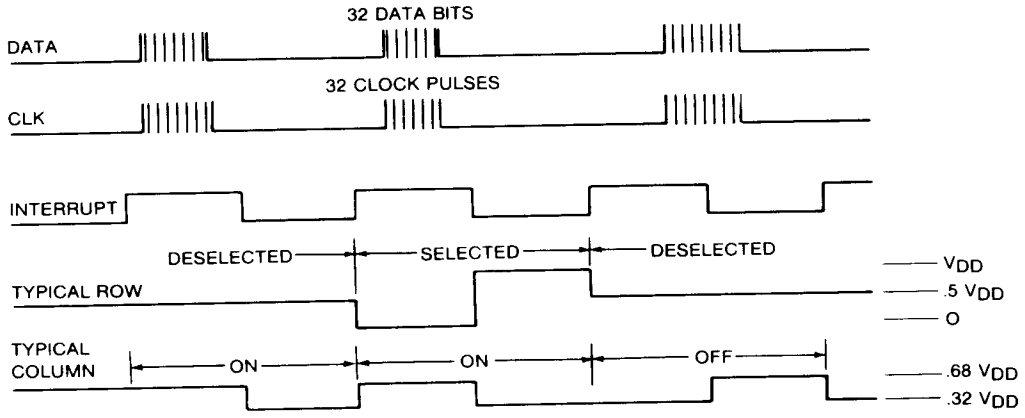
V_{DD}	−.3 to + 17 volts
Inputs	+ V_{DD} − 17 to + V_{DD} + .3 volts
Power Dissipation	250 mW
Operating Temperature	
Ceramic Package	− 55 to + 125°C
Plastic Package	− 40 to + 85°C
Storage Temperature	− 65 to + 125°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

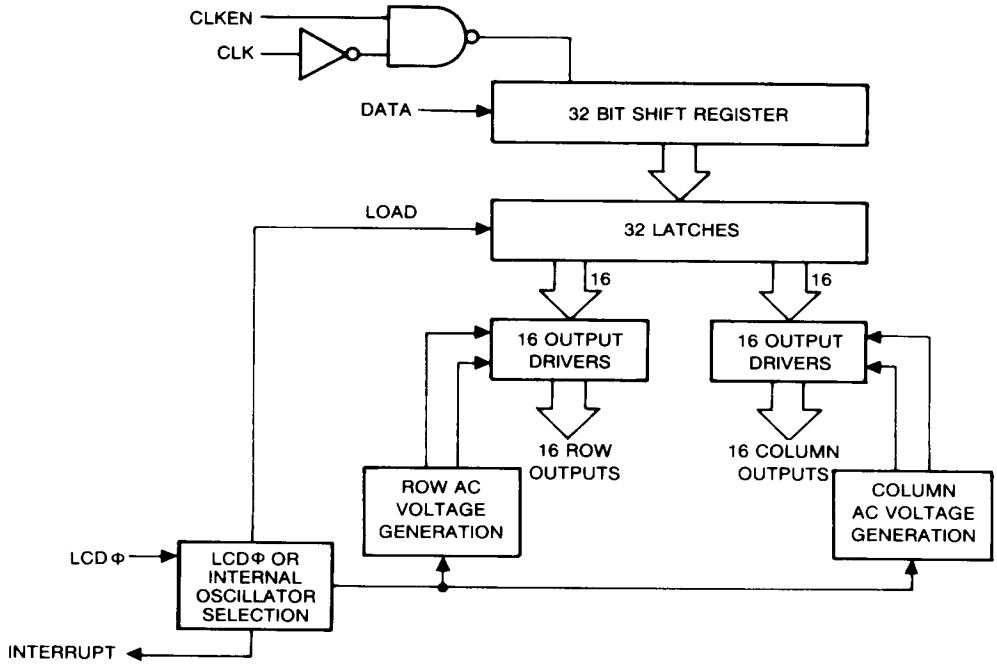
ELECTRICAL CHARACTERISTICS at T_A = + 25°C and V_{DD} = 5V unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		3	12	V
Supply Current	I_{DD}			750	µA
Input High Level	V_{IH}		.75V_{DD}	V_{DD}	V
Input Low Level	V_{IL}		V_{DD}−15	.25V_{DD}	V
Input Leakage	I_L			5	µA
Input Capacitance	C_I			5	pf
Row Output High	V_{OH}		V_{DD}−.05	V_{DD}	V
Row Output Low	V_{OL}		0	.05	V
Row Output Unselected	V_{OM}		.5V_{DD}−.05	.5V_{DD}+.05	V
Column Output High	V_{OH}		.68V_{DD}−.05	.68V_{DD}+.05	V
Column Output Low	V_{OL}		.32V_{DD}−.05	.32V_{DD}+.05	V
Row and Column Output Impedance	R_{ON}	I_L = 10 µA		40	KΩ
Interrupt Output Impedence	R_{ON}	I_L = 100 µA		1.5	KΩ
Clock Rate	f		DC	1.5	MHz
Data in Setup Time	t_{DS}	Data change to clock fall	300		nsec.
Data in Hold Time	t_{DH}	Clock fall to data change	100		nsec.
LCDΦ High Level	V_{IH}		.9V_{DD}	V_{DD}	V
LCDΦ Low Level	V_{IL}		0	.1V_{DD}	V
LCDΦ Input Impedance	R_{IN}		1	3	MΩ

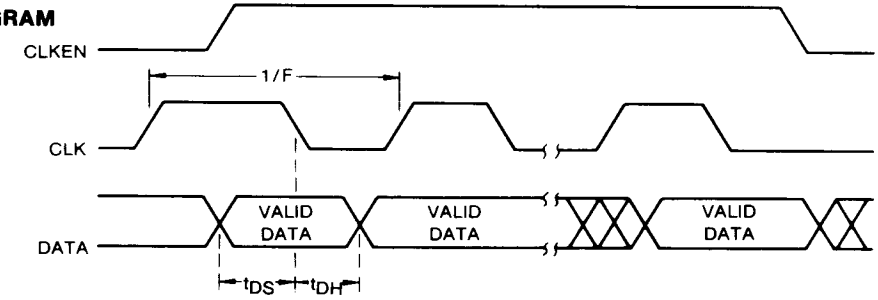
TYPICAL WAVEFORMS



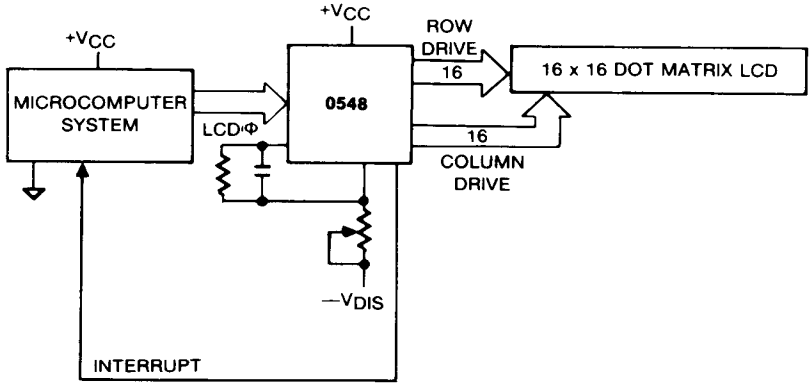
BLOCK DIAGRAM



TIMING DIAGRAM



TYPICAL SYSTEM BLOCK DIAGRAM



OPERATING NOTES

1. The Shift register loads and shifts on the falling edge of clock.
2. A logic 1 on Data In causes a segment to be visible.
3. A parallel transfer of data from the shift register to the latches occurs upon the rising edge of Interrupt Output.
4. Row waveforms are out of phase with Interrupt Output if selected and at mid-point voltage otherwise. Levels are V_{DD}, 0, and $V_{DD}/2$.
5. Column waveforms are in phase with Interrupt Output if selected and out of phase if not selected. Levels are .32 V_{DD} and .68 V_{DD}.
6. The intended mode of operation is as follows:
   a. Interrupt Output frequency is the minimum no flicker frequency (> 30Hz) times the number of backplanes utilized.
   b. Interrupt Output is exactly 50% duty cycle (to keep DC off the display) and is synchronized with loading the data from shift register to latches.
   c. In between each Interrupt Output rising edge, serial data is loaded for the next row to await the next Interrupt Output rising edge, which causes parallel transfer from shift register to display latches.
   d. The Interrupt Output goes to the microcomputer and is treated as a refresh request, or the microcomputer drives the LCDΦ input with 50% duty cycle.
   e. Backplanes are addressed sequentially and individually.
7. The LCDΦ pin can be used in two modes. If LCDΦ is driven, the Interrupt Output will follow it. LCDΦ will also oscillate if a resistor and capacitor are connected in parallel to ground. The resistor value should be at least 1MΩ. The approximate relationship is $f_{out} = \frac{1}{RC}$, which appears at Interrupt Output.
8. To cascade and synchronize several circuits, either connect Interrupt Output of one circuit to LCDΦ of all other circuits (thus one oscillator provides frequency control for all circuits) or connect LCDΦ of all circuits to a common driving signal. Then connect all clock lines together to the clock signal and connect each Data In to a different line of the data bus, allowing a parallel loading of all circuits' serial data. It is also possible to tie all data lines together and drive each clock individually like a chip select. Another alternative is to use the clock enable to allow reading data into specific circuits.
9. There are two obvious signal races to be avoided.
   a. Changing data when clock is falling, and
   b. Allowing Interrupt Output rising edge to be very close to clock falling edge.
10. If supply voltage is altered to optimize LCD contrast or for temperature compensation, it is best to tie all positive supply terminals in common and vary the negative supply. This prevents inadvertently forward biasing diodes.
11. Output locations correspond to a clockwise advancing shift register, thus Row 1 is the last data loaded and Col 16 is the first data loaded.
12. The RMS voltages this circuit delivers to individual LCD pixels depends on V_{DD} and the number of backplanes (N) used according to the following equations:

$$V_{RMS\ OFF} = V_{DD}\sqrt{\frac{.0324\ N + .07}{N}}$$

$$V_{RMS\ ON} = V_{DD}\sqrt{\frac{.0324\ N + .43}{N}}$$

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