# Am2907/Am2908

Quad Bus Transceivers with Interface Logic



## DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceiver
- D-type driver register with open-collector bus driver output can sink 100mA at 0.8V max.
- Internal 4-bit odd parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Am2907 has 2.0V input receiver threshold; Am2908 is "DECQ or LSI-II bus compatible" with 1.5V receiver threshold

## GENERAL DESCRIPTION

The Am2907 and Am2908 are high-performance bus transceivers intended for bipolar or MOS microprocessor system applications. The Am2908 is Digital Equipment Corporation "Q or LSI-II bus compatible" while the Am2907 features a 2.0V receiver threshold. These devices consist of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches, that feature three-state outputs. The devices also contain a four-bit odd parity checker/generator.

These LSI bus transceivers are fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the $A_i$ data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2907 and Am2908 feature a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

The Am2907 has receiver threshold typically of 2.0V while the Am2908 threshold is typically 1.5V.

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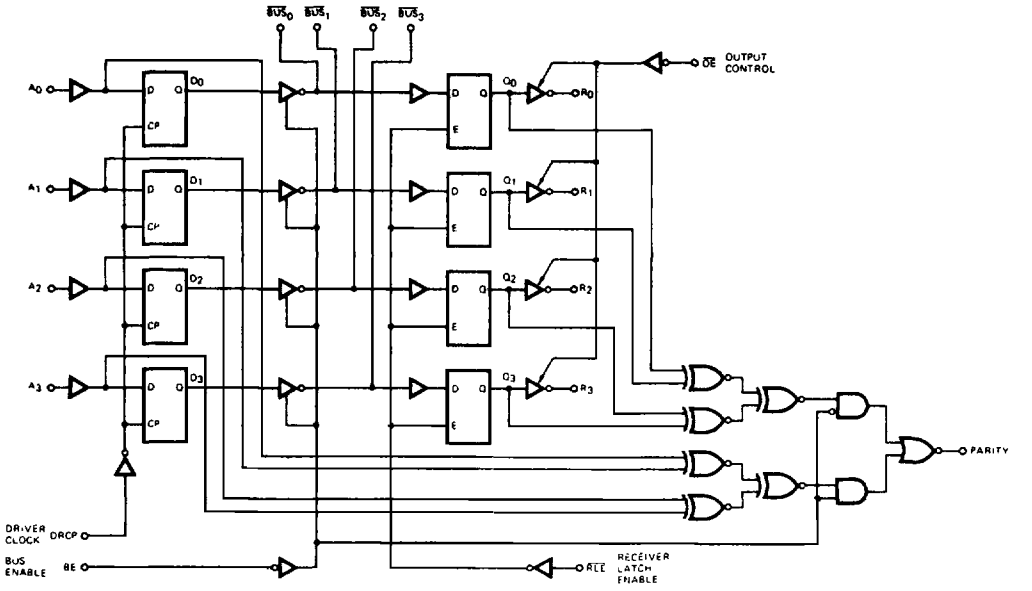
Refer to Page 13-1 for Essential Information on Military Devices

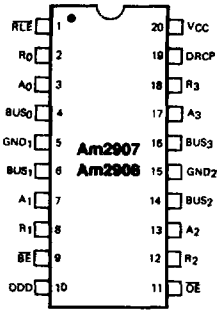
## BLOCK DIAGRAM




BD001890

## CONNECTION DIAGRAM
### Top View

D-20-1




CD003060

Note: Pin 1 is marked for orientation

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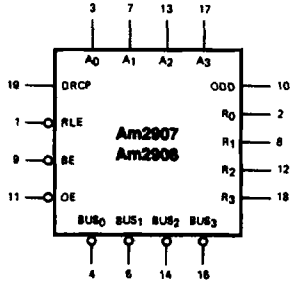
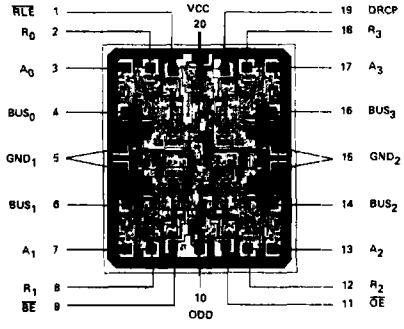
## LOGIC SYMBOL




LS000840

## METALLIZATION AND PAD LAYOUT




**DIE SIZE 0.088" x 0.103"**

## ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

**Am2907/ Am2908**

**D C B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - P – 20-pin plastic DIP
  - X – Dice

Device type
Quad Bus Transceivers

| Valid Combinations | |
|---|---|
| Am2907<br>Am2908 | PC<br>DC, DCB, DM, DMB<br>FM, FMB<br>XC, XM |

**Valid Combinations**

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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Refer to Page 13-1 for Essential Information on Military Devices

## PIN DESCRIPTION

| Pin No. | Name | I/O | Description |
|---|---|---|---|
| 3, 7<br>13, 17 | $A_0$, $A_1$<br>$A_2$, $A_3$ | I | The four driver register inputs. |
| 19 | DRCP | I | Driver Clock Pulse: Clock pulse for the driver register. |
| 9 | $\overline{BE}$ | I | Bus Enable. When the Bus Enable is HIGH. The four drivers are in the high impedance state. |
| 4<br>6<br>14<br>16 | $\overline{BUS}_0$,<br>$\overline{BUS}_1$,<br>$\overline{BUS}_2$,<br>$\overline{BUS}_3$ | I/O | The four driver outputs and receiver inputs (data is inverted). |
| 2, 8, 12, 18 | $R_0$, $R_1$,<br>$R_2$, $R_3$ | O | The four receiver outputs. Data from the bus is inverted while data from the A inputs is non-inverted. |
| 1 | $\overline{RLE}$ | O | Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs. |
| 10 | ODD | O | Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state. |
| 11 | $\overline{OE}$ | I | Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state. |

## TRUTH TABLE

| INPUTS | | | | | INTERNAL TO DEVICE | | BUS | OUTPUT | |
|---|---|---|---|---|---|---|---|---|---|
| $A_i$ | DRCP | $\overline{BE}$ | $\overline{RLE}$ | $\overline{OE}$ | $D_i$ | $Q_i$ | $B_i$ | $R_i$ | FUNCTION |
| X | X | H | X | X | X | X | H | X | Driver output disable |
| X | X | X | X | H | X | X | X | Z | Receiver output disable |
| X<br>X | X<br>X | H<br>H | L<br>L | L<br>L | X<br>X | L<br>H | L<br>H | H<br>L | Driver output disable and receive data via Bus input |
| X | X | X | H | X | X | NC | X | X | Latch received data |
| L<br>H | ↑<br>↑ | X<br>X | X<br>X | X<br>X | L<br>H | X<br>X | X<br>X | X<br>X | Load driver register |
| X<br>X | L<br>H | X<br>X | X<br>X | X<br>X | NC<br>NC | X<br>X | X<br>X | X<br>X | No driver clock restrictions |
| X | X | L | X | X | H | X | L | X | Drive Bus |

H = HIGH  Z = HIGH Impedance  X = Don't care  i = 0, 1, 2, 3
L = LOW  NC = No change  ↑ = LOW to HIGH transition

## PARITY OUTPUT FUNCTION TABLE

| $\overline{BE}$ | ODD PARITY OUTPUT |
|---|---|
| L | ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$ |
| H | ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$ |

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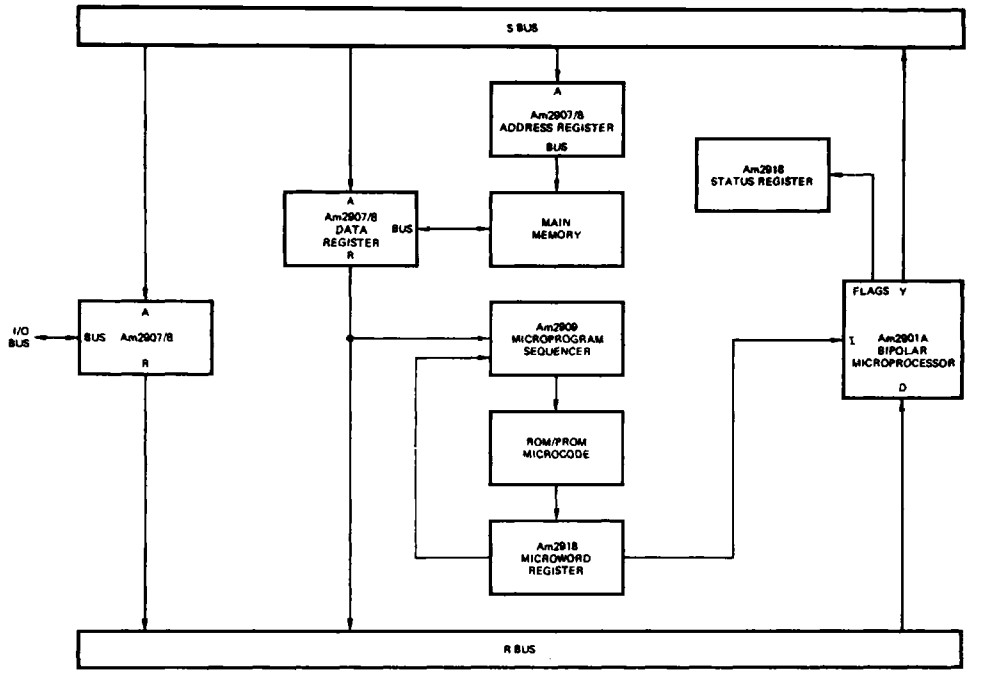
Refer to Page 13-1 for Essential Information on Military Devices

## APPLICATIONS




AF001000

The Am2907 can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs for
High Output State ..... −0.5V to +$V_{CC}$ max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Bus ..... 200mA
DC Output Current, Into Outputs
(Except Bus) ..... 30mA
DC Input Current ..... −30mA to +5.0mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Parameters | Description | Test Conditions (Note 2) | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Receiver Output HIGH Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IL}$ or $V_{IH}$ | MIL: $I_{OH}$ = −1.0mA | 2.4 | 3.4 | | Volts |
| | | | COM'L: $I_{OH}$ = −2.6mA | 2.4 | 3.4 | | |
| $V_{OH}$ | Parity Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −660µA, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL | 2.5 | 3.4 | | Volts |
| | | | COM'L | 2.7 | 3.4 | | |
| $V_{OL}$ | Output LOW voltage (Except Bus) | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IL}$ or $V_{IH}$ | $I_{OL}$ = 4mA | | 0.27 | 0.4 | Volts |
| | | | $I_{OL}$ = 8mA | | 0.32 | 0.45 | |
| | | | $I_{OL}$ = 12mA | | 0.37 | 0.5 | |
| $V_{IH}$ | Input HIGH Level (Except Bus) | Guaranteed input logical HIGH for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level (Except Bus)( | Guaranteed input logical LOW for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage (Except Bus) | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ | Input LOW Current (Except Bus) | $V_{CC}$ = MAX, $V_{IN}$ = 0.4V | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current (Except Bus) | $V_{CC}$ = MAX, $V_{IN}$ = 2.7V | | | | 20 | µA |
| $I_I$ | Input HIGH Current (Except Bus) | $V_{CC}$ = MAX, $V_{IN}$ = 5.5V | | | | 100 | µA |
| $I_{SC}$ | Output Short Circuit Current (Except Bus) | $V_{CC}$ = MAX | | −12 | | −65 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX, All inputs = GND | Am2907 | | 75 | 110 | mA |
| | | | Am2908 | | 80 | 120 | |
| $I_O$ | Off-State Output Current (Receiver Outputs) | $V_{CC}$ = MAX | $V_O$ = 2.4V | | | 20 | µA |
| | | | $V_O$ = 0.4V | | | −20 | |

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Refer to Page 13-1 for Essential Information on Military Devices

## BUS INPUT/OUTPUT CHARACTERISTICS over operating temperature range

| Parameters | Description | Test Conditions (Note 2) | | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Bus Output LOW Voltage | $V_{CC}$ = MIN | $I_{OL}$ = 40mA | | | 0.32 | 0.5 | Volts |
| | | | $I_{OL}$ = 70mA | | | 0.41 | 0.7 | |
| | | | $I_{OL}$ = 100mA | | | 0.55 | 0.8 | |
| $I_O$ | Bus Leakage Current | $V_{CC}$ = MAX | $V_O$ = 0.4V | | | | -50 | μA |
| | | | $V_O$ = 4.5V | MIL | | | 200 | |
| | | | | COM'L | | | 100 | |
| $I_{OFF}$ | Bus Leakage Current (Power Off) | $V_O$ = 4.5V | | | | | 100 | μA |
| $V_{TH}$ | Receiver Input HIGH Threshold | Bus Enable = 2.4V | Am2907 | MIL | 2.4 | 2.0 | | Volts |
| | | | | COM'L | 2.3 | 2.0 | | |
| | | | Am2908 | MIL | 1.9 | 1.5 | | |
| | | | | COM'L | 1.7 | 1.5 | | |
| $V_{TL}$ | Receiver Input LOW Threshold | Bus Enable = 2.4V | Am2907 | MIL | | 2.0 | 1.5 | Volts |
| | | | | COM'L | | 2.0 | 1.6 | |
| | | | Am2908 | MIL | | 1.5 | 1.1 | |
| | | | | COM'L | | 1.5 | 1.3 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = -18mA | | | | | -1.2 | Volts |

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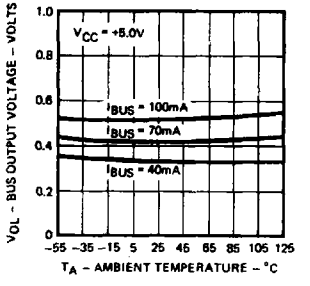
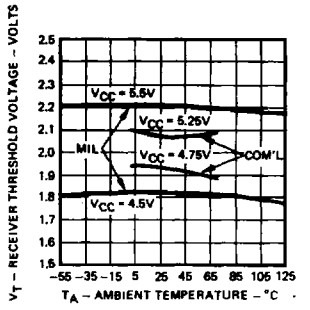
## TYPICAL PERFORMANCE CURVES

**Bus Output Low Voltage Versus Ambient Temperature**



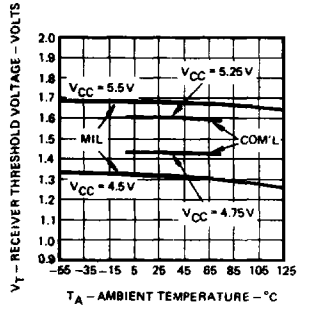

OP001340

**Am2907 Receiver Threshold Variation Versus Ambient Temperature**




OP001330

**Am2908 Receiver Threshold Variation Versus Ambient Temperature**




OP001420

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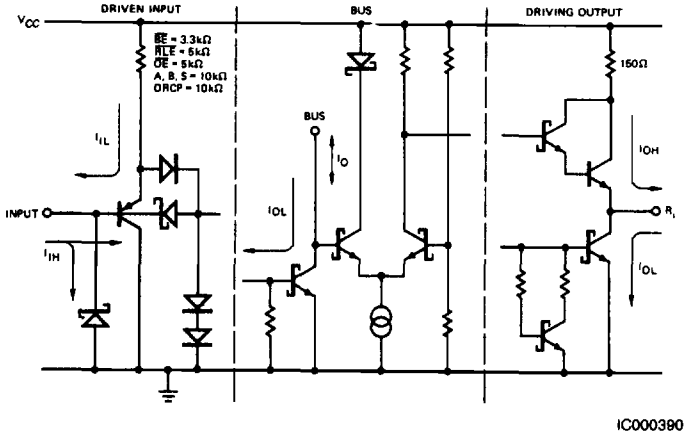
Refer to Page 13-1 for Essential Information on Military Devices

## INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| Parameters | Description | Test Conditions | COMMERCIAL Am2907 Min | COMMERCIAL Am2907 Typ (Note 1) | COMMERCIAL Am2907 Max | MILITARY Am2907 Min | MILITARY Am2907 Typ (Note 1) | MILITARY Am2907 Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | Driver Clock (DRCP) to Bus | $C_L$ (BUS) = 50 pF, $R_L$ (BUS) = 50 Ω | | 21 | 36 | | 21 | 40 | ns |
| $t_{PLH}$ | | | | 21 | 36 | | 21 | 40 | |
| $t_{PHL}$ | Bus Enable ($\overline{BE}$) to Bus | | | 13 | 23 | | 13 | 26 | ns |
| $t_{PLH}$ | | | | 13 | 23 | | 13 | 26 | |
| $t_s$ | Data Inputs | $C_L$ = 15 pF, $R_L$ = 2.0 kΩ | 15 | | | 18 | | | ns |
| $t_h$ | | | 7.0 | | | 8.0 | | | |
| $t_{PW}$ | Clock Pulse Width (HIGH) | | 25 | | | 28 | | | ns |
| $t_{PLH}$ | Bus to Receiver Output (Latch Enabled) | | | 18 | 34 | | 18 | 37 | ns |
| $t_{PHL}$ | | | | 18 | 34 | | 18 | 37 | |
| $t_{PLH}$ | Latch Enable to Receiver Output | | | 21 | 34 | | 21 | 37 | ns |
| $t_{PHL}$ | | | | 21 | 34 | | 21 | 37 | |
| $t_s$ | Bus to Latch Enable ($\overline{RLE}$) | | 18 | | | 21 | | | ns |
| $t_h$ | | | 5.0 | | | 7.0 | | | |
| $t_{PLH}$ | Data to Odd Parity Out (Driver Enabled) | | | 21 | 36 | | 21 | 40 | ns |
| $t_{PHL}$ | | | | 21 | 36 | | 21 | 40 | |
| $t_{PLH}$ | Bus to Odd Parity Out (Driver Inhibit) | | | 21 | 36 | | 21 | 40 | ns |
| $t_{PHL}$ | | | | 21 | 36 | | 21 | 40 | |
| $t_{PLH}$ | Latch Enable ($\overline{RLE}$) to Odd Parity Output | | | 21 | 36 | | 21 | 40 | ns |
| $t_{PHL}$ | | | | 21 | 36 | | 21 | 40 | |
| $t_{ZH}$ | Output Control to Output | | | 14 | 25 | | 14 | 28 | ns |
| $t_{ZL}$ | | | | 14 | 25 | | 14 | 28 | |
| $t_{HZ}$ | Output Control to Output | $C_L$ = 5.0 pF, $R_L$ = 2.0 kΩ | | 14 | 25 | | 14 | 28 | ns |
| $t_{LZ}$ | | | | 14 | 25 | | 14 | 28 | |

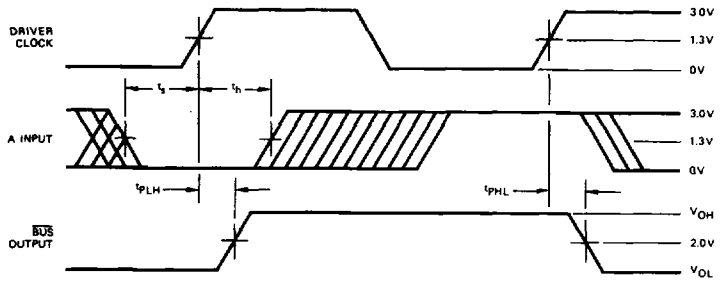
Notes: 1. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| Parameters | Description | Test Conditions | COMMERCIAL Am2908 Min | COMMERCIAL Am2908 Typ (Note 1) | COMMERCIAL Am2908 Max | MILITARY Am2908 Min | MILITARY Am2908 Typ (Note 1) | MILITARY Am2908 Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | Driver Clock (DRCP) to Bus | $C_L$ (BUS) = 50 pF<br>$R_L$ (BUS):<br>91 Ω to $V_{CC}$<br>200 Ω to GND | | 21 | 36 | | 21 | 40 | ns |
| $t_{PLH}$ | | | | 21 | 36 | | 21 | 40 | |
| $t_{PHL}$ | Bus Enable ($\overline{BE}$) to Bus | | | 13 | 23 | | 13 | 26 | ns |
| $t_{PLH}$ | | | | 13 | 23 | | 13 | 26 | |
| $t_r$ | Bus Output Rise Time | | 7 | 10 | | 5 | 10 | | ns |
| $t_f$ | Bus Output Fall Time | | 4 | 6 | | 3 | 6 | | |
| $t_s$ | Data Inputs | | 15 | | | 18 | | | ns |
| $t_h$ | | | 7.0 | | | 8.0 | | | |
| $t_{PW}$ | Clock Pulse Width (HIGH) | | 25 | | | 28 | | | ns |
| $t_{PLH}$ | Bus to Receiver Output (Latch Enabled) | $C_L$ = 50 pF<br>$R_L$ = 2.0 kΩ | | 18 | 35 | | 18 | 38 | ns |
| $t_{PHL}$ | | | | 18 | 35 | | 18 | 38 | |
| $t_{PLH}$ | Latch Enable to Receiver Output | | | 21 | 35 | | 21 | 38 | ns |
| $t_{PHL}$ | | | | 21 | 35 | | 21 | 38 | |
| $t_s$ | Bus to Latch Enable ($\overline{RLE}$) | | 18 | | | 21 | | | ns |
| $t_h$ | | | 5.0 | | | 7.0 | | | |
| $t_{PLH}$ | Data to Odd Parity Out (Driver Enabled) | $C_L$ = 15 pF<br>$R_L$ = 2.0 kΩ | | 21 | 36 | | 21 | 40 | ns |
| $t_{PHL}$ | | | | 21 | 36 | | 21 | 40 | |
| $t_{PLH}$ | Bus to Odd Parity Out (Driver Inhibit) | | | 21 | 36 | | 21 | 40 | ns |
| $t_{PHL}$ | | | | 21 | 36 | | 21 | 40 | |
| $t_{PLH}$ | Latch Enable ($\overline{RLE}$) to Odd Parity Output | | | 21 | 36 | | 21 | 40 | ns |
| $t_{PHL}$ | | | | 21 | 36 | | 21 | 40 | |
| $t_{ZH}$ | Output Control to Output | | | 14 | 25 | | 14 | 28 | ns |
| $t_{ZL}$ | | | | 14 | 25 | | 14 | 28 | |
| $t_{HZ}$ | Output Control to Output | $C_L$ = 5.0 pF<br>$R_L$ = 2.0 kΩ | | 14 | 25 | | 14 | 28 | ns |
| $t_{LZ}$ | | | | 14 | 25 | | 14 | 28 | |

Notes: 1. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.

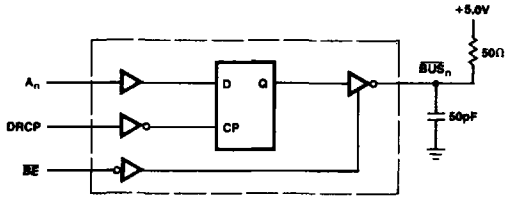
## SWITCHING WAVEFORMS




WF002430

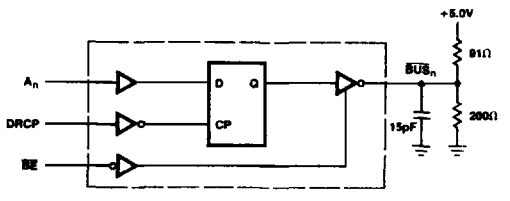
**INPUT SET-UP AND HOLD TIMES.**

## SWITCHING TEST CIRCUIT




TC000950

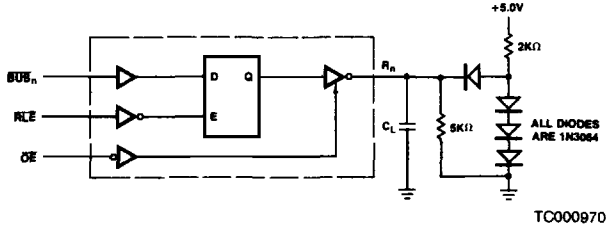
**Am2907**
**DRIVER SWITCHING TEST CIRCUIT**




TC000960

**Am2908**
**DRIVER SWITCHING TEST CIRCUIT**

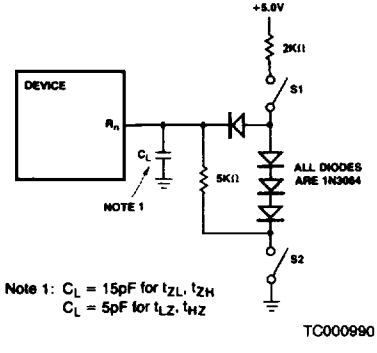
## SWITCHING TEST CIRCUIT




TC000970

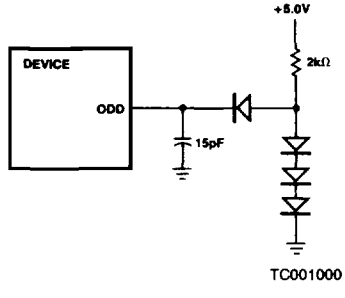
Note: $C_L$ = 15pF for Am2907
$C_L$ = 50pF for Am2908

**Am2907/08 RECEIVER SWITCHING TEST CIRCUIT.**




TC000990

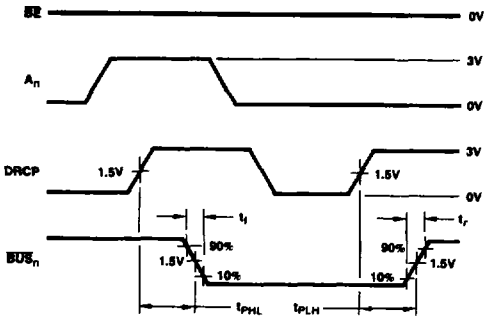
**LOAD FOR RECEIVER TRI-STATE TEST**




TC001000

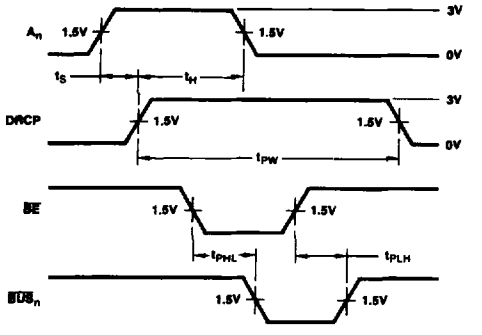
**LOAD FOR PARITY OUTPUT**

## SWITCHING WAVEFORMS



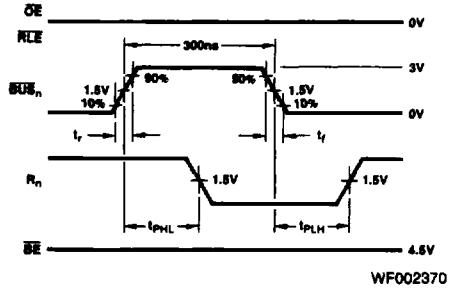

WF002340

**DRIVER CLOCK (DRCP) TO BUS**



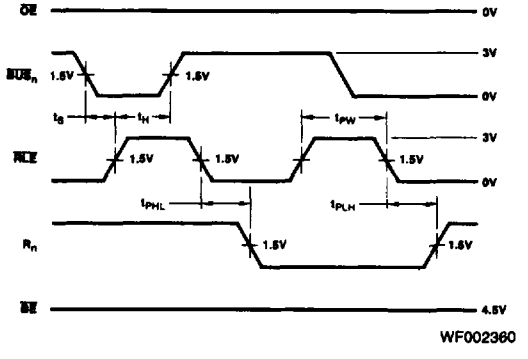

WF002330

**BUS ENABLE ($\overline{BE}$) TO BUS**




WF002370

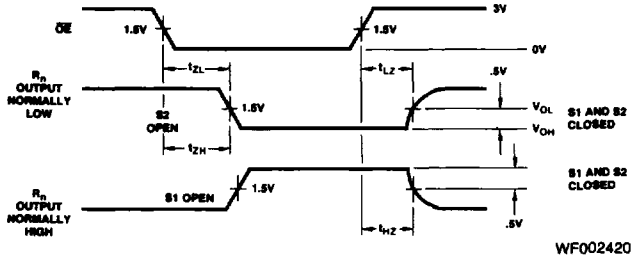
**BUS TO RECEIVER OUTPUT (LATCH ENABLED)**




WF002360

**LATCH ENABLE TO RECEIVER OUTPUT**

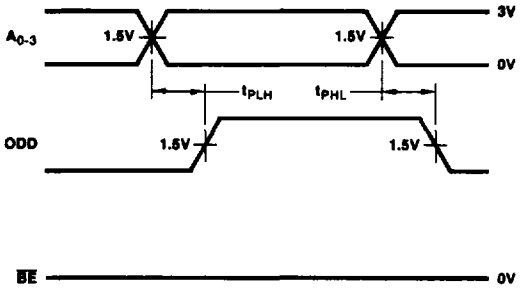
## SWITCHING WAVEFORMS



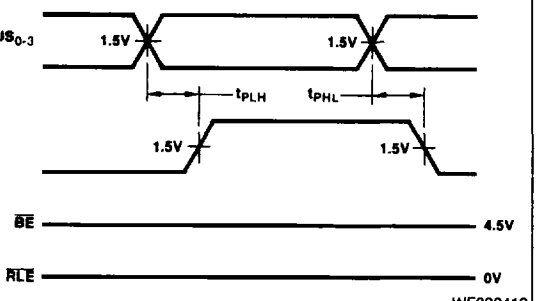

WF002420

**RECEIVER TRI-STATE WAVEFORMS**

05399A




A INPUT TO PARITY OUTPUT




BUS TO PARITY OUTPUT