

SRAM MODULE

128K x 32 SRAM LOW VOLTAGE

FEATURES

- High speed: 17, 20 and 25ns
- High-density 512KB design
- High-performance, low-power, CMOS double-metal process
- Single +3.3V $\pm 0.3V$ power supply
- 5V-tolerant I/O
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- All inputs and outputs are TTL-compatible
- Industry-standard pinout
- Low profile
- Upgradable to a 256K x 32 module

OPTIONS

- Timing
 - 17ns access -17
 - 20ns access -20
 - 25ns access -25
- Packages
 - 64-pin SIMM M
 - 64-pin ZIP Z
- 2V data retention (optional) L
- 2V data retention, low power (optional) LP
- Part Number Example: MT4LS12832M-20 LP

MARKING

NOTE: Not all combinations of speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

GENERAL DESCRIPTION

The MT4LS12832 is a high-speed SRAM memory module containing 131,072 words organized in a x32-bit configuration. The module consists of four low voltage 128K x 8 fast SRAMs mounted on a 64-pin, single-sided, FR4-printed circuit board.

Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in a High-Z state for additional flexibility in system design and memory expansion.

PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry-standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

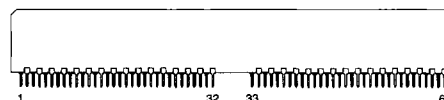
The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single

PIN ASSIGNMENT (Top View)

64-Pin SIMM (SE-2)



64-Pin ZIP (SG-3)



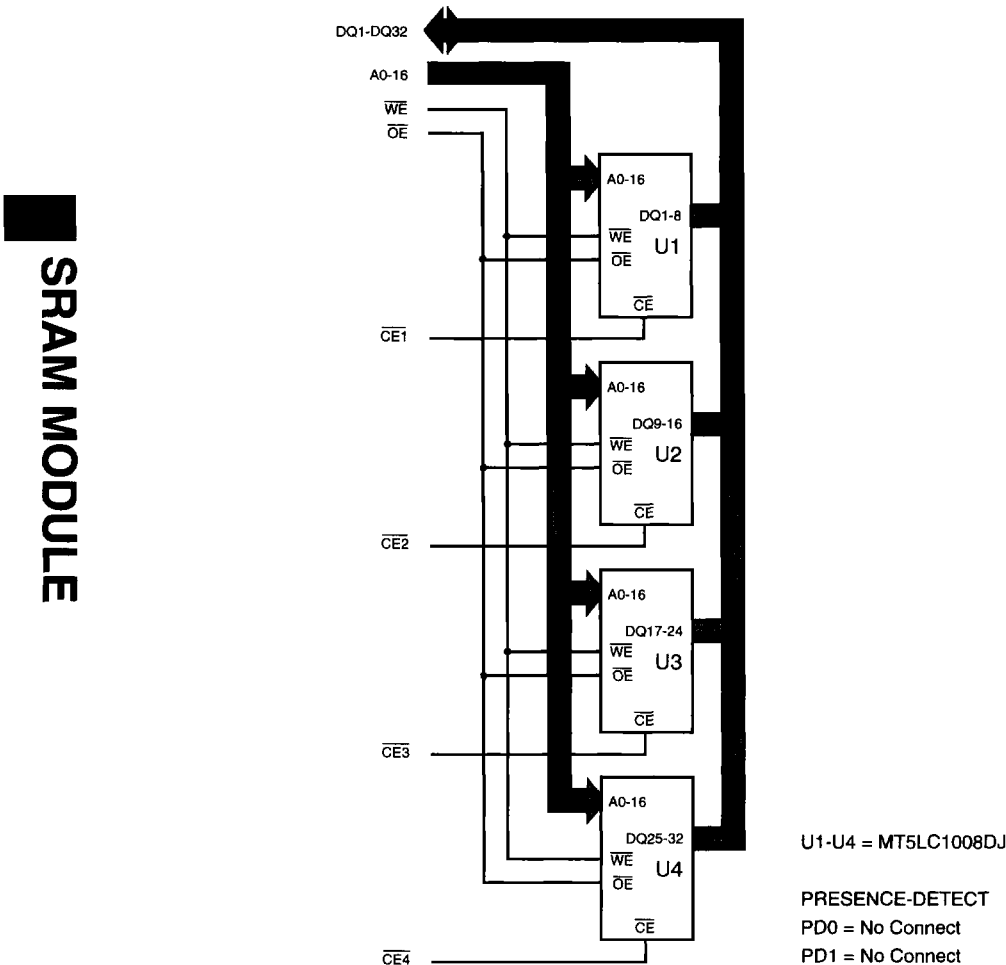
PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	A16	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

+3.3V DC supply and all inputs and outputs are fully TTL-compatible.

The "L" and "LP" versions each provide a significant reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a significant reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

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FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss.....	-0.5V to +4.6V
V _{IN}	-0.5V to +6.0V
Storage temperature	-55°C to +125°C
Power dissipation	4W
Short circuit output current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{cc} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.0	5.5V	V	1, 2
Input Low (Logic 0) Voltage		V _{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}	A0-A16, WE, OE	-4	4	μA	
		CE1-CE4	-1	1	μA	
Output Leakage Current	Output(s) disabled	DQ1-DQ32	-1	1	μA	
	0V ≤ V _{OUT} ≤ V _{CC}					
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V	1
Supply Voltage		V _{CC}	3.0	3.6	V	1

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DESCRIPTION	CONDITIONS	SYMBOL	VER	TYP	MAX			UNITS	NOTES
					-17	-20	-25		
Power Supply Current: Operating	CE ≤ V _{IL} ; V _{CC} = MAX f = MAX = 1/ t _{RC} outputs open	I _{CC}	ALL	280	620	580	540	mA	3, 13
Power Supply Current: Standby	CE ≥ V _{IH} ; V _{CC} = MAX f = MAX = 1/ t _{RC} outputs open	I _{SB1}	STD,L	80	180	160	140	mA	13
			LP	6	12	12	12	mA	
	CE ≥ V _{CC} -0.2V; V _{CC} = MAX V _{IN} ≤ V _{SS} +0.2V or V _{IN} ≥ V _{CC} -0.2V; f = 0	I _{SB2}	STD,L	4	12	12	12	mA	13
			LP	2.8	6	6	6	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A16, WE, OE	T _A = 25°C; f = 1 MHz V _{CC} = 3.3V	C _{I1}	30	pF	4
Input Capacitance: CE1-CE4		C _{I2}	8	pF	4
Input/Output Capacitance: DQ1-DQ32		C _{I/O}	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS(Note 5) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$)

DESCRIPTION		-17		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	¹ RC	17		20		25		ns	
Address access time	¹ AA		17		20		25	ns	
Chip Enable access time	¹ ACE		17		20		25	ns	
Output hold from address change	¹ OH	3		3		5		ns	
Chip Enable to output in Low-Z	¹ LZCE	5		5		5		ns	7
Chip disable to output in High-Z	¹ HZCE		7		8		10	ns	6, 7
Chip Enable to power-up time	¹ PU	0		0		0		ns	
Chip disable to power-down time	¹ PD		17		20		25	ns	
Output Enable access time	¹ AOE		6		7		8	ns	
Output Enable to output in Low-Z	¹ LZOE	0		0		0		ns	
Output disable to output in High-Z	¹ HZOE		6		7		8	ns	6
WRITE Cycle									
WRITE cycle time	¹ WC	17		20		25		ns	
Chip Enable to end of write	¹ CW	12		12		15		ns	
Address valid to end of write	¹ AW	12		12		15		ns	
Address setup time	¹ AS	0		0		0		ns	
Address hold from end of write	¹ AH	0		0		0		ns	
WRITE pulse width	¹ WP1	12		12		15		ns	
WRITE pulse width	¹ WP2	13		15		15		ns	
Data setup time	¹ DS	8		8		10		ns	
Data hold time	¹ DH	0		0		0		ns	
Write disable to output in Low-Z	¹ LZWE	3		3		5		ns	7
Write Enable to output in High-Z	¹ HZWE		7		8		10	ns	6, 7

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AC TEST CONDITIONS

Input pulse levels	V _{SS} to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

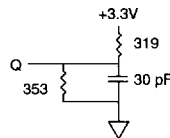


Fig. 1 OUTPUT LOAD EQUIVALENT

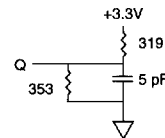


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

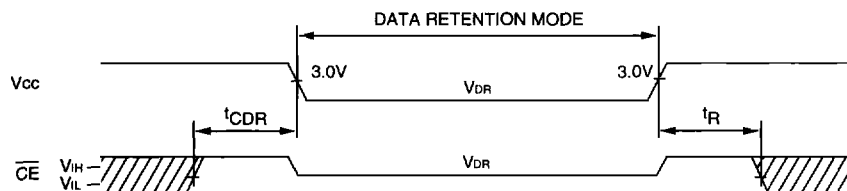
- All voltages referenced to V_{SS} (GND).
- Overshoot: V_{IH} ≤ +6.0V for t ≤ t_{KC}/2
Undershoot: V_{IL} ≥ -2.0V for t ≤ t_{KC}/2
Power-up: V_{IH} ≥ +6.0V and V_{CC} ≤ 3.1V for t ≤ 200 msec.
- I_{CC} is dependent on output loading and cycle rates.
- This parameter is sampled.
- Test conditions as specified with the output loading as shown in Fig. 1, unless otherwise noted.
- t_{HZCE}, t_{HZOE} and t_{HZWE} are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE}.
- $\overline{WE}$ is HIGH for READ cycle.
- Device is continuously selected. All chip enables are held in their active state.
- Address valid prior to, or coincident with, latest occurring chip enable.
- t_{RC}=READ cycle time
- Chip enable and write enable can initiate and terminate a WRITE cycle.
- Typical values are measured at 3.3V, 25°C and 20ns cycle time.
- Typical currents are measured at 25°C.

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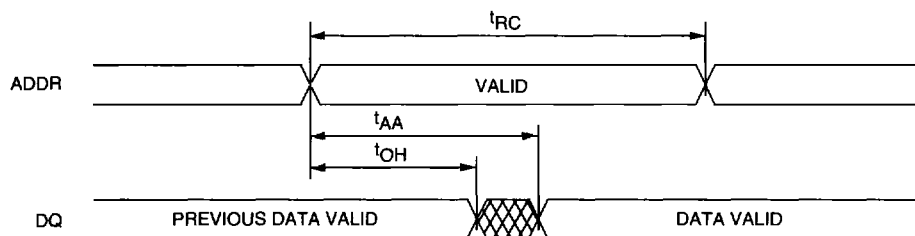
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V _{CC} for Retention Data		V _{DR}	2			V	
Data Retention Current L version	$\overline{CE} \geq V_{CC} - 0.2V$ Other inputs: V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ V _{SS} + 0.2V V _{CC} = 2V	I _{CCDR}		580	1,040	μA	14
Data Retention Current LP version	$\overline{CE} \geq V_{CC} - 0.2V$ V _{CC} = 2V	I _{CCDR}		580	1,040	μA	14
Chip Deselect to Data Retention Time		t _{CDR}	0			ns	4
Operation Recovery Time		t _R	t _{RC}			ns	4, 11

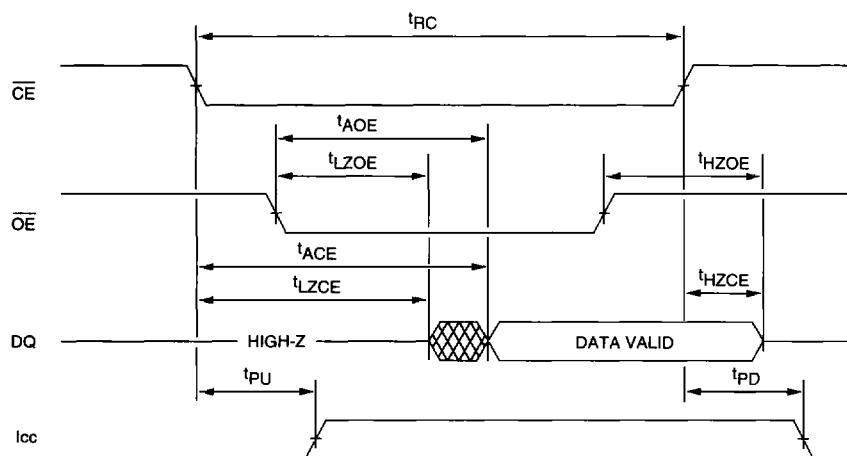
LOW V_{CC} DATA RETENTION WAVEFORM



READ CYCLE NO. 1 8, 9



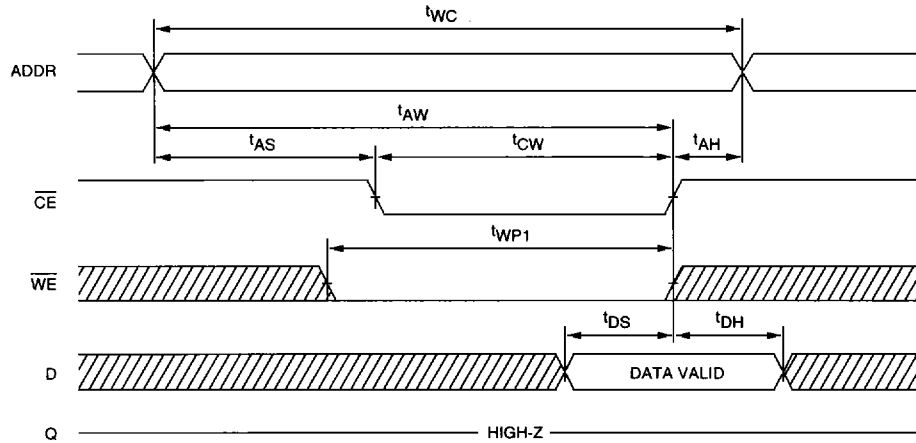
READ CYCLE NO. 2 7, 8, 10



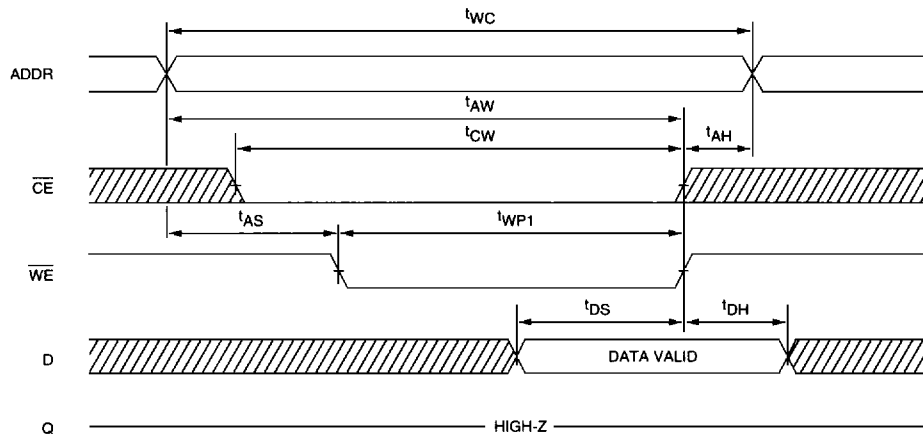
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1¹² (Chip Enable Controlled)



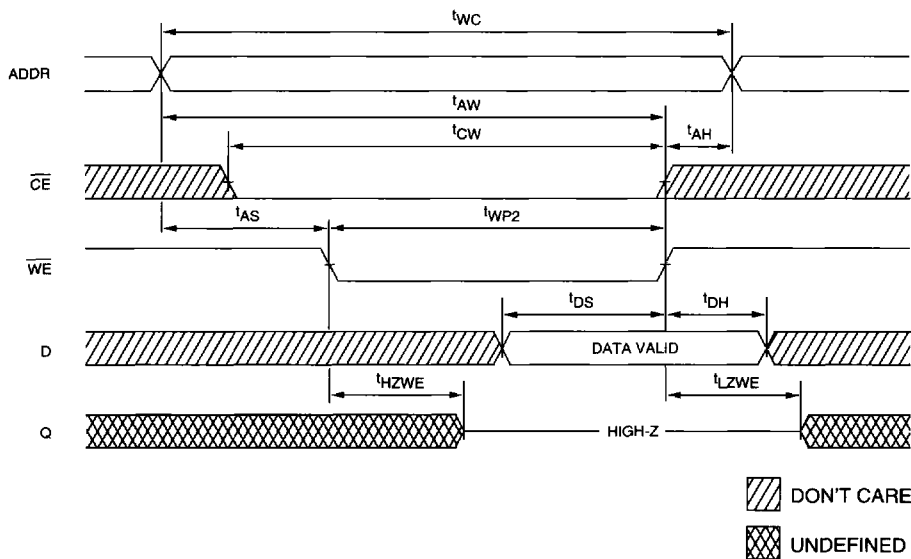
WRITE CYCLE NO. 2¹² (Write Enable Controlled)



DON'T CARE
 UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 ^{7, 12}
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).